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CY96330 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 48MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 20.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

■ 0.18μm CMOS

CPU

■ F^{2}MC-16FX CPU

■ Up to 48 MHz internal, 20.8 ns instruction cycle time

■ Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)

■ 8-byte instruction execution queue

■ Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

■ On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)

■ 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).

■ Up to 48 MHz external clock

■ 32-100 kHz subsystem quartz clock

■ 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog

■ Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.

■ Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)

■ Clock modulator

On-chip voltage regulator

■ Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

Low voltage reset

■ Reset is generated when supply voltage is below minimum.

Code Security

■ Protects ROM content from unintended read-out

Memory Patch Function

■ Replaces ROM content

■ Can also be used to implement embedded debug support

DMA

■ Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

■ Fast Interrupt processing

■ 8 programmable priority levels

■ Non-Maskable Interrupt (NMI)

Timers

■ Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

■ Watchdog Timer

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I^{2}C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

External bus interface

- 8-bit or 16-bit bidirectional data

- Up to 24-bit addresses

- 6 chip select signals

- Multiplexed address/data lines

- Non-multiplexed address/data lines

- Wait state request

- External bus master possible

- Timing programmable

Alarm comparator

- Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds

- Threshold voltages defined externally or generated internally

- Status is readable, interrupts can be masked separately

I/O Ports

- Virtually all external pins can be used as general purpose I/O

- All push-pull outputs (except when used as I2C SDA/SCL line)

- Bit-wise programmable as input/output or peripheral signal

- Bit-wise programmable input enable

- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL

- Bit-wise programmable pull-up resistor

- Bit-wise programmable output driving strength for EMI optimization

Package

- 144-pin plastic LQFP M08

Flash Memory

- Supports automatic programming, Embedded Algorithm

- Write/Erase/Erase-Suspend/Resume commands

- A flag indicating completion of the algorithm

- Number of erase cycles: 10,000 times

- Data retention time: 20 years

- Erase can be performed on each sector individually

- Sector protection

- Flash Security feature to protect the content of the Flash

- Low voltage detection during Flash erase

USB

- USB function (corresponds to USB Full Speed)

- USB Mini-HOST function

- Supports up to 6 endpoints

Contents

1. Product Lineup

Features		CY96V300	CY96(F)33xY/R	CY96(F)33xU
Product type		Evaluation sample	Flash product: CY96F33x Mask ROM product: CY9633x	
Product options				
YS			Low voltage reset persistently on / Single clock devices	
RS			Low voltage reset can be disabled / Single clock devices	
YW		NA	Low voltage reset persistently on / Dual clock devices	
RW			Low voltage reset can be disabled / Dual clock devices	
US			USB / Low voltage reset can be disabled / Single clock devices	
UW			USB / Low voltage reset can be disabled / Dual clock devices	
Flash/ROM	RAM			
288KB	24KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM		CY96F336U
544KB	32KB		CY96F338Y CY96F338R	CY96F338U
Package		BGA416	LQS144	
DMA		16 channels	10 channels	
USART		10 channels	8 channels	
I^{2}C			2 channels	
A/D Converter		40 channels	40 channels	36 channels
A/D Converter Reference Voltage switch		yes	No	
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)	
16-bit Free-Running Timer			4 channels	
16-bit Output Compare			12 channels	
16-bit Input Capture			10 channels	
16-bit Programmable Pulse Generator			20 channels	
CAN Interface		5 channels	3 channels (1 channel for CY96F336U)	
USB		No	No	1 channel
External Interrupts			16 channels	
Non-Maskable Interrupt			1 channel	
Real Time Clock			1	

Features	CY96V300	CY96(F)33xY/R	CY96(F)33xU
I/O Ports	136	122 for part number with suffix "W", 124 for part number with suffix "S"	118 for part number with suffix "W", 120 for part number with suffix "S"
Alarm comparator	2 channels		
External bus interface	Yes		
Chip select	6 signals		
Clock output function	2 channels		
Low voltage reset	Yes		
On-chip RC-oscillator	Yes		

2. Block Diagram

Block diagram of CY96(F)33xY/R

*1: Available only on devices with suffix "W"

Block diagram of CY96(F)33xU
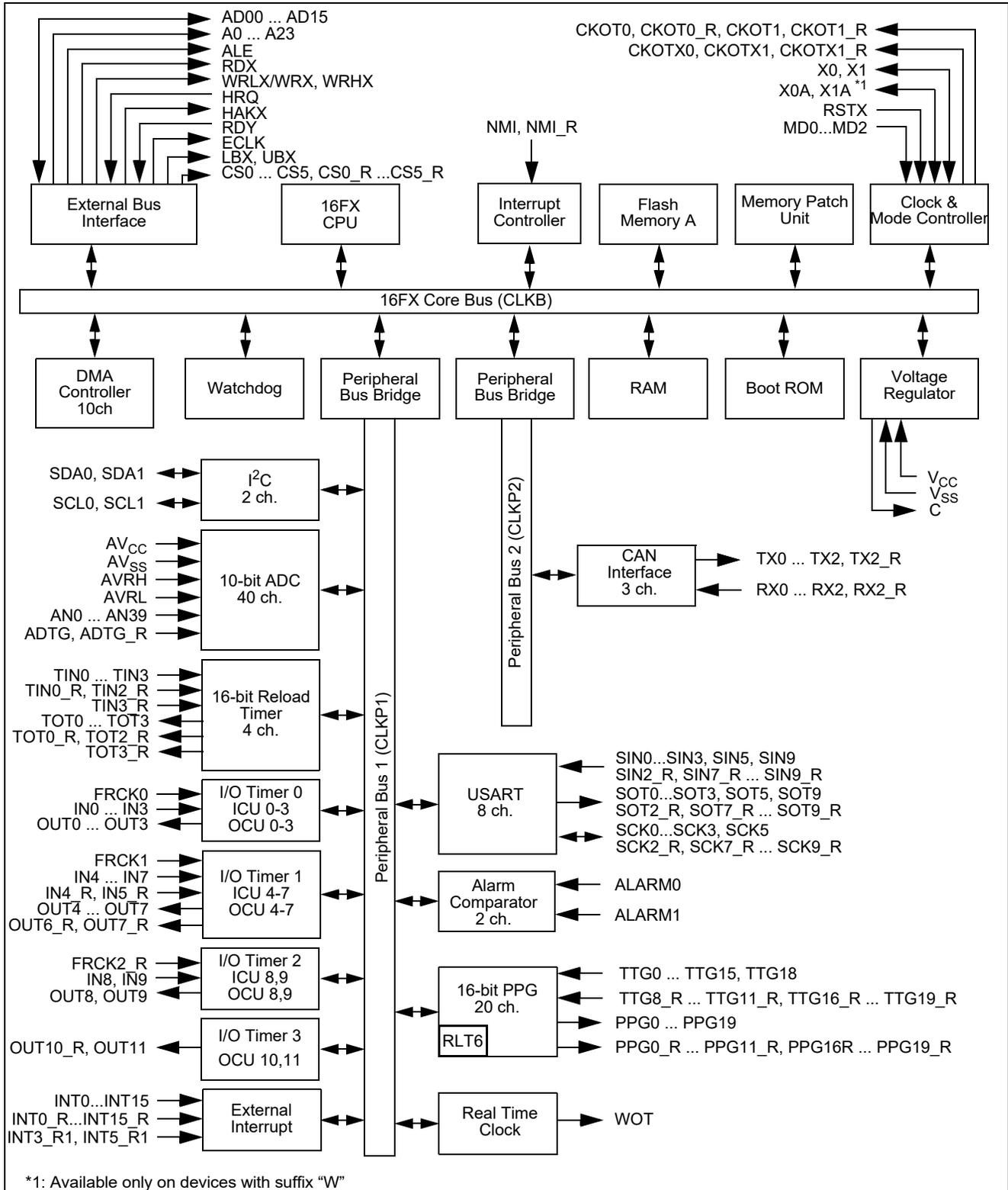
*1: Available only on devices with suffix "W"
*2 : CAN1 and CAN2 not available on CY96F336U
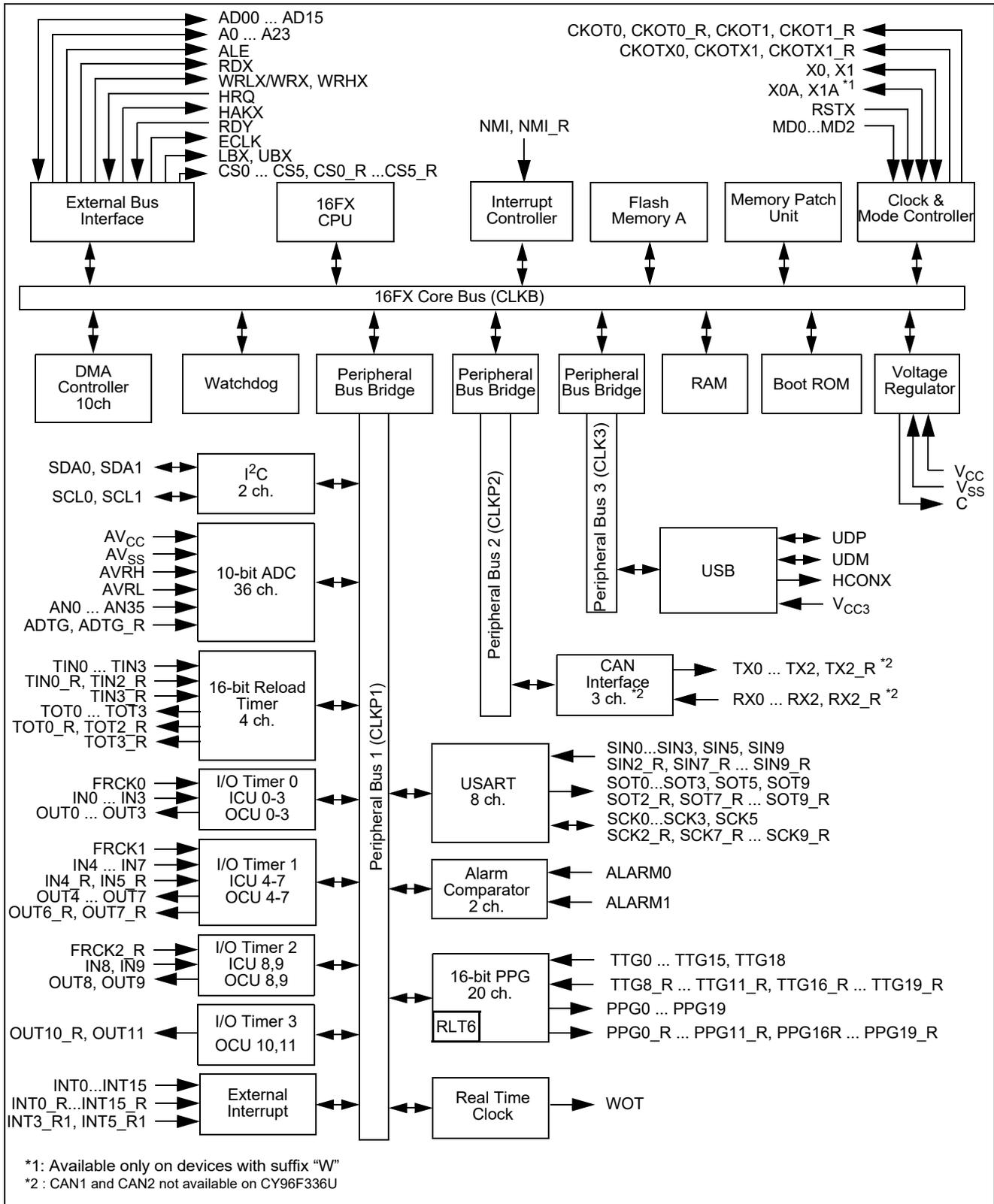
3. Pin Assignments

Pin assignment of CY96F33xY/R (LQS144)

LQFP - 144

Package code (mold)
LQS144

(LQS144)

*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1
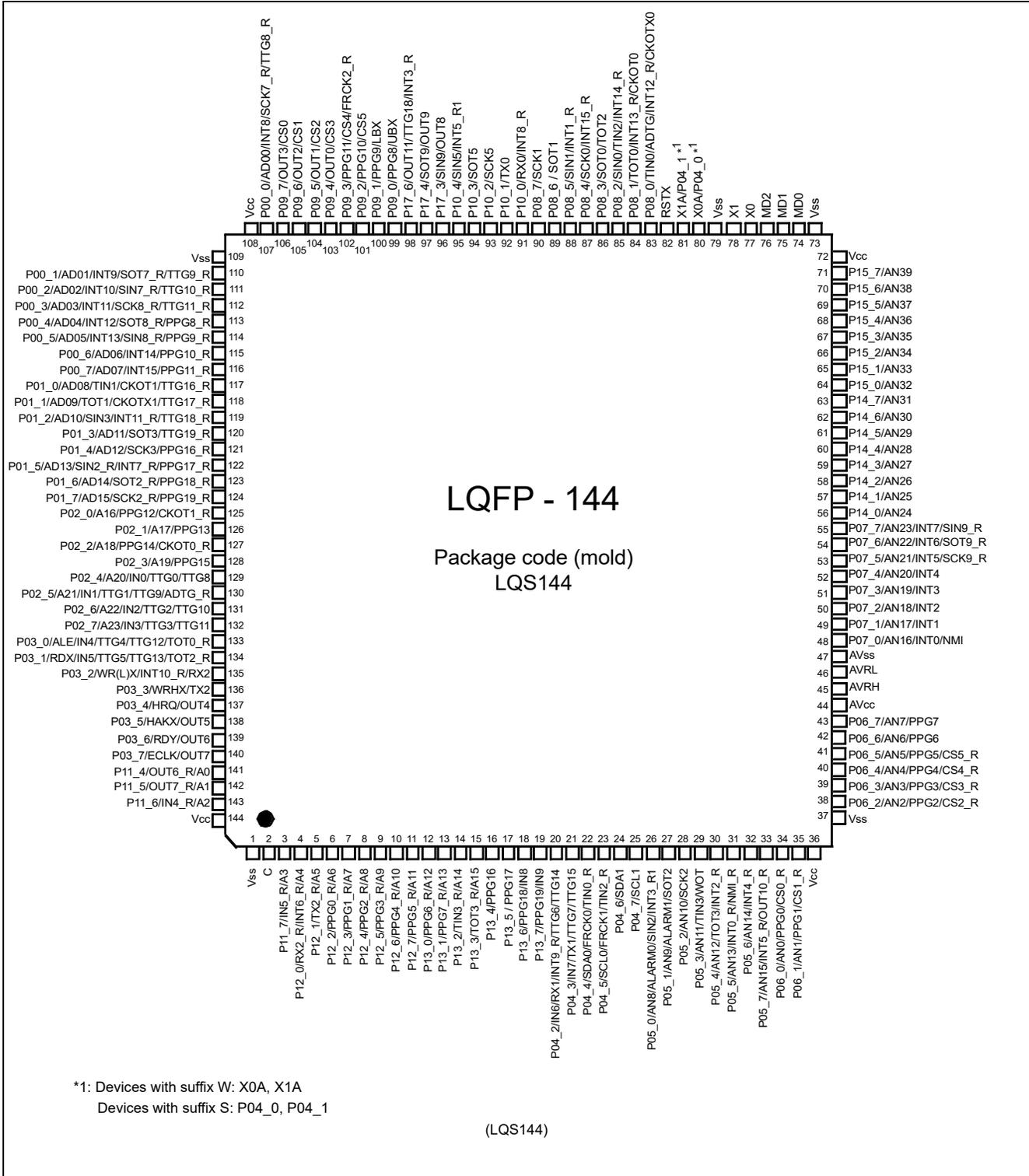
Pin assignment of CY96F33xU (LQS144) USB device

LQFP - 144

Package code (mold)
LQS144

*1: Devices with suffix W: X0A, X1A
   Devices with suffix S: P04_0, P04_1

*2: TX1, RX1, TX2, RX2, TX2_R, RX2_R not available on CY96F336U

(LQS144)
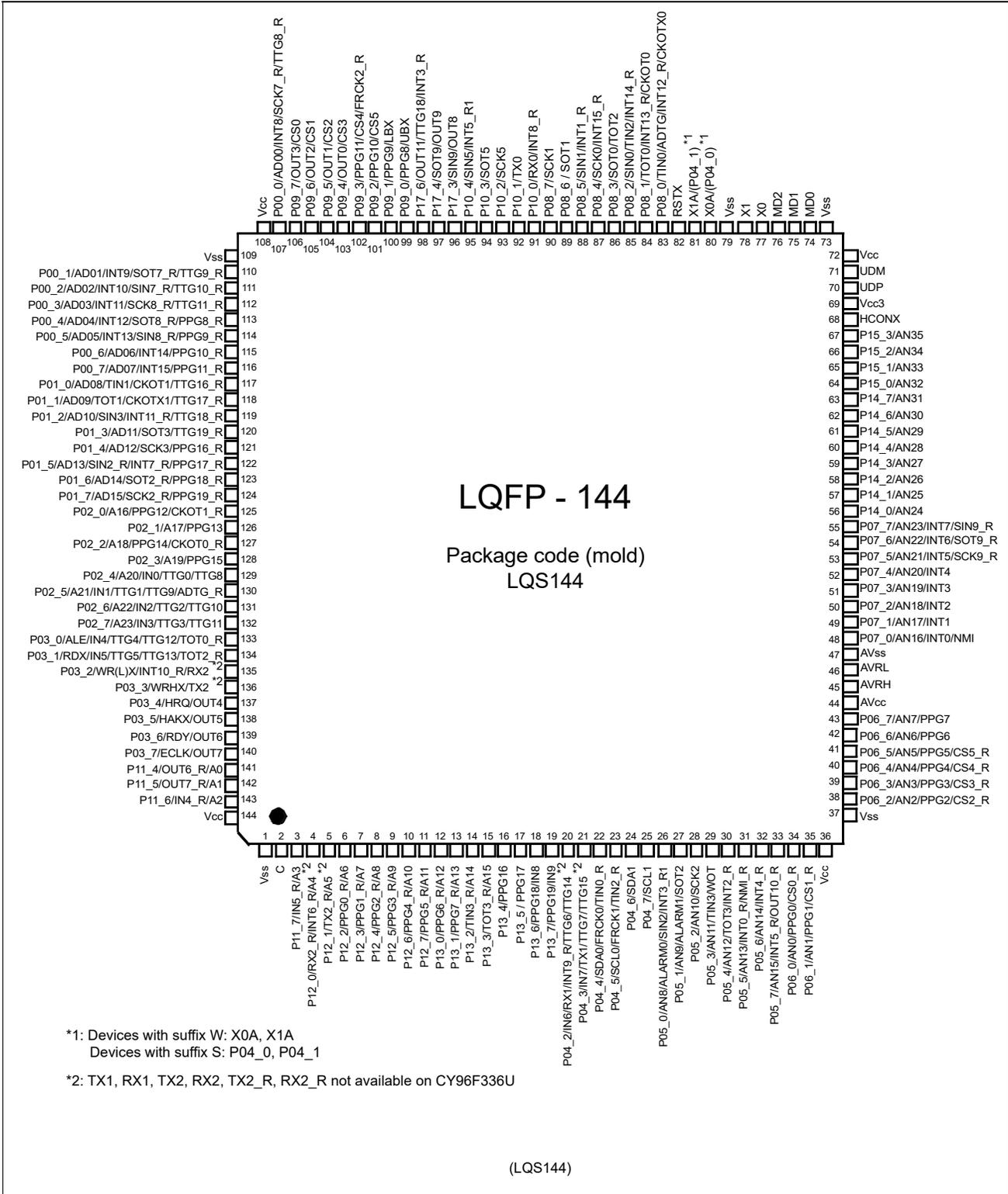
4. Pin Function Description

Pin Function description (1 of 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HCONX	USB	USB connection to host or hub
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output

Pin Function description (2 of 3)

Pin name	Feature	Description
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
RXn_R	CAN	Relocated CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I^2C	I^2C interface n clock I/O input/output
SDAn	I^2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
TXn_R	CAN	Relocated CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
UDM	USB	USB minus

Pin Function description (3 of 3)

Pin name	Feature	Description
UDP	USB	USB plus
V_{CC}	Supply	Power supply
V_{CC3}	Supply	USB Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

5. Pin Circuit Type

Pin no.	LQS144	
	Circuit type [1]	
	CY96(F)33xY/R	**CY96(F)33xU (USB device)**
1	Supply	
2	F	
3 to 21	H	
22 to 25	N	
26 to 35	I	
36, 37	Supply	
38 to 43	I	
44	Supply	
45	G	
46 to 47	Supply	
48 to 67	I	
68	I	O
69	I	Supply (3.3V)
70, 71	I	P
72, 73	Supply	
74 to 76	C	
77, 78	A	
79	Supply	
80, 81	B [2]	
80, 81	H [3]	
82	E	
83 to 107	H	
108, 109	Supply	
110 to 143	H	
144	Supply	

*1: Please refer to 6."I/O Circuit Type" for details on the I/O circuit types

*2: Devices with suffix "W"

*3: Devices without suffix "W"

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx.20MΩ (X1A: 19.5MΩ, X0A: 0.5MΩ) Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.
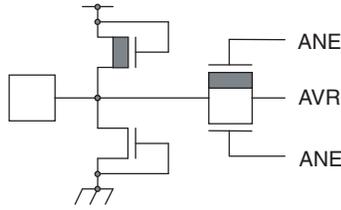
Type	Circuit	Remarks
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
O		HCONX • Available only for device with suffix "U"
P		USB IO cell: UDP and UDM • Available only for device with suffix "U"

7. Memory Map

CY96V300B

CY96(F)33x

FF:FFFF_H

Emulation ROM

USER ROM / External Bus*4

DE:0000_H

External Bus

External Bus

10:0000_H

0F:E000_H

Boot-ROM

Boot-ROM

Reserved

0E:0000_H

Reserved

External RAM

02:0000_H

Reserved

Internal RAM bank 1

RAMEND1*2
RAMSTART1*2

Internal RAM bank 1

RAM availability depending on the device

01:0000_H

Reserved

ROM/RAM MIRROR

ROM/RAM MIRROR

00:8000_H

Internal RAM bank 0

RAMSTART0*2

Internal RAM bank 0

Reserved

External Bus

External Bus end address*2

RAM-START0*3

External Bus

00:0C00_H

Peripherals

Peripherals

00:0380_H

GPR*1

GPR*1

00:0180_H

DMA

DMA

00:0100_H

External Bus

External Bus

00:00F0_H

Peripheral

Peripheral

00:0000_H

*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the 9."User ROM Memory Map For Flash Devices" on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. RAMSTART/END and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
CY96F336	24KByte	-	$00:11FF_H$	$00:2240_H$	-	-
CY96F338, CY96338	28KByte	4kB	$00:11FF_H$	$00:1240_H$	$01:8000_H$	$01:8FFF_H$

9. User ROM Memory Map For Flash Devices

Alternative mode CPU address	Flash memory mode address	CY96F336U Flash size 288kByte	CY96F338Y CY96F338R CY96F338U Flash size 544kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	S37 - 64K	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	S36 - 64K	S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$		S35 - 64K	Flash A
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		S34 - 64K	
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		S33 - 64K	
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$		S32 - 64K	
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$			
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$			
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$	External bus		
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$			
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$		External bus	
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$			
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$			
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$			
E0:FFFF$_H$ E0:0000$_H$				
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	Flash A
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K [1]	SA0 - 8K [1]	
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD[2:0] = 010)

CY96F33x		
Pin number	**USART Number**	**Normal function**
LQFP-144		
85	USART0	SIN0
86		SOT0
87		SCK0
88	USART1	SIN1
89		SOT1
90		SCK1
26	USART2	SIN2
27		SOT2
28		SCK2

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 110.
If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

11. I/O Map

I/O map CY96(F)33x (1 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000_H	I/O Port P00 - Port Data Register	PDR00		R/W
000001_H	I/O Port P01 - Port Data Register	PDR01		R/W
000002_H	I/O Port P02 - Port Data Register	PDR02		R/W
000003_H	I/O Port P03 - Port Data Register	PDR03		R/W
000004_H	I/O Port P04 - Port Data Register	PDR04		R/W
000005_H	I/O Port P05 - Port Data Register	PDR05		R/W
000006_H	I/O Port P06 - Port Data Register	PDR06		R/W
000007_H	I/O Port P07 - Port Data Register	PDR07		R/W
000008_H	I/O Port P08 - Port Data Register	PDR08		R/W
000009_H	I/O Port P09 - Port Data Register	PDR09		R/W
$00000A_H$	I/O Port P10 - Port Data Register	PDR10		R/W
$00000B_H$	I/O Port P11 - Port Data Register	PDR11		R/W
$00000C_H$	I/O Port P12 - Port Data Register	PDR12		R/W
$00000D_H$	I/O Port P13 - Port Data Register	PDR13		R/W
$00000E_H$	I/O Port P14 - Port Data Register	PDR14		R/W
$00000F_H$	I/O Port P15 - Port Data Register	PDR15		R/W
000010_H	Reserved			-
000011_H	I/O Port P17 - Port Data Register	PDR17		R/W
000012_H-000017_H	Reserved			-
000018_H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019_H	ADC0 - Control Status register High	ADCSH		R/W
$00001A_H$	ADC0 - Data Register Low	ADCRL	ADCR	R
$00001B_H$	ADC0 - Data Register High	ADCRH		R
$00001C_H$	ADC0 - Setting Register		ADSR	R/W
$00001D_H$	ADC0 - Setting Register			R/W
$00001E_H$	ADC0 - Extended Configuration Register	ADECR		R/W
$00001F_H$	Reserved			-
000020_H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021_H	FRT0 - Data register of free-running timer			R/W

I/O map CY96(F)33x (2 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000022_H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023_H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024_H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025_H	FRT1 - Data register of free-running timer			R/W
000026_H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027_H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028_H	OCU0 - Output Compare Control Status	OCS0		R/W
000029_H	OCU1 - Output Compare Control Status	OCS1		R/W
$00002A_H$	OCU0 - Compare Register		OCCP0	R/W
$00002B_H$	OCU0 - Compare Register			R/W
$00002C_H$	OCU1 - Compare Register		OCCP1	R/W
$00002D_H$	OCU1 - Compare Register			R/W
$00002E_H$	OCU2 - Output Compare Control Status	OCS2		R/W
$00002F_H$	OCU3 - Output Compare Control Status	OCS3		R/W
000030_H	OCU2 - Compare Register		OCCP2	R/W
000031_H	OCU2 - Compare Register			R/W
000032_H	OCU3 - Compare Register		OCCP3	R/W
000033_H	OCU3 - Compare Register			R/W
000034_H	OCU4 - Output Compare Control Status	OCS4		R/W
000035_H	OCU5 - Output Compare Control Status	OCS5		R/W
000036_H	OCU4 - Compare Register		OCCP4	R/W
000037_H	OCU4 - Compare Register			R/W
000038_H	OCU5 - Compare Register		OCCP5	R/W
000039_H	OCU5 - Compare Register			R/W
$00003A_H$	OCU6 - Output Compare Control Status	OCS6		R/W
$00003B_H$	OCU7 - Output Compare Control Status	OCS7		R/W
$00003C_H$	OCU6 - Compare Register		OCCP6	R/W
$00003D_H$	OCU6 - Compare Register			R/W
$00003E_H$	OCU7 - Compare Register		OCCP7	R/W
$00003F_H$	OCU7 - Compare Register			R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000040$_H$	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041$_H$	ICU0/ICU1 - Edge register	ICE01		R/W
000042$_H$	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043$_H$	ICU0 - Capture Register High	IPCPH0		R
000044$_H$	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045$_H$	ICU1 - Capture Register High	IPCPH1		R
000046$_H$	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047$_H$	ICU2/ICU3 - Edge register	ICE23		R/W
000048$_H$	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049$_H$	ICU2 - Capture Register High	IPCPH2		R
00004A$_H$	ICU3 - Capture Register Low	IPCPL3	IPCP3	R
00004B$_H$	ICU3 - Capture Register High	IPCPH3		R
00004C$_H$	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004D$_H$	ICU4/ICU5 - Edge register	ICE45		R/W
00004E$_H$	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004F$_H$	ICU4 - Capture Register High	IPCPH4		R
000050$_H$	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051$_H$	ICU5 - Capture Register High	IPCPH5		R
000052$_H$	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053$_H$	ICU6/ICU7 - Edge register	ICE67		R/W
000054$_H$	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055$_H$	ICU6 - Capture Register High	IPCPH6		R
000056$_H$	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057$_H$	ICU7 - Capture Register High	IPCPH7		R
000058$_H$	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059$_H$	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
00005A$_H$	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B$_H$	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005C$_H$	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005D$_H$	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00005E$_H$	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005F$_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060$_H$	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061$_H$	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062$_H$	RLT0 - Reload Register - for writing		TMRLR0	W
000062$_H$	RLT0 - Reload Register - for reading		TMR0	R
000063$_H$	RLT0 - Reload Register - for writing			W
000063$_H$	RLT0 - Reload Register - for reading			R
000064$_H$	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065$_H$	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066$_H$	RLT1 - Reload Register - for writing		TMRLR1	W
000066$_H$	RLT1 - Reload Register - for reading		TMR1	R
000067$_H$	RLT1 - Reload Register - for writing			W
000067$_H$	RLT1 - Reload Register - for reading			R
000068$_H$	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069$_H$	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006A$_H$	RLT2 - Reload Register - for writing		TMRLR2	W
00006A$_H$	RLT2 - Reload Register - for reading		TMR2	R
00006B$_H$	RLT2 - Reload Register - for writing			W
00006B$_H$	RLT2 - Reload Register - for reading			R
00006C$_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D$_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E$_H$	RLT3 - Reload Register - for writing		TMRLR3	W
00006E$_H$	RLT3 - Reload Register - for reading		TMR3	R
00006F$_H$	RLT3 - Reload Register - for writing			W
00006F$_H$	RLT3 - Reload Register - for reading			R
000070$_H$	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071$_H$	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074$_H$	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075$_H$	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076$_H$	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077$_H$	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078$_H$	PPG0 - Timer register		PTMR0	R
000079$_H$	PPG0 - Timer register			R
00007A$_H$	PPG0 - Period setting register		PCSR0	W
00007B$_H$	PPG0 - Period setting register			W
00007C$_H$	PPG0 - Duty cycle register		PDUT0	W
00007D$_H$	PPG0 - Duty cycle register			W
00007E$_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F$_H$	PPG0 - Control status register High	PCNH0		R/W
000080$_H$	PPG1 - Timer register		PTMR1	R
000081$_H$	PPG1 - Timer register			R
000082$_H$	PPG1 - Period setting register		PCSR1	W
000083$_H$	PPG1 - Period setting register			W
000084$_H$	PPG1 - Duty cycle register		PDUT1	W
000085$_H$	PPG1 - Duty cycle register			W
000086$_H$	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087$_H$	PPG1 - Control status register High	PCNH1		R/W
000088$_H$	PPG2 - Timer register		PTMR2	R
000089$_H$	PPG2 - Timer register			R
00008A$_H$	PPG2 - Period setting register		PCSR2	W
00008B$_H$	PPG2 - Period setting register			W
00008C$_H$	PPG2 - Duty cycle register		PDUT2	W
00008D$_H$	PPG2 - Duty cycle register			W
00008E$_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W
$0000A1_H$	PPG4 - Duty cycle register			W
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$	PPG5 - Timer register		PTMR5	R
$0000A5_H$	PPG5 - Timer register			R
$0000A6_H$	PPG5 - Period setting register		PCSR5	W
$0000A7_H$	PPG5 - Period setting register			W
$0000A8_H$	PPG5 - Duty cycle register		PDUT5	W
$0000A9_H$	PPG5 - Duty cycle register			W
$0000AA_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W
$0000AB_H$	PPG5 - Control status register High	PCNH5		R/W
$0000AC_H$	I^2C0 - Bus Status Register	IBSR0		R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000AD$_H$	I^{2}C0 - Bus Control Register	IBCR0		R/W
0000AE$_H$	I^{2}C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF$_H$	I^{2}C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0$_H$	I^{2}C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1$_H$	I^{2}C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2$_H$	I^{2}C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3$_H$	I^{2}C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4$_H$	I^{2}C0 - Data Register	IDAR0		R/W
0000B5$_H$	I^{2}C0 - Clock Control Register	ICCR0		R/W
0000B6$_H$	I^{2}C1 - Bus Status Register	IBSR1		R
0000B7$_H$	I^{2}C1 - Bus Control Register	IBCR1		R/W
0000B8$_H$	I^{2}C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9$_H$	I^{2}C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA$_H$	I^{2}C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB$_H$	I^{2}C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC$_H$	I^{2}C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD$_H$	I^{2}C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE$_H$	I^{2}C1 - Data Register	IDAR1		R/W
0000BF$_H$	I^{2}C1 - Clock Control Register	ICCR1		R/W
0000C0$_H$	USART0 - Serial Mode Register	SMR0		R/W
0000C1$_H$	USART0 - Serial Control Register	SCR0		R/W
0000C2$_H$	USART0 - TX Register	TDR0		W
0000C2$_H$	USART0 - RX Register	RDR0		R
0000C3$_H$	USART0 - Serial Status	SSR0		R/W
0000C4$_H$	USART0 - Control/Com. Register	ECCR0		R/W
0000C5$_H$	USART0 - Ext. Status Register	ESCR0		R/W
0000C6$_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
0000C7$_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W
0000C8$_H$	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9$_H$	Reserved			-

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000CA$_H$	USART1 - Serial Mode Register	SMR1		R/W
0000CB$_H$	USART1 - Serial Control Register	SCR1		R/W
0000CC$_H$	USART1 - TX Register	TDR1		W
0000CC$_H$	USART1 - RX Register	RDR1		R
0000CD$_H$	USART1 - Serial Status	SSR1		R/W
0000CE$_H$	USART1 - Control/Com. Register	ECCR1		R/W
0000CF$_H$	USART1 - Ext. Status Register	ESCR1		R/W
0000D0$_H$	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1$_H$	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2$_H$	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3$_H$	Reserved			-
0000D4$_H$	USART2 - Serial Mode Register	SMR2		R/W
0000D5$_H$	USART2 - Serial Control Register	SCR2		R/W
0000D6$_H$	USART2 - TX Register	TDR2		W
0000D6$_H$	USART2 - RX Register	RDR2		R
0000D7$_H$	USART2 - Serial Status	SSR2		R/W
0000D8$_H$	USART2 - Control/Com. Register	ECCR2		R/W
0000D9$_H$	USART2 - Ext. Status Register	ESCR2		R/W
0000DA$_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB$_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DC$_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DD$_H$	Reserved			-
0000DE$_H$	USART3 - Serial Mode Register	SMR3		R/W
0000DF$_H$	USART3 - Serial Control Register	SCR3		R/W
0000E0$_H$	USART3 - TX Register	TDR3		W
0000E0$_H$	USART3 - RX Register	RDR3		R
0000E1$_H$	USART3 - Serial Status	SSR3		R/W
0000E2$_H$	USART3 - Control/Com. Register	ECCR3		R/W
0000E3$_H$	USART3 - Ext. Status Register	ESCR3		R/W
0000E4$_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000E5$_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6$_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7$_H$-0000EF$_H$	Reserved			-
0000F0$_H$-0000FF$_H$	External Bus area	EXTBUS0		R/W
000100$_H$	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101$_H$	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102$_H$	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103$_H$	DMA0 - DMA control register	DMACS0		R/W
000104$_H$	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105$_H$	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106$_H$	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107$_H$	DMA0 - Data counter high byte	DCTH0		R/W
000108$_H$	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109$_H$	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A$_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B$_H$	DMA1 - DMA control register	DMACS1		R/W
00010C$_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010D$_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E$_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F$_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110$_H$	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111$_H$	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112$_H$	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113$_H$	DMA2 - DMA control register	DMACS2		R/W
000114$_H$	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115$_H$	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116$_H$	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117$_H$	DMA2 - Data counter high byte	DCTH2		R/W
000118$_H$	DMA3 - Buffer address pointer low byte	BAPL3		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000119$_H$	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A$_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B$_H$	DMA3 - DMA control register	DMACS3		R/W
00011C$_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D$_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E$_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F$_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120$_H$	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121$_H$	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122$_H$	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123$_H$	DMA4 - DMA control register	DMACS4		R/W
000124$_H$	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125$_H$	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126$_H$	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127$_H$	DMA4 - Data counter high byte	DCTH4		R/W
000128$_H$	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129$_H$	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012A$_H$	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012B$_H$	DMA5 - DMA control register	DMACS5		R/W
00012C$_H$	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012D$_H$	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012E$_H$	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012F$_H$	DMA5 - Data counter high byte	DCTH5		R/W
000130$_H$	DMA6 - Buffer address pointer low byte	BAPL6		R/W
000131$_H$	DMA6 - Buffer address pointer middle byte	BAPM6		R/W
000132$_H$	DMA6 - Buffer address pointer high byte	BAPH6		R/W
000133$_H$	DMA6 - DMA control register	DMACS6		R/W
000134$_H$	DMA6 - I/O register address pointer low byte	IOAL6	IOA6	R/W
000135$_H$	DMA6 - I/O register address pointer high byte	IOAH6		R/W
000136$_H$	DMA6 - Data counter low byte	DCTL6	DCT6	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000137$_H$	DMA6 - Data counter high byte	DCTH6		R/W
000138$_H$	DMA7 - Buffer address pointer low byte	BAPL7		R/W
000139$_H$	DMA7 - Buffer address pointer middle byte	BAPM7		R/W
00013A$_H$	DMA7 - Buffer address pointer high byte	BAPH7		R/W
00013B$_H$	DMA7 - DMA control register	DMACS7		R/W
00013C$_H$	DMA7 - I/O register address pointer low byte	IOAL7	IOA7	R/W
00013D$_H$	DMA7 - I/O register address pointer high byte	IOAH7		R/W
00013E$_H$	DMA7 - Data counter low byte	DCTL7	DCT7	R/W
00013F$_H$	DMA7 - Data counter high byte	DCTH7		R/W
000140$_H$	DMA8 - Buffer address pointer low byte	BAPL8		R/W
000141$_H$	DMA8 - Buffer address pointer middle byte	BAPM8		R/W
000142$_H$	DMA8 - Buffer address pointer high byte	BAPH8		R/W
000143$_H$	DMA8 - DMA control register	DMACS8		R/W
000144$_H$	DMA8 - I/O register address pointer low byte	IOAL8	IOA8	R/W
000145$_H$	DMA8 - I/O register address pointer high byte	IOAH8		R/W
000146$_H$	DMA8 - Data counter low byte	DCTL8	DCT8	R/W
000147$_H$	DMA8 - Data counter high byte	DCTH8		R/W
000148$_H$	DMA9 - Buffer address pointer low byte	BAPL9		R/W
000149$_H$	DMA9 - Buffer address pointer middle byte	BAPM9		R/W
00014A$_H$	DMA9 - Buffer address pointer high byte	BAPH9		R/W
00014B$_H$	DMA9 - DMA control register	DMACS9		R/W
00014C$_H$	DMA9 - I/O register address pointer low byte	IOAL9	IOA9	R/W
00014D$_H$	DMA9 - I/O register address pointer high byte	IOAH9		R/W
00014E$_H$	DMA9 - Data counter low byte	DCTL9	DCT9	R/W
00014F$_H$	DMA9 - Data counter high byte	DCTH9		R/W
000150$_H$-00017F$_H$	Reserved			-
000180$_H$-00037F$_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380$_H$	DMA0 - Interrupt select	DISEL0		R/W
000381$_H$	DMA1 - Interrupt select	DISEL1		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382$_H$	DMA2 - Interrupt select	DISEL2		R/W
000383$_H$	DMA3 - Interrupt select	DISEL3		R/W
000384$_H$	DMA4 - Interrupt select	DISEL4		R/W
000385$_H$	DMA5 - Interrupt select	DISEL5		R/W
000386$_H$	DMA6 - Interrupt select	DISEL6		R/W
000387$_H$	DMA7 - Interrupt select	DISEL7		R/W
000388$_H$	DMA8 - Interrupt select	DISEL8		R/W
000389$_H$	DMA9 - Interrupt select	DISEL9		R/W
00038A$_H$-00038F$_H$	Reserved			-
000390$_H$	DMA - Status register low byte	DSRL	DSR	R/W
000391$_H$	DMA - Status register high byte	DSRH		R/W
000392$_H$	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393$_H$	DMA - Stop status register high byte	DSSRH		R/W
000394$_H$	DMA - Enable register low byte	DERL	DER	R/W
000395$_H$	DMA - Enable register high byte	DERH		R/W
000396$_H$-00039F$_H$	Reserved			-
0003A0$_H$	Interrupt level register	ILR	ICR	R/W
0003A1$_H$	Interrupt index register	IDX		R/W
0003A2$_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3$_H$	Interrupt vector table base register High	TBRH		R/W
0003A4$_H$	Delayed Interrupt register	DIRR		R/W
0003A5$_H$	Non Maskable Interrupt register	NMI		R/W
0003A6$_H$-0003AB$_H$	Reserved			-
0003AC$_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD$_H$	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE$_H$	ROM mirror control register	ROMM		R/W
0003AF$_H$	EDSU configuration register	EDSU		R/W
0003B0$_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1$_H$	Memory patch control/status register ch 0/1			R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003B2$_H$	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3$_H$	Memory patch control/status register ch 2/3			R/W
0003B4$_H$	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5$_H$	Memory patch control/status register ch 4/5			R/W
0003B6$_H$	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7$_H$	Memory patch control/status register ch 6/7			R/W
0003B8$_H$	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9$_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BA$_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BB$_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BC$_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
0003BD$_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BE$_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BF$_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0$_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1$_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2$_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3$_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4$_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5$_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6$_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7$_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8$_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9$_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CA$_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CB$_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CC$_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CD$_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CE$_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CF$_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
$0003D9_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
$0003DA_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
$0003DB_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
$0003DC_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
$0003DD_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
$0003DE_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
$0003DF_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
$0003E0_H$- $0003F0_H$	Reserved			-
$0003F1_H$	Memory Control Status Register A	MCSRA		R/W
$0003F2_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
$0003F3_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
$0003F4_H$- $0003F8_H$	Reserved			-
$0003F9_H$	Flash Memory Write Control register 1	FMWC1		R/W
$0003FA_H$	Flash Memory Write Control register 2	FMWC2		R/W
$0003FB_H$	Flash Memory Write Control register 3	FMWC3		R/W
$0003FC_H$	Flash Memory Write Control register 4	FMWC4		R/W
$0003FD_H$	Flash Memory Write Control register 5	FMWC5		R/W
$0003FE_H$- $0003FF_H$	Reserved			-
000400_H	Standby Mode control register	SMCR		R/W
000401_H	Clock select register	CKSR		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000402$_H$	Clock Stabilization select register	CKSSR		R/W
000403$_H$	Clock monitor register	CKMR		R
000404$_H$	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405$_H$	Clock Frequency control register High	CKFCRH		R/W
000406$_H$	PLL Control register Low	PLLCRL	PLLCR	R/W
000407$_H$	PLL Control register High	PLLCRH		R/W
000408$_H$	RC clock timer control register	RCTCR		R/W
000409$_H$	Main clock timer control register	MCTCR		R/W
00040A$_H$	Sub clock timer control register	SCTCR		R/W
00040B$_H$	Reset cause and clock status register with clear function	RCCSRC		R
00040C$_H$	Reset configuration register	RCR		R/W
00040D$_H$	Reset cause and clock status register	RCCSR		R
00040E$_H$	Watch dog timer configuration register	WDTC		R/W
00040F$_H$	Watch dog timer clear pattern register	WDTCP		W
000410$_H$-000414$_H$	Reserved			-
000415$_H$	Clock output activation register	COAR		R/W
000416$_H$	Clock output configuration register 0	COCR0		R/W
000417$_H$	Clock output configuration register 1	COCR1		R/W
000418$_H$	Clock Modulator control register	CMCR		R/W
000419$_H$	Reserved			-
00041A$_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B$_H$	Clock Modulator Parameter register High	CMPRH		R/W
00041C$_H$-00042B$_H$	Reserved			-
00042C$_H$	Voltage Regulator Control register	VRCR		R/W
00042D$_H$	Clock Input and LVD Control Register	CILCR		R/W
00042E$_H$-00042F$_H$	Reserved			-
000430$_H$	I/O Port P00 - Data Direction Register	DDR00		R/W
000431$_H$	I/O Port P01 - Data Direction Register	DDR01		R/W
000432$_H$	I/O Port P02 - Data Direction Register	DDR02		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000433$_H$	I/O Port P03 - Data Direction Register	DDR03		R/W
000434$_H$	I/O Port P04 - Data Direction Register	DDR04		R/W
000435$_H$	I/O Port P05 - Data Direction Register	DDR05		R/W
000436$_H$	I/O Port P06 - Data Direction Register	DDR06		R/W
000437$_H$	I/O Port P07 - Data Direction Register	DDR07		R/W
000438$_H$	I/O Port P08 - Data Direction Register	DDR08		R/W
000439$_H$	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A$_H$	I/O Port P10 - Data Direction Register	DDR10		R/W
00043B$_H$	I/O Port P11 - Data Direction Register	DDR11		R/W
00043C$_H$	I/O Port P12 - Data Direction Register	DDR12		R/W
00043D$_H$	I/O Port P13 - Data Direction Register	DDR13		R/W
00043E$_H$	I/O Port P14 - Data Direction Register	DDR14		R/W
00043F$_H$	I/O Port P15 - Data Direction Register	DDR15		R/W
000440$_H$	Reserved			-
000441$_H$	I/O Port P17 - Data Direction Register	DDR17		R/W
000442$_H$-000443$_H$	Reserved			-
000444$_H$	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445$_H$	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446$_H$	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447$_H$	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448$_H$	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449$_H$	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A$_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B$_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044C$_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
00044D$_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
00044E$_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
00044F$_H$	I/O Port P11 - Port Input Enable Register	PIER11		R/W
000450$_H$	I/O Port P12 - Port Input Enable Register	PIER12		R/W
000451$_H$	I/O Port P13 - Port Input Enable Register	PIER13		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000452$_H$	I/O Port P14 - Port Input Enable Register	PIER14		R/W
000453$_H$	I/O Port P15 - Port Input Enable Register	PIER15		R/W
000454$_H$	Reserved			-
000455$_H$	I/O Port P17 - Port Input Enable Register	PIER17		R/W
000456$_H$-000457$_H$	Reserved			-
000458$_H$	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459$_H$	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A$_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B$_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C$_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D$_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E$_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F$_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460$_H$	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461$_H$	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462$_H$	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463$_H$	I/O Port P11 - Port Input Level Register	PILR11		R/W
000464$_H$	I/O Port P12 - Port Input Level Register	PILR12		R/W
000465$_H$	I/O Port P13 - Port Input Level Register	PILR13		R/W
000466$_H$	I/O Port P14 - Port Input Level Register	PILR14		R/W
000467$_H$	I/O Port P15 - Port Input Level Register	PILR15		R/W
000468$_H$	Reserved			-
000469$_H$	I/O Port P17 - Port Input Level Register	PILR17		R/W
00046A$_H$-00046B$_H$	Reserved			-
00046C$_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D$_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E$_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F$_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470$_H$	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000471$_H$	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472$_H$	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473$_H$	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474$_H$	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475$_H$	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476$_H$	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477$_H$	I/O Port P11 - Extended Port Input Level Register	EPILR11		R/W
000478$_H$	I/O Port P12 - Extended Port Input Level Register	EPILR12		R/W
000479$_H$	I/O Port P13 - Extended Port Input Level Register	EPILR13		R/W
00047A$_H$	I/O Port P14 - Extended Port Input Level Register	EPILR14		R/W
00047B$_H$	I/O Port P15 - Extended Port Input Level Register	EPILR15		R/W
00047C$_H$	Reserved			-
00047D$_H$	I/O Port P17 - Extended Port Input Level Register	EPILR17		R/W
00047E$_H$-00047F$_H$	Reserved			-
000480$_H$	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481$_H$	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482$_H$	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483$_H$	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484$_H$	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485$_H$	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486$_H$	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487$_H$	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488$_H$	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489$_H$	I/O Port P09 - Port Output Drive Register	PODR09		R/W
00048A$_H$	I/O Port P10 - Port Output Drive Register	PODR10		R/W
00048B$_H$	I/O Port P11 - Port Output Drive Register	PODR11		R/W
00048C$_H$	I/O Port P12 - Port Output Drive Register	PODR12		R/W
00048D$_H$	I/O Port P13 - Port Output Drive Register	PODR13		R/W
00048E$_H$	I/O Port P14 - Port Output Drive Register	PODR14		R/W
00048F$_H$	I/O Port P15 - Port Output Drive Register	PODR15		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000490$_H$	Reserved			-
000491$_H$	I/O Port P17 - Port Output Drive Register	PODR17		R/W
000492$_H$-00049B$_H$	Reserved			-
00049C$_H$	I/O Port P08 - Port High Drive Register	PHDR08		R/W
00049D$_H$	I/O Port P09 - Port High Drive Register	PHDR09		R/W
00049E$_H$	I/O Port P10 - Port High Drive Register	PHDR10		R/W
00049F$_H$-0004A7$_H$	Reserved			-
0004A8$_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9$_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AA$_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004AB$_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004AC$_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004AD$_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AE$_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AF$_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0$_H$	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
0004B1$_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
0004B2$_H$	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
0004B3$_H$	I/O Port P11 - Pull-Up resistor Control Register	PUCR11		R/W
0004B4$_H$	I/O Port P12 - Pull-Up resistor Control Register	PUCR12		R/W
0004B5$_H$	I/O Port P13 - Pull-Up resistor Control Register	PUCR13		R/W
0004B6$_H$	I/O Port P14 - Pull-Up resistor Control Register	PUCR14		R/W
0004B7$_H$	I/O Port P15 - Pull-Up resistor Control Register	PUCR15		R/W
0004B8$_H$	Reserved			-
0004B9$_H$	I/O Port P17 - Pull-Up resistor Control Register	PUCR17		R/W
0004BA$_H$-0004BB$_H$	Reserved			-
0004BC$_H$	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD$_H$	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE$_H$	I/O Port P02 - External Pin State Register	EPSR02		R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004BF$_H$	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0$_H$	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1$_H$	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2$_H$	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3$_H$	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4$_H$	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5$_H$	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6$_H$	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7$_H$	I/O Port P11 - External Pin State Register	EPSR11		R
0004C8$_H$	I/O Port P12 - External Pin State Register	EPSR12		R
0004C9$_H$	I/O Port P13 - External Pin State Register	EPSR13		R
0004CA$_H$	I/O Port P14 - External Pin State Register	EPSR14		R
0004CB$_H$	I/O Port P15 - External Pin State Register	EPSR15		R
0004CC$_H$	Reserved			-
0004CD$_H$	I/O Port P17 - External Pin State Register	EPSR17		R
0004CE$_H$-0004CF$_H$	Reserved			-
0004D0$_H$	ADC analog input enable register 0	ADER0		R/W
0004D1$_H$	ADC analog input enable register 1	ADER1		R/W
0004D2$_H$	ADC analog input enable register 2	ADER2		R/W
0004D3$_H$	ADC analog input enable register 3	ADER3		R/W
0004D4$_H$	ADC analog input enable register 4	ADER4		R/W
0004D5$_H$	Reserved			-
0004D6$_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7$_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8$_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9$_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA$_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB$_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC$_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD$_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004DE$_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF$_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0$_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1$_H$	RTC - Sub Second Register M	WTBRH0		R/W
0004E2$_H$	RTC - Sub-Second Register H	WTBR1		R/W
0004E3$_H$	RTC - Second Register	WTSR		R/W
0004E4$_H$	RTC - Minutes	WTMR		R/W
0004E5$_H$	RTC - Hour	WTHR		R/W
0004E6$_H$	RTC - Timer Control Extended Register	WTCER		R/W
0004E7$_H$	RTC - Clock select register	WTCKSR		R/W
0004E8$_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9$_H$	RTC - Timer Control Register High	WTCRH		R/W
0004EA$_H$	CAL - Calibration unit Control register	CUCR		R/W
0004EB$_H$	Reserved			-
0004EC$_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED$_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE$_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF$_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0$_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1$_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2$_H$-0004F9$_H$	Reserved			-
0004FA$_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB$_H$-0004FF$_H$	Reserved			-
000500$_H$	FRT2 - Data register of free-running timer		TCDT2	R/W
000501$_H$	FRT2 - Data register of free-running timer			R/W
000502$_H$	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503$_H$	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504$_H$	FRT3 - Data register of free-running timer		TCDT3	R/W
000505$_H$	FRT3 - Data register of free-running timer			R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000506$_H$	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507$_H$	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508$_H$	OCU8 - Output Compare Control Status	OCS8		R/W
000509$_H$	OCU9 - Output Compare Control Status	OCS9		R/W
00050A$_H$	OCU8 - Compare Register		OCCP8	R/W
00050B$_H$	OCU8 - Compare Register			R/W
00050C$_H$	OCU9 - Compare Register		OCCP9	R/W
00050D$_H$	OCU9 - Compare Register			R/W
00050E$_H$	OCU10 - Output Compare Control Status	OCS10		R/W
00050F$_H$	OCU11 - Output Compare Control Status	OCS11		R/W
000510$_H$	OCU10 - Compare Register		OCCP10	R/W
000511$_H$	OCU10 - Compare Register			R/W
000512$_H$	OCU11 - Compare Register		OCCP11	R/W
000513$_H$	OCU11 - Compare Register			R/W
000514$_H$	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515$_H$	ICU8/ICU9 - Edge Register	ICE89		R/W
000516$_H$	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517$_H$	ICU8 - Capture Register High	IPCPH8		R
000518$_H$	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519$_H$	ICU9 - Capture Register High	IPCPH9		R
00051A$_H$-000529$_H$	Reserved			-
00052A$_H$	USART5 - Serial Mode Register	SMR5		R/W
00052B$_H$	USART5 - Serial Control Register	SCR5		R/W
00052C$_H$	USART5 - RX Register	TDR5		W
00052C$_H$	USART5 - TX Register	RDR5		R
00052D$_H$	USART5 - Serial Status	SSR5		R/W
00052E$_H$	USART5 - Control/Com. Register	ECCR5		R/W
00052F$_H$	USART5 - Ext. Status Register	ESCR5		R/W
000530$_H$	USART5 - Baud Rate Generator Register Low	BGRL5	BGR5	R/W
000531$_H$	USART5 - Baud Rate Generator Register High	BGRH5		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000532$_H$	USART5 - Extended Serial Interrupt Register	ESIR5		R/W
000533$_H$-00053D$_H$	Reserved			-
00053E$_H$	USART7 - Serial Mode Register	SMR7		R/W
00053F$_H$	USART7 - Serial Control Register	SCR7		R/W
000540$_H$	USART7 - Serial TX Register	TDR7		W
000540$_H$	USART7 - Serial RX Register	RDR7		R
000541$_H$	USART7 - Serial Status Register	SSR7		R/W
000542$_H$	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543$_H$	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544$_H$	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545$_H$	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546$_H$	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547$_H$	Reserved			-
000548$_H$	USART8 - Serial Mode Register	SMR8		R/W
000549$_H$	USART8 - Serial Control Register	SCR8		R/W
00054A$_H$	USART8 - Serial TX Register	TDR8		W
00054A$_H$	USART8 - Serial RX Register	RDR8		R
00054B$_H$	USART8 - Serial Status Register	SSR8		R/W
00054C$_H$	USART8 - Ext. Control/Com. Register	ECCR8		R/W
00054D$_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054E$_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054F$_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550$_H$	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551$_H$	Reserved			-
000552$_H$	USART9 - Serial Mode Register	SMR9		R/W
000553$_H$	USART9 - Serial Control Register	SCR9		R/W
000554$_H$	USART9 - Serial TX Register	TDR9		W
000554$_H$	USART9 - Serial RX Register	RDR9		R
000555$_H$	USART9 - Serial Status Register	SSR9		R/W
000556$_H$	USART9 - Ext. Control/Com. Register	ECCR9		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000557$_H$	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558$_H$	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559$_H$	USART9 - Baud Rate Generator Register High	BGRH9		R/W
00055A$_H$	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
00055B$_H$-00055F$_H$	Reserved			-
000560$_H$	ALARM0 - Control Status Register	ACSR0		R/W
000561$_H$	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562$_H$	ALARM1 - Control Status Register	ACSR1		R/W
000563$_H$	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564$_H$	PPG6 - Timer register		PTMR6	R
000565$_H$	PPG6 - Timer register			R
000566$_H$	PPG6 - Period setting register		PCSR6	W
000567$_H$	PPG6 - Period setting register			W
000568$_H$	PPG6 - Duty cycle register		PDUT6	W
000569$_H$	PPG6 - Duty cycle register			W
00056A$_H$	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056B$_H$	PPG6 - Control status register High	PCNH6		R/W
00056C$_H$	PPG7 - Timer register		PTMR7	R
00056D$_H$	PPG7 - Timer register			R
00056E$_H$	PPG7 - Period setting register		PCSR7	W
00056F$_H$	PPG7 - Period setting register			W
000570$_H$	PPG7 - Duty cycle register		PDUT7	W
000571$_H$	PPG7 - Duty cycle register			W
000572$_H$	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573$_H$	PPG7 - Control status register High	PCNH7		R/W
000574$_H$	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575$_H$	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576$_H$	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577$_H$	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578$_H$	PPG8 - Timer register		PTMR8	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000579_H	PPG8 - Timer register			R
$00057A_H$	PPG8 - Period setting register		PCSR8	W
$00057B_H$	PPG8 - Period setting register			W
$00057C_H$	PPG8 - Duty cycle register		PDUT8	W
$00057D_H$	PPG8 - Duty cycle register			W
$00057E_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
$00057F_H$	PPG8 - Control status register High	PCNH8		R/W
000580_H	PPG9 - Timer register		PTMR9	R
000581_H	PPG9 - Timer register			R
000582_H	PPG9 - Period setting register		PCSR9	W
000583_H	PPG9 - Period setting register			W
000584_H	PPG9 - Duty cycle register		PDUT9	W
000585_H	PPG9 - Duty cycle register			W
000586_H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587_H	PPG9 - Control status register High	PCNH9		R/W
000588_H	PPG10 - Timer register		PTMR10	R
000589_H	PPG10 - Timer register			R
$00058A_H$	PPG10 - Period setting register		PCSR10	W
$00058B_H$	PPG10 - Period setting register			W
$00058C_H$	PPG10 - Duty cycle register		PDUT10	W
$00058D_H$	PPG10 - Duty cycle register			W
$00058E_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
$00058F_H$	PPG10 - Control status register High	PCNH10		R/W
000590_H	PPG11 - Timer register		PTMR11	R
000591_H	PPG11 - Timer register			R
000592_H	PPG11 - Period setting register		PCSR11	W
000593_H	PPG11 - Period setting register			W
000594_H	PPG11 - Duty cycle register		PDUT11	W
000595_H	PPG11 - Duty cycle register			W
000596_H	PPG11 - Control status register Low	PCNL11	PCN11	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W
0005A9$_H$	PPG13 - Duty cycle register			W
0005AA$_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB$_H$	PPG13 - Control status register High	PCNH13		R/W
0005AC$_H$	PPG14 - Timer register		PTMR14	R
0005AD$_H$	PPG14 - Timer register			R
0005AE$_H$	PPG14 - Period setting register		PCSR14	W
0005AF$_H$	PPG14 - Period setting register			W
0005B0$_H$	PPG14 - Duty cycle register		PDUT14	W
0005B1$_H$	PPG14 - Duty cycle register			W
0005B2$_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3$_H$	PPG14 - Control status register High	PCNH14		R/W
0005B4$_H$	PPG15 - Timer register		PTMR15	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005B5$_H$	PPG15 - Timer register			R
0005B6$_H$	PPG15 - Period setting register		PCSR15	W
0005B7$_H$	PPG15 - Period setting register			W
0005B8$_H$	PPG15 - Duty cycle register		PDUT15	W
0005B9$_H$	PPG15 - Duty cycle register			W
0005BA$_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
0005BB$_H$	PPG15 - Control status register High	PCNH15		R/W
0005BC$_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
0005BD$_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
0005BE$_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
0005BF$_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
0005C0$_H$	PPG16 - Timer register		PTMR16	R
0005C1$_H$	PPG16 - Timer register			R
0005C2$_H$	PPG16 - Period setting register		PCSR16	W
0005C3$_H$	PPG16 - Period setting register			W
0005C4$_H$	PPG16 - Duty cycle register		PDUT16	W
0005C5$_H$	PPG16 - Duty cycle register			W
0005C6$_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
0005C7$_H$	PPG16 - Control status register High	PCNH16		R/W
0005C8$_H$	PPG17 - Timer register		PTMR17	R
0005C9$_H$	PPG17 - Timer register			R
0005CA$_H$	PPG17 - Period setting register		PCSR17	W
0005CB$_H$	PPG17 - Period setting register			W
0005CC$_H$	PPG17 - Duty cycle register		PDUT17	W
0005CD$_H$	PPG17 - Duty cycle register			W
0005CE$_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF$_H$	PPG17 - Control status register High	PCNH17		R/W
0005D0$_H$	PPG18 - Timer register		PTMR18	R
0005D1$_H$	PPG18 - Timer register			R
0005D2$_H$	PPG18 - Period setting register		PCSR18	W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005D3$_H$	PPG18 - Period setting register			W
0005D4$_H$	PPG18 - Duty cycle register		PDUT18	W
0005D5$_H$	PPG18 - Duty cycle register			W
0005D6$_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7$_H$	PPG18 - Control status register High	PCNH18		R/W
0005D8$_H$	PPG19 - Timer register		PTMR19	R
0005D9$_H$	PPG19 - Timer register			R
0005DA$_H$	PPG19 - Period setting register		PCSR19	W
0005DB$_H$	PPG19 - Period setting register			W
0005DC$_H$	PPG19 - Duty cycle register		PDUT19	W
0005DD$_H$	PPG19 - Duty cycle register			W
0005DE$_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF$_H$	PPG19 - Control status register High	PCNH19		R/W
0005E0$_H$-00065F$_H$	Reserved			-
000660$_H$	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661$_H$	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662$_H$	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663$_H$	Peripheral Resource Relocation Register 13	PRRR13		W
000664$_H$-00069F$_H$	Reserved			-
0006A0$_H$	USB - Host Control register Low	HCNTL0	HCNT0	R/W
0006A1$_H$	USB - Host Control register High	HCNTH0		R/W
0006A2$_H$	USB - Host Interrupt Register	HIRQ0		R/W
0006A3$_H$	USB - Host Error Status Register	HERR0		R/W
0006A4$_H$	USB - Host State Status Register	HSTATE0		R/W
0006A5$_H$	USB - Host SOF Int. Frame Compare Register	HFCOMP0		R/W
0006A6$_H$	USB - Host Retry Timer Setting Register Low	HRTIMERL0		R/W
0006A7$_H$	USB - Host Retry Timer Setting Register Middle	HRTIMERM0		R/W
0006A8$_H$	USB - Host Retry Timer Setting Register High	HRTIMERH0		R/W
0006A9$_H$	USB - Host Address Register	HADR0		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006AA$_H$	USB - Host EOF Setting Register Low	HEOFL0	HEOF0	R/W
0006AB$_H$	USB - Host EOF Setting Register High	HEOFH0		R/W
0006AC$_H$	USB - Host Frame Register Low	HFRAMEL0	HFRAME0	R/W
0006AD$_H$	USB - Host Frame Register High	HFRAMEH0		R/W
0006AE$_H$	USB - Host Token End Point Register	HTOKEN0		R/W
0006AF$_H$	Reserved			-
0006B0$_H$	USB - UDC Control Register	UDCC0		R/W
0006B1$_H$	Reserved			-
0006B2$_H$	USB - EP0 Control Register Low	EP0CL0	EP0C0	R/W
0006B3$_H$	USB - EP0 Control Register High	EP0CH0		R/W
0006B4$_H$	USB - EP1 Control Register Low	EP1CL0	EP1C0	R/W
0006B5$_H$	USB - EP1 Control Register High - non public	EP1CH0		R/W
0006B6$_H$	USB - EP2 Control Register Low	EP2CL0	EP2C0	R/W
0006B7$_H$	USB - EP2 Control Register High	EP2CH0		R/W
0006B8$_H$	USB - EP3 Control Register Low	EP3CL0	EP3C0	R/W
0006B9$_H$	USB - EP3 Control Register High	EP3CH0		R/W
0006BA$_H$	USB - EP4 Control Register Low	EP4CL0	EP4C0	R/W
0006BB$_H$	USB - EP4 Control Register High	EP4CH0		R/W
0006BC$_H$	USB - EP5 Control Register Low	EP5CL0	EP5C0	R/W
0006BD$_H$	USB - EP5 Control Register High	EP5CH0		R/W
0006BE$_H$	USB - Timer Stamp Register Low	TMSPL0	TMSP0	R/W
0006BF$_H$	USB - Timer Stamp Register High	TMSPH0		R/W
0006C0$_H$	USB - UDC Status Register	UDCS0		R/W
0006C1$_H$	USB - UDC Interrupt Enable Register	UDCIE0		R/W
0006C2$_H$	USB - EP0I Status Register Low	EP0ISL0	EP0IS0	W
0006C3$_H$	USB - EP0I Status Register High	EP0ISH0		R/W
0006C4$_H$	USB - EP0O Status Register Low	EP0OSL0	EP0OS0	R/W
0006C5$_H$	USB - EP0O Status Register High	EP0OSH0		R/W
0006C6$_H$	USB - EP1 Status Register Low	EP1SL0	EP1S0	R/W
0006C7$_H$	USB - EP1 Status Register High	EP1SH0		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006C8$_H$	USB - EP2 Status Register Low	EP2SL0	EP2S0	R/W
0006C9$_H$	USB - EP2 Status Register High	EP2SH0		R/W
0006CA$_H$	USB - EP3 Status Register Low	EP3SL0	EP3S0	R/W
0006CB$_H$	USB - EP3 Status Register High	EP3SH0		R/W
0006CC$_H$	USB - EP4 Status Register Low	EP4SL0	EP4S0	R/W
0006CD$_H$	USB - EP4 Status Register High	EP4SH0		R/W
0006CE$_H$	USB - EP5 Status Register Low	EP5SL0	EP5S0	R/W
0006CF$_H$	USB - EP5 Status Register High	EP5SH0		R/W
0006D0$_H$	USB - EP0 Data register Low	EP0DTL0	EP0DT0	R/W
0006D1$_H$	USB - EP0 Data register High	EP0DTH0		R/W
0006D2$_H$	USB - EP1 Data register Low	EP1DTL0	EP1DT0	R/W
0006D3$_H$	USB - EP1 Data register High	EP1DTH0		R/W
0006D4$_H$	USB - EP2 Data register Low	EP2DTL0	EP2DT0	R/W
0006D5$_H$	USB - EP2 Data register High	EP2DTH0		R/W
0006D6$_H$	USB - EP3 Data register Low	EP3DTL0	EP3DT0	R/W
0006D7$_H$	USB - EP3 Data register High	EP3DTH0		R/W
0006D8$_H$	USB - EP4 Data register Low	EP4DTL0	EP4DT0	R/W
0006D9$_H$	USB - EP4 Data register High	EP4DTH0		R/W
0006DA$_H$	USB - EP5 Data register Low	EP5DTL0	EP5DT0	R/W
0006DB$_H$	USB - EP5 Data register High	EP5DTH0		R/W
0006DC$_H$- 0006DF$_H$	Reserved			-
0006E0$_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
0006E1$_H$	External Bus - Area configuration register 0 High	EACH0		R/W
0006E2$_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3$_H$	External Bus - Area configuration register 1 High	EACH1		R/W
0006E4$_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5$_H$	External Bus - Area configuration register 2 High	EACH2		R/W
0006E6$_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7$_H$	External Bus - Area configuration register 3 High	EACH3		R/W
0006E8$_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006E9$_H$	External Bus - Area configuration register 4 High	EACH4		R/W
0006EA$_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EB$_H$	External Bus - Area configuration register 5 High	EACH5		R/W
0006EC$_H$	External Bus - Area select register 2	EAS2		R/W
0006ED$_H$	External Bus - Area select register 3	EAS3		R/W
0006EE$_H$	External Bus - Area select register 4	EAS4		R/W
0006EF$_H$	External Bus - Area select register 5	EAS5		R/W
0006F0$_H$	External Bus - Mode register	EBM		R/W
0006F1$_H$	External Bus - Clock and Function register	EBCF		R/W
0006F2$_H$	External Bus - Address output enable register 0	EBAE0		R/W
0006F3$_H$	External Bus - Address output enable register 1	EBAE1		R/W
0006F4$_H$	External Bus - Address output enable register 2	EBAE2		R/W
0006F5$_H$	External Bus - Control signal register	EBCS		R/W
0006F6$_H$-0006FF$_H$	Reserved			-
000700$_H$	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701$_H$	CAN0 - Control register High (reserved)	CTRLRH0		R
000702$_H$	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703$_H$	CAN0 - Status register High (reserved)	STATRH0		R
000704$_H$	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705$_H$	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706$_H$	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707$_H$	CAN0 - Bit Timing Register High	BTRH0		R/W
000708$_H$	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709$_H$	CAN0 - Interrupt Register High	INTRH0		R
00070A$_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B$_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C$_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D$_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E$_H$-00070F$_H$	Reserved			-

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000710_H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711_H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712_H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713_H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714_H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000747$_H$	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748$_H$	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749$_H$	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074A$_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074B$_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074C$_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074D$_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
00074E$_H$	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
00074F$_H$	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750$_H$	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751$_H$	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752$_H$	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753$_H$	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754$_H$	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755$_H$	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756$_H$-00077F$_H$	Reserved			-
000780$_H$	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781$_H$	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782$_H$	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783$_H$	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784$_H$-00078F$_H$	Reserved			-
000790$_H$	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791$_H$	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792$_H$	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793$_H$	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794$_H$-00079F$_H$	Reserved			-
0007A0$_H$	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1$_H$	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2$_H$	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0007A3_H$	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
$0007A4_H$- $0007AF_H$	Reserved			-
$0007B0_H$	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
$0007B1_H$	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
$0007B2_H$	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
$0007B3_H$	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
$0007B4_H$- $0007CD_H$	Reserved			-
$0007CE_H$	CAN0 - Output enable register	COER0		R/W
$0007CF_H$- $0007FF_H$	Reserved			-
000800_H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$- $00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000814$_H$	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815$_H$	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816$_H$	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817$_H$	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818$_H$	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819$_H$	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A$_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B$_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C$_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D$_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E$_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F$_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820$_H$	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821$_H$	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822$_H$	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823$_H$	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824$_H$	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825$_H$	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826$_H$-00083F$_H$	Reserved			-
000840$_H$	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841$_H$	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842$_H$	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843$_H$	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844$_H$	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845$_H$	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846$_H$	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847$_H$	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848$_H$	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849$_H$	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084A$_H$	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00084B$_H$	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084C$_H$	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084D$_H$	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084E$_H$	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084F$_H$	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850$_H$	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851$_H$	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852$_H$	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853$_H$	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854$_H$	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855$_H$	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856$_H$-00087F$_H$	Reserved			-
000880$_H$	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881$_H$	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882$_H$	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883$_H$	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884$_H$-00088F$_H$	Reserved			-
000890$_H$	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891$_H$	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892$_H$	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893$_H$	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894$_H$-00089F$_H$	Reserved			-
0008A0$_H$	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1$_H$	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2$_H$	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3$_H$	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4$_H$-0008AF$_H$	Reserved			-
0008B0$_H$	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0008B1$_H$	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2$_H$	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3$_H$	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4$_H$-0008CD$_H$	Reserved			-
0008CE$_H$	CAN1 - Output enable register	COER1		R/W
0008CF$_H$-0008FF$_H$	Reserved			-
000900$_H$	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901$_H$	CAN2 - Control register High (reserved)	CTRLRH2		R
000902$_H$	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903$_H$	CAN2 - Status register High (reserved)	STATRH2		R
000904$_H$	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905$_H$	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906$_H$	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907$_H$	CAN2 - Bit Timing Register High	BTRH2		R/W
000908$_H$	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909$_H$	CAN2 - Interrupt Register High	INTRH2		R
00090A$_H$	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090B$_H$	CAN2 - Test Register High (reserved)	TESTRH2		R
00090C$_H$	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090D$_H$	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090E$_H$-00090F$_H$	Reserved			-
000910$_H$	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911$_H$	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912$_H$	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913$_H$	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914$_H$	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915$_H$	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916$_H$	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917$_H$	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000918$_H$	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919$_H$	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
00091A$_H$	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
00091B$_H$	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
00091C$_H$	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
00091D$_H$	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
00091E$_H$	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W
00091F$_H$	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920$_H$	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921$_H$	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922$_H$	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923$_H$	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924$_H$	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925$_H$	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W
000926$_H$-00093F$_H$	Reserved			-
000940$_H$	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	R/W
000941$_H$	CAN2 - IF2 Command request register High	IF2CREQH2		R/W
000942$_H$	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	R/W
000943$_H$	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944$_H$	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	R/W
000945$_H$	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		R/W
000946$_H$	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	R/W
000947$_H$	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		R/W
000948$_H$	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	R/W
000949$_H$	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		R/W
00094A$_H$	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	R/W
00094B$_H$	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		R/W
00094C$_H$	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	R/W
00094D$_H$	CAN2 - IF2 Message Control Register High	IF2MCTRH2		R/W
00094E$_H$	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00094F$_H$	CAN2 - IF2 Data A1 High	IF2DTA1H2		R/W
000950$_H$	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	R/W
000951$_H$	CAN2 - IF2 Data A2 High	IF2DTA2H2		R/W
000952$_H$	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	R/W
000953$_H$	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954$_H$	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W
000955$_H$	CAN2 - IF2 Data B2 High	IF2DTB2H2		R/W
000956$_H$-00097F$_H$	Reserved			-
000980$_H$	CAN2 - Transmission Request 1 Register Low	TREQR1L2	TREQR12	R
000981$_H$	CAN2 - Transmission Request 1 Register High	TREQR1H2		R
000982$_H$	CAN2 - Transmission Request 2 Register Low	TREQR2L2	TREQR22	R
000983$_H$	CAN2 - Transmission Request 2 Register High	TREQR2H2		R
000984$_H$-00098F$_H$	Reserved			-
000990$_H$	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991$_H$	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992$_H$	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993$_H$	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994$_H$-00099F$_H$	Reserved			-
0009A0$_H$	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
0009A1$_H$	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
0009A2$_H$	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
0009A3$_H$	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
0009A4$_H$-0009AF$_H$	Reserved			-
0009B0$_H$	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R
0009B1$_H$	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
0009B2$_H$	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
0009B3$_H$	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0009B4_H$-$0009CD_H$	Reserved			-
$0009CE_H$	CAN2 - Output enable register	COER2		R/W
$0009CF_H$-$000BFF_H$	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

12. Interrupt Vector Table

Interrupt vector table CY96(F)33x (1 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	PLL_UNLOCK	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9

Interrupt vector table CY96(F)33x (2 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
27	390$_H$	EXTINT10	Yes	27	External Interrupt 10
28	38C$_H$	EXTINT11	Yes	28	External Interrupt 11
29	388$_H$	EXTINT12	Yes	29	External Interrupt 12
30	384$_H$	EXTINT13	Yes	30	External Interrupt 13
31	380$_H$	EXTINT14	Yes	31	External Interrupt 14
32	37C$_H$	EXTINT15	Yes	32	External Interrupt 15
33	378$_H$	CAN0	No	33	CAN Controller 0
34	374$_H$	CAN1	No	34	CAN Controller 1
35	370$_H$	CAN2	No	35	CAN Controller 2
36	36C$_H$	PPG0	Yes	36	Programmable Pulse Generator 0
37	368$_H$	PPG1	Yes	37	Programmable Pulse Generator 1
38	364$_H$	PPG2	Yes	38	Programmable Pulse Generator 2
39	360$_H$	PPG3	Yes	39	Programmable Pulse Generator 3
40	35C$_H$	PPG4	Yes	40	Programmable Pulse Generator 4
41	358$_H$	PPG5	Yes	41	Programmable Pulse Generator 5
42	354$_H$	PPG6	Yes	42	Programmable Pulse Generator 6
43	350$_H$	PPG7	Yes	43	Programmable Pulse Generator 7
44	34C$_H$	PPG8	Yes	44	Programmable Pulse Generator 8
45	348$_H$	PPG9	Yes	45	Programmable Pulse Generator 9
46	344$_H$	PPG10	Yes	46	Programmable Pulse Generator 10
47	340$_H$	PPG11	Yes	47	Programmable Pulse Generator 11
48	33C$_H$	PPG12	Yes	48	Programmable Pulse Generator 12
49	338$_H$	PPG13	Yes	49	Programmable Pulse Generator 13
50	334$_H$	PPG14	Yes	50	Programmable Pulse Generator 14
51	330$_H$	PPG15	Yes	51	Programmable Pulse Generator 15
52	32C$_H$	PPG16	Yes	52	Programmable Pulse Generator 16
53	328$_H$	PPG17	Yes	53	Programmable Pulse Generator 17

Interrupt vector table CY96(F)33x (3 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
54	324$_H$	PPG18	Yes	54	Programmable Pulse Generator 18
55	320$_H$	PPG19	Yes	55	Programmable Pulse Generator 19
56	31C$_H$	RLT0	Yes	56	Reload Timer 0
57	318$_H$	RLT1	Yes	57	Reload Timer 1
58	314$_H$	RLT2	Yes	58	Reload Timer 2
59	310$_H$	RLT3	Yes	59	Reload Timer 3
60	30C$_H$	PPGRLT	Yes	60	Reload Timer 6 - dedicated for PPG
61	308$_H$	ICU0	Yes	61	Input Capture Unit 0
62	304$_H$	ICU1	Yes	62	Input Capture Unit 1
63	300$_H$	ICU2	Yes	63	Input Capture Unit 2
64	2FC$_H$	ICU3	Yes	64	Input Capture Unit 3
65	2F8$_H$	ICU4	Yes	65	Input Capture Unit 4
66	2F4$_H$	ICU5	Yes	66	Input Capture Unit 5
67	2F0$_H$	ICU6	Yes	67	Input Capture Unit 6
68	2EC$_H$	ICU7	Yes	68	Input Capture Unit 7
69	2E8$_H$	ICU8	Yes	69	Input Capture Unit 8
70	2E4$_H$	ICU9	Yes	70	Input Capture Unit 9
71	2E0$_H$	OCU0	Yes	71	Output Compare Unit 0
72	2DC$_H$	OCU1	Yes	72	Output Compare Unit 1
73	2D8$_H$	OCU2	Yes	73	Output Compare Unit 2
74	2D4$_H$	OCU3	Yes	74	Output Compare Unit 3
75	2D0$_H$	OCU4	Yes	75	Output Compare Unit 4
76	2CC$_H$	OCU5	Yes	76	Output Compare Unit 5
77	2C8$_H$	OCU6	Yes	77	Output Compare Unit 6
78	2C4$_H$	OCU7	Yes	78	Output Compare Unit 7
79	2C0$_H$	OCU8	Yes	79	Output Compare Unit 8
80	2BC$_H$	OCU9	Yes	80	Output Compare Unit 9

Interrupt vector table CY96(F)33x (4 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8$_H$	OCU10	Yes	81	Output Compare Unit 10
82	2B4$_H$	OCU11	Yes	82	Output Compare Unit 11
83	2B0$_H$	FRT0	Yes	83	Free Running Timer 0
84	2AC$_H$	FRT1	Yes	84	Free Running Timer 1
85	2A8$_H$	FRT2	Yes	85	Free Running Timer 2
86	2A4$_H$	FRT3	Yes	86	Free Running Timer 3
87	2A0$_H$	RTC0	No	87	Real Timer Clock
88	29C$_H$	CAL0	No	88	Clock Calibration Unit
89	298$_H$	IIC0	Yes	89	I^{2}C interface
90	294$_H$	IIC1	Yes	90	I^{2}C interface
91	290$_H$	ADC0	Yes	91	A/D Converter
92	28C$_H$	ALARM0	No	92	Alarm Comparator 0
93	288$_H$	ALARM1	No	93	Alarm Comparator 1
94	284$_H$	LINR0	Yes	94	LIN USART 0 RX
95	280$_H$	LINT0	Yes	95	LIN USART 0 TX
96	27C$_H$	LINR1	Yes	96	LIN USART 1 RX
97	278$_H$	LINT1	Yes	97	LIN USART 1 TX
98	274$_H$	LINR2	Yes	98	LIN USART 2 RX
99	270$_H$	LINT2	Yes	99	LIN USART 2 TX
100	26C$_H$	LINR3	Yes	100	LIN USART 3 RX
101	268$_H$	LINT3	Yes	101	LIN USART 3 TX
102	264$_H$	LINR5	Yes	102	LIN USART 5 RX
103	260$_H$	LINT5	Yes	103	LIN USART 5 TX
104	25C$_H$	LINR7	Yes	104	LIN USART 7 RX
105	258$_H$	LINT7	Yes	105	LIN USART 7 TX
106	254$_H$	LINR8	Yes	106	LIN USART 8 RX
107	250$_H$	LINT8	Yes	107	LIN USART 8 TX

Interrupt vector table CY96(F)33x (5 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
108	24C$_H$	LINR9	Yes	108	LIN USART 9 RX
109	248$_H$	LINT9	Yes	109	LIN USART 9 TX
110	244$_H$	FLASH_A	No	110	Main Flash memory interrupt (only Flash devices)
111	240$_H$	reserved	-	-	reserved
112	23C$_H$	USB_EP0IN0	Yes	112	USB End point 0 IN
113	238$_H$	USB_EP0OUT0	Yes	113	USB End point 0 OUT
114	234$_H$	USB_EP10	Yes	114	USB End point 1
115	230$_H$	USB_EP20	Yes	115	USB End point 2
116	22C$_H$	USB_EP30	Yes	116	USB End point 3
117	228$_H$	USB_EP40	Yes	117	USB End point 4
118	224$_H$	USB_EP50	Yes	118	USB End point 5
119	220$_H$	USB_F10	No	119	USB function Flags 1 (SUSP SOF BRST WKUP CONF)
120	21C$_H$	USB_F20	No	120	USB function Flags 2 (SPK)
121	218$_H$	USB_H10	No	121	USB MiniHost 1 (DIRQ CNNIRQ URIRQ RWKIRQ)
122	214$_H$	USB_H20	No	122	USB MiniHost 2 (SOFIRQ CMPIRQ)

13. Handling Devices

Special care is required for the following when handling the device:
- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:
- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock
   - When using a single phase external clock, X0 pin must be driven and X1 pin left open.
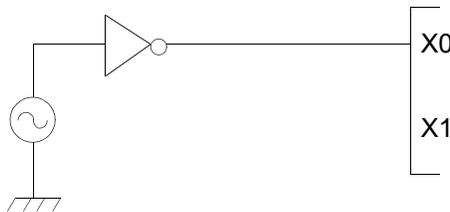
2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.
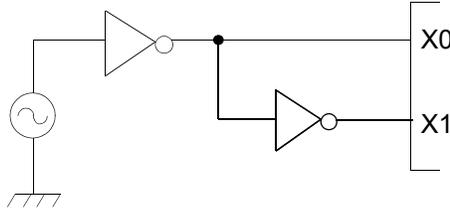
13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes $0.1V/\mu s$ or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [*1]
USB power supply voltage	V_{CC3}	V_{SS} - 0.3	V_{SS} + 4.0	V	USB device only
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V [*2]
USB Input voltage	V_{IUSB}	V_{SS} - 0.5	V_{SS} + 4.0	V	$V_{IUSB} \leq V_{CC3}$ + 0.5 (USB pins UDP, UDM)
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V [*2]
USB output voltage	V_{OUSB}	V_{SS} - 0.5	V_{SS} + 4.0	V	$V_{OUSB} \leq V_{CC3}$ + 0.5 (USB pins UDP, UDM)
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins [*3]
Total Maximum Clamp Current	$\Sigma|I_{CLAMP}|$	-	40	mA	Applicable to general purpose I/O pins [*3]
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
	I_{OLUSB}	-	36	mA	USB pins UDP, UDM
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
	$I_{OLAVUSB}$	-	15	mA	USB pins UDP, UDM
"L" level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
"L" level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
	I_{OHUSB}	-	-36	mA	USB pins UDP, UDM
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
	$I_{OHAVUSB}$	-	-15	mA	USB pins UDP, UDM
"H" level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
"H" level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs

Parameter	Symbol	Rating Min	Rating Max	Unit	Remarks
Permitted Power dissipation (Flash devices) [*4]	P_D	-	370[*5]	mW	$T_A=105^oC$
		-	740[*5]	mW	$T_A=85^oC$
		-	460[*5]	mW	$T_A=125^oC$, no Flash program/erase, CY96(F)338Y/R only [*6]
		-	550[*5]	mW	$T_A=120^oC$, no Flash program/erase, CY96(F)338Y/R only [*6]
Operating ambient temperature	T_A	0	+70	^oC	CY96V300B
		-40	+105		CY96(F)33x
		-40	+125		CY96(F)338Y/R[*6]
Storage temperature	T_{STG}	-55	+150	^oC	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3: • Applicable to all general purpose I/O pins (Pnn_m)
   • Use within recommended operating conditions.
   • Use at DC voltage (current)
   • The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
   • The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
   • Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
   • Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
   • Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

   • Sample recommended circuits:
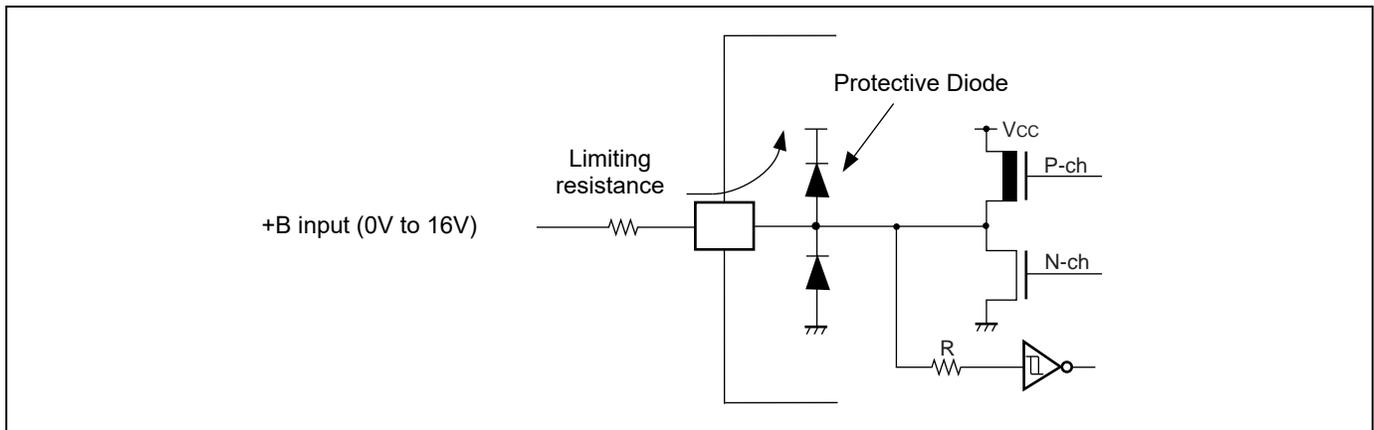
*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.

I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	**Typ**	**Max**		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
USB power supply voltage	V_{CC3}	3.0	3.3	3.6	V	USB device only
Smoothing capacitor at C pin	C_S	4.7	-	10	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

14.3 DC characteristics

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{CC3} = 3.0V \text{ to } 3.6V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5V$
				$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			TTL input selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IHUSB}	UDP, UDM	-	2.0	-	$V_{CC3} + 0.3$	V	USB pins
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	2.5	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	

$(T_A = -40°C$ to $125°C$, $V_{CC} = AV_{CC} = 3.0V$ to $5.5V$, $V_{CC3} = 3.0V$ to $3.6V$, $V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILUSB}	UDP, UDM	-	V_{SS} - 0.3	-	0.8	V	USB pins
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -1.6mA					
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -5mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -3mA					
	V_{OH3}	3mA outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -2mA					
	V_{OHUSB}	UDP, UDM	$3.0V \leq V_{CC3} < 3.6V$ I_{OH} = -20mA	V_{CC3} - 0.4	-	-	V	USB pins

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{CC3} = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OL} = +2mA $3.0V \leq V_{CC} < 4.5V$ I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OL} = +5mA $3.0V \leq V_{CC} < 4.5V$ I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA
	V_{OL3}	3mA outputs	$3.0V \leq V_{CC} \leq 5.5V$ I_{OL} = +3mA	-	-	0.4	V	
	V_{OLUSB}	UDP, UDM	$3.0V \leq V_{CC3} < 3.6V$ I_{OL} = +20mA	-	-	0.4	V	USB pins
Input leak current	I_{IL}	Pnn_m (except USB pins)	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	μA	Single port pin
USB input leak current		UDP, UDM	$V_{SS} < V_I < V_{CC3}$	-5	-	+5	μA	USB pins
Pull-up resistance	R_{UP}	Pnn_m, RSTX	V_{CC} = 3.3V ± 10%	40	100	160	kΩ	
			V_{CC} = 5.0V ± 10%	25	50	100	kΩ	

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz, CLKP3 = 48MHz	+25°C	39	47	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			+125°C	40	50		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	45	57	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 2 Flash/ROM wait states
			+125°C	46	60		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	56	68	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			+125°C	57	71		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 4MHz	+25°C	5	6	mA	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			+125°C	5.6	9		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 2MHz	+25°C	2.9	4	mA	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			+125°C	3.5	6.5		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 0	+25°C	0.4	0.6	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode 1 Flash/ROM wait state
			+125°C	0.9	3.5		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 1	+25°C	0.15	0.25	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.65	3.2		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 32kHz	+25°C	0.1	0.2	mA	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.6	3		

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz CLKP3 = 48MHz	+25°C	12.5	15	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V
			+125°C	13.3	17.5		
		PLL Sleep mode with CLKS1/2 = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	17	20	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V
			+125°C	17.8	22.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	19	22	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V
			+125°C	19.8	24.5		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2/3 = 4MHz	+25°C	1.9	2.3	mA	CLKPLL, CLKSC and CLKRC stopped
			+125°C	2.4	5		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 2MHz	+25°C	0.9	1.4	mA	CLKMC, CLKPLL and CLKSC stopped
			+125°C	1.5	4.1		
	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 100kHz, SMCR:LPMSS = 0	+25°C	0.3	0.5	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			+125°C	0.8	3.4		
		RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 100kHz, SMCR:LPMSS = 1	+25°C	0.06	0.15	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			+125°C	0.56	3		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2/3 = 32kHz	+25°C	0.04	0.12	mA	CLKMC, CLKPLL and CLKRC stopped
			+125°C	0.54	2.9		

$(T_A = -40°C$ to $125°C, V_{CC} = AV_{CC} = 3.0V$ to $5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz	+25°C	1.6	2	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V
			+125°C	2.1	4.8		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0	+25°C	0.35	0.5	mA	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode
			+125°C	0.85	3.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1	+25°C	0.1	0.15	mA	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode
			+125°C	0.6	2.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0	+25°C	0.35	0.5	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			+125°C	0.85	3.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1	+25°C	0.1	0.15	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			+125°C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0	+25°C	0.3	0.45	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			+125°C	0.8	3.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1	+25°C	0.05	0.1	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			+125°C	0.55	2.8		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz	+25°C	0.03	0.1	mA	CLKMC, CLKPLL and CLKRC stopped
			+125°C	0.53	2.8		

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110$_B$	+25°C	0.02	0.08	mA	Core voltage at 1.8V
			+125°C	0.52	2.8		
		VRCR:LPMB[2:0] = 000$_B$	+25°C	0.015	0.06	mA	Core voltage at 1.2V
			+125°C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25°C	90	140	µA	This current must be added to all Power supply currents above
			+125°C	100	150		
Clock modulator current	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

*: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

14.4 AC Characteristics

Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode". PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
		X0A, X1A	0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	
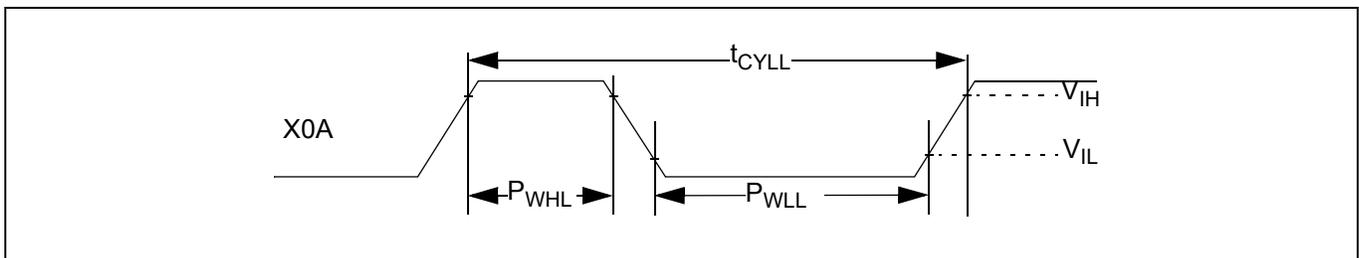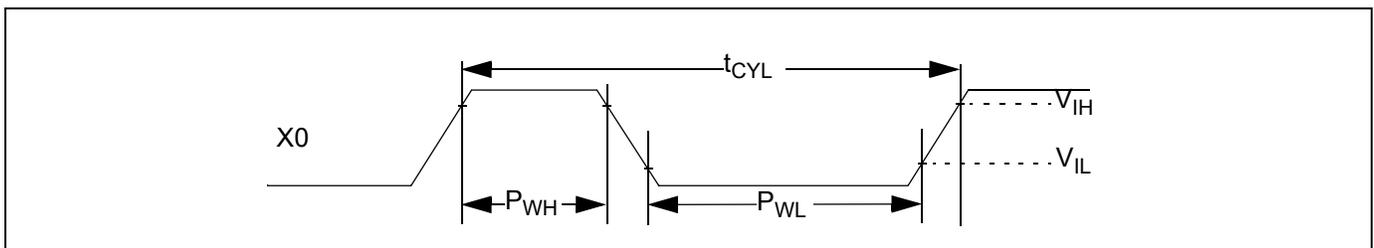
Internal Clock timing

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	90	0	96	MHz	CY96F33x
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	43.5	0	48	MHz	CY96F33x
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	
Internal peripheral clock frequency (Clock CLKP3)	f_{CLKP3}	0	43.5	0	48	MHz	CY96F33x

WARNING: For USB usage, it is important to change the voltage regulator setting to output 1.9V. Please refer to the chapter Standby Mode and Voltage Regulator control circuit of the hardware manual to perform such setting.

External Reset timing

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	
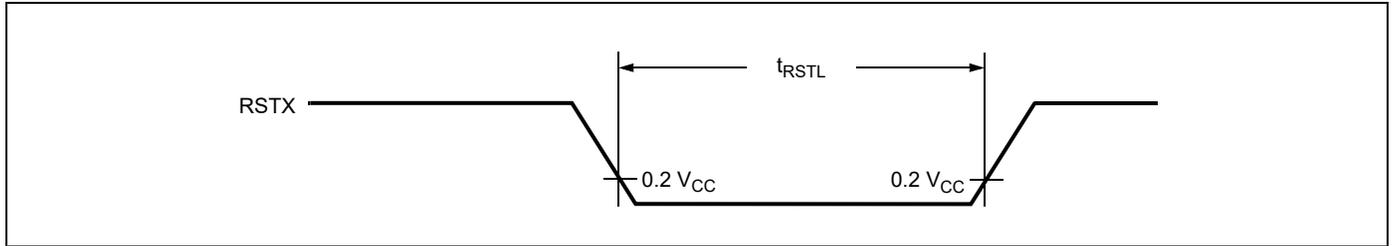
Power On Reset timing

(T$_A$ = -40°C to 125°C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t$_R$	Vcc	0.05	-	30	ms	
Power off time	t$_{OFF}$	Vcc	1	-	-	ms	
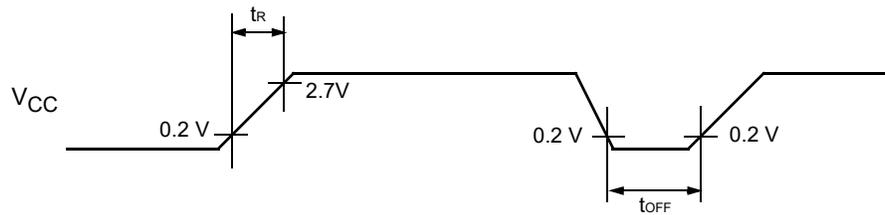
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

External Input timing

$(T_A = -40°C$ to $125°C, V_{CC} = AV_{CC} = 3.0V$ to $5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	**Max**		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1} + 200$ $(t_{CLKP1}=1/f_{CLKP1})$	—	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics
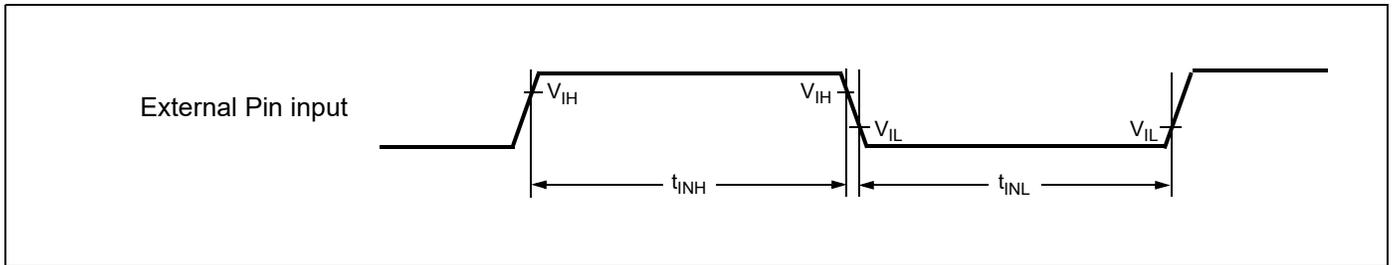
USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [*1]	—	N*t_{CLKP1} - 30 [*1]	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock "L" pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock "H" pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96300 Super series Hardware Manual"
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...

Internal Shift Clock Mode

External Shift Clock Mode
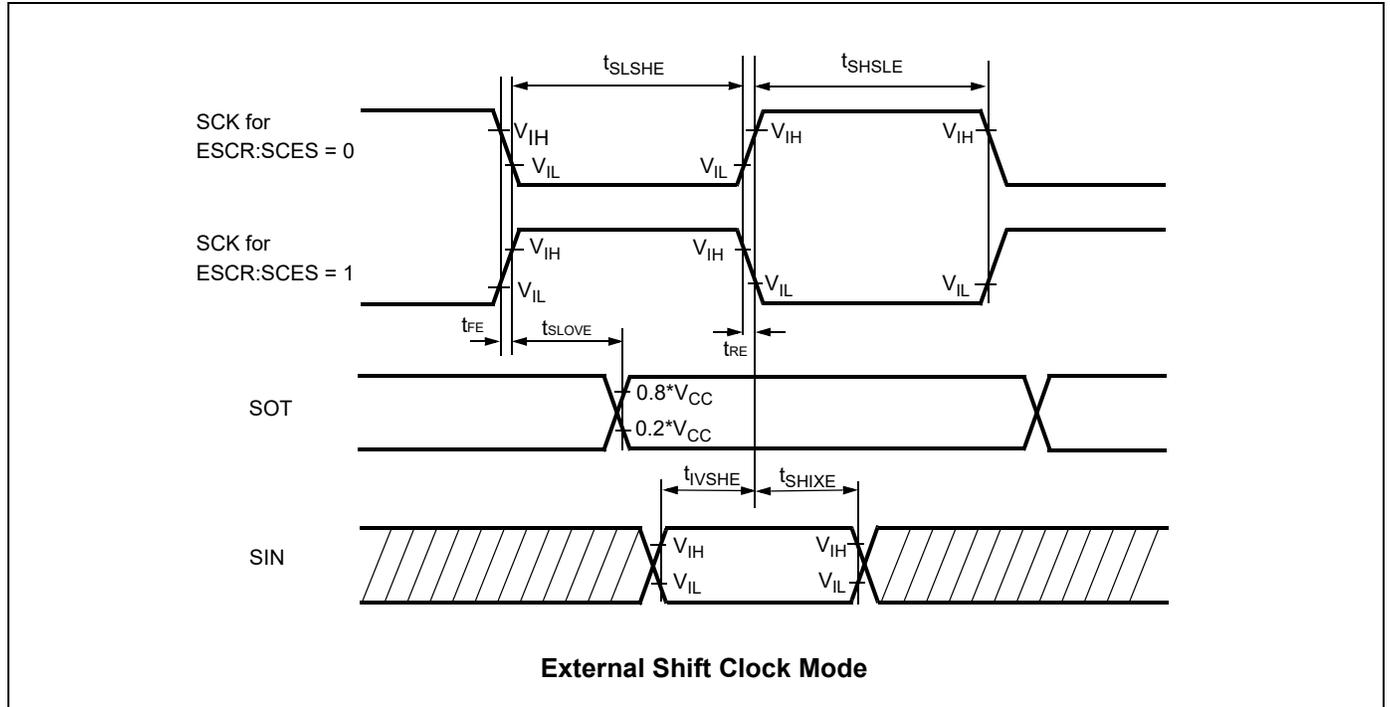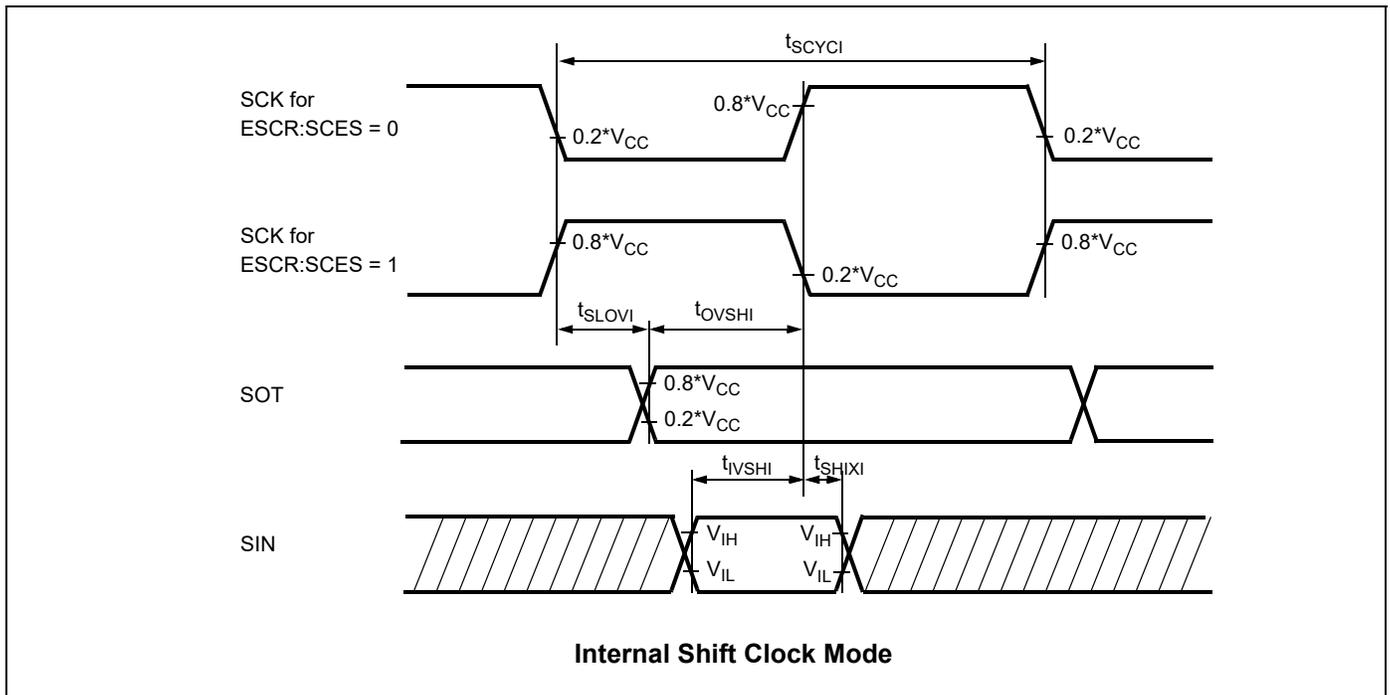
External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			$t_{CYC}/2$-5	$t_{CYC}/2$+5		
	t_{CLCH}			$t_{CYC}/2$-5	$t_{CYC}/2$+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-15	15	ns	
	t_{CLAV}			-15	15		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 3.0$ to $4.5V$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
	t_{CLCH}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-20	20	ns	
	t_{CLAV}			-20	20		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

Refer to the Hardware Manual for detailed Timing Charts
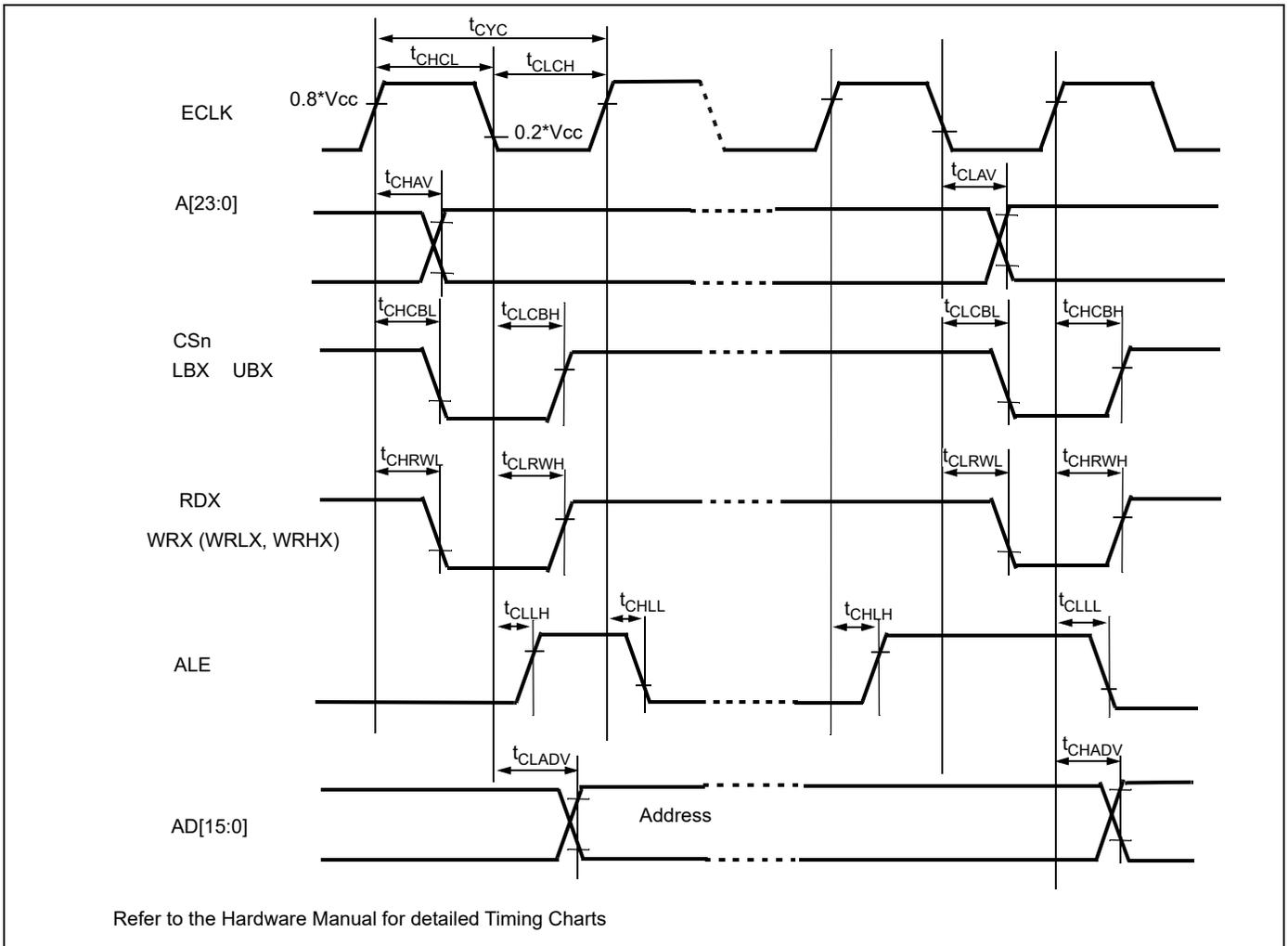
Bus Timing (Read)

($T_A = -40°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	**Max**		
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	—	ns	EBM:NMS = 0
			EACL:STS=1	$t_{CYC} - 5$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	—		
Valid address $\Rightarrow$ ALE $\downarrow$ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	—		
ALE $\downarrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
Valid address $\Rightarrow$ RDX $\downarrow$ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 15$	—	ns	
Valid address $\Rightarrow$ RDX $\downarrow$ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
Valid address $\Rightarrow$ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 55$	ns	w/o cycle extension

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm$ 10%, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
Valid address $\Rightarrow$ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	—	$3\,t_{CYC}/2 - 5$	—	ns	w/o cycle extension
RDX $\downarrow$ $\Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3\,t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX $\uparrow$ $\Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid $\Rightarrow$ Data hold time	t_{AXDX}	A[23:0], AD[15:0]	—	0	—	ns	
RDX $\uparrow$ $\Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:0], ECLK		$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK	—	$t_{CYC}/2 - 15$	—		
RDX $\downarrow$ $\Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE $\downarrow$ $\Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	-10	—		
ECLK$\uparrow$ $\Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

$(T_A = -40°C \text{ to } +125°C, V_{CC} = 3.0 \text{ to } 4.5V, V_{SS} = 0.0 \text{ V}, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Symbol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address $\Rightarrow$ ALE $\downarrow$ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	EBM:NMS = 0
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE $\downarrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		
Valid address $\Rightarrow$ RDX $\downarrow$ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 20$	—	ns	
Valid address $\Rightarrow$ RDX $\downarrow$ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
Valid address $\Rightarrow$ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 60$	ns	w/o cycle extension

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 3.0$ to $4.5V$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	

Refer to the Hardware Manual for detailed Timing Charts
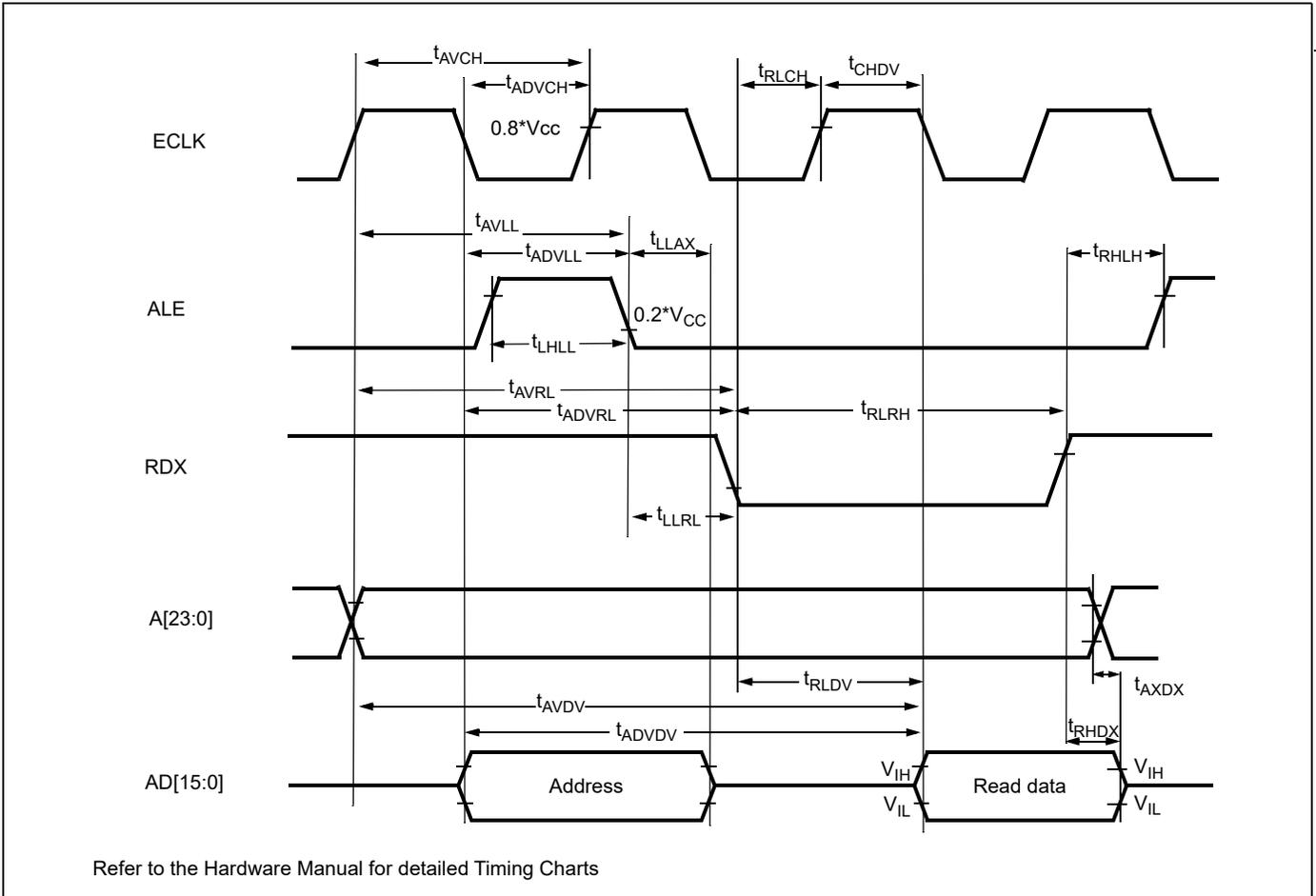
Bus Timing (Write)

$(T_A = -40°C \text{ to } +125°C, V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ WRX $\downarrow$ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 15$	—		
Valid address $\Rightarrow$ WRX $\downarrow$ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 5$	—	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 20$	—	ns	w/o cycle extension
WRX $\uparrow$ $\Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 15$	—	ns	
WRX $\uparrow$ $\Rightarrow$ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	$- 15$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX $\uparrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	
WRX $\uparrow$ $\Rightarrow$ ALE $\uparrow$ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	—		
WRX $\downarrow$ $\Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
CSn $\Rightarrow$ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 15$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 15$		
CSn $\Rightarrow$ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 15$		

$(T_A = -40°C \text{ to } +125°C, V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	**Max**		
WRX $\Rightarrow$ CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	-15	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX $\Rightarrow$ CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	

$(T_A = -40°C \text{ to } +125°C, V_{CC} = 3.0 \text{ to } 4.5V, V_{SS} = 0.0 \text{ V}, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	**Max**		
Valid address $\Rightarrow$ WRX $\downarrow$ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 20$	—		
Valid address $\Rightarrow$ WRX $\downarrow$ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX $\uparrow$ $\Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX $\uparrow$ $\Rightarrow$ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	-20	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX $\uparrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	
WRX $\uparrow$ $\Rightarrow$ ALE $\uparrow$ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	—		
WRX $\downarrow$ $\Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	

$(T_A = -40°C \text{ to } +125°C, V_{CC} = 3.0 \text{ to } 4.5V, V_{SS} = 0.0 \text{ V}, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CSn ⇒ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 20$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 20$		
CSn ⇒ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 20$		
WRX ⇒ CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	-20	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX ⇒ CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	

Refer to the Hardware Manual for detailed Timing Charts
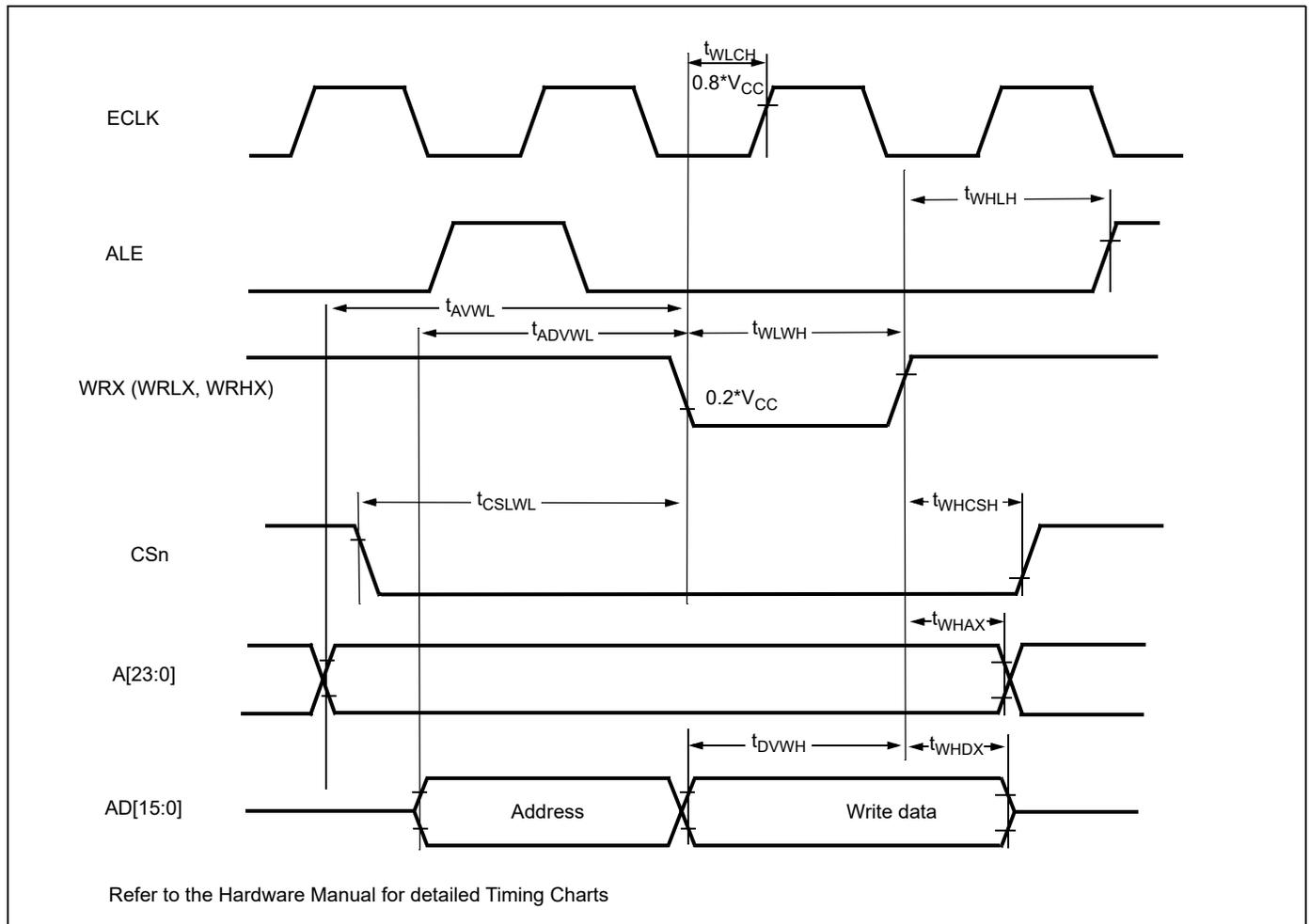
Ready Input Timing

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 5.0$ V $± 10\%$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 3.0$ to $4.5V$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

Refer to the Hardware Manual for detailed Timing Charts
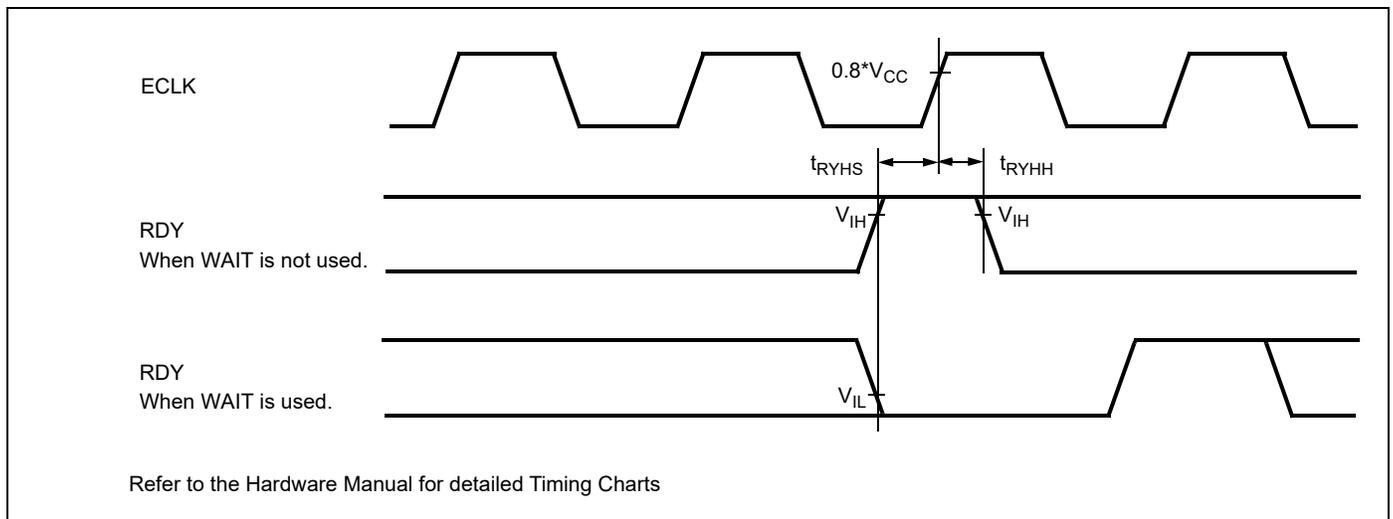
Hold Timing

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 5.0$ V $\pm 10\%$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	**Max**		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t_{XHAL}	HAKX	—	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

$(T_A = -40°C$ to $+125°C$, $V_{CC} = 3.0$ to $4.5V$, $V_{SS} = 0.0$ V, $IO_{drive} = 5mA$, $C_L = 50pF)$

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	**Max**		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t_{XHAL}	HAKX	—	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	

Refer to the Hardware Manual for detailed Timing Charts
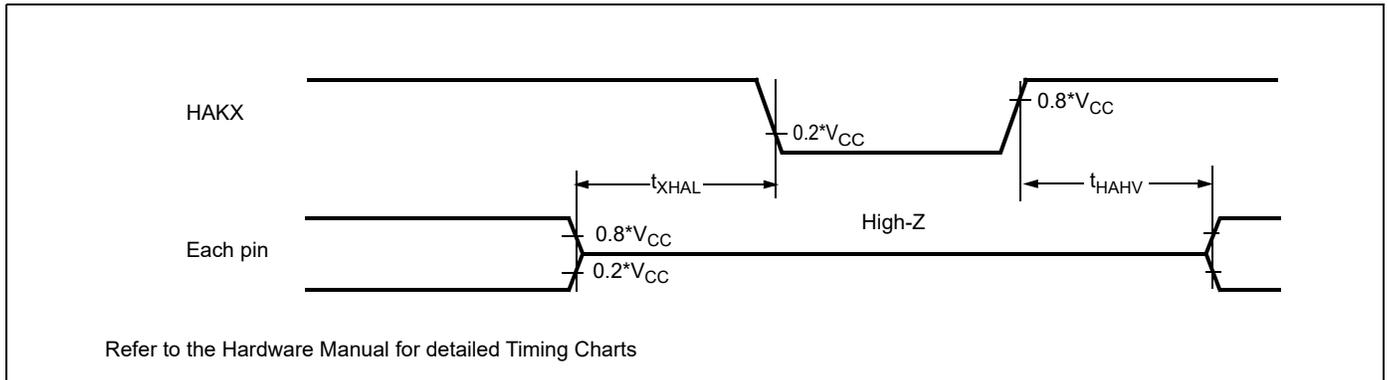
I^{2}C Timing

$(T_A$ = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	R = 1.7 kΩ, C = 50 pF[1]	4.7	—	0.6	—	μs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45[2]	0	0.9[3]	μs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	μs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.
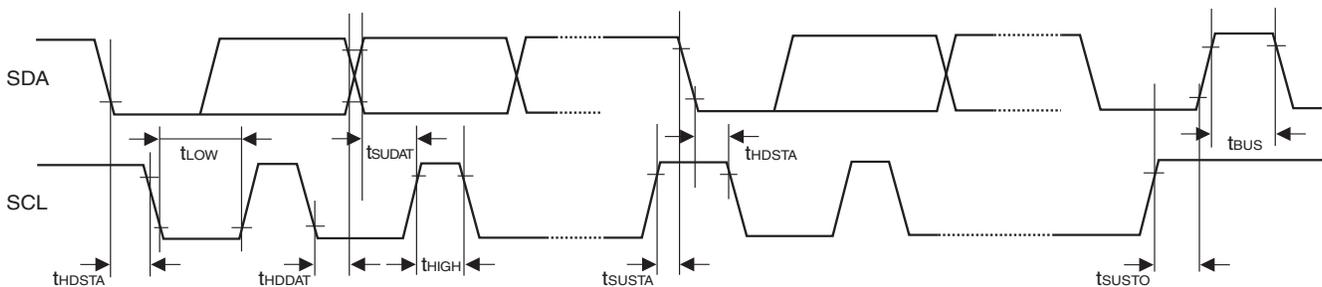
14.5 USB Characteristics

(T$_A$ = -40°C to 105°C, V$_{CC}$ = AV$_{CC}$= 3.0V to 5.5V,V$_{SS}$ = AV$_{SS}$ = 0V, V$_{CC3}$ = 3.0V to 3.6V, USB pins UDP and UDM)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	**Max**		
Input characteristics	Input High level voltage	V$_{IH}$	—	2.0	V$_{CC}$ + 0.3	V	*1
	Input Low level voltage	V$_{IL}$	—	V$_{SS}$ − 0.3	0.8	V	*1
	Differential input sensitivity	V$_{DI}$	—	0.2	—	V	*2
	Differential common mode input voltage	V$_{CM}$	—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V$_{OH}$	External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V$_{OL}$	External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V$_{CRS}$	—	1.3	2.0	V	*4
	Rise time	t$_{FR}$	—	4	20	nS	*5
	Fall time	t$_{FF}$	—	4	20	nS	*5
	Rise/fall time matching	t$_{RFM}$	—	90	111.11	%	*5
	Output impedance	Z$_{DRV}$	—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C$_{EDGE}$	—	—	75	pF	*6
Series resistance		R$_S$	—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V$_{IL}$ (Max) = 0.8 [V],
V$_{IH}$ (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

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*2 : Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 [mV] of differential input sensitivity when the differential data input is within 0.8 [V] to 2.5 [V] to the local ground reference level.
Above voltage range is the common mode input voltage range.
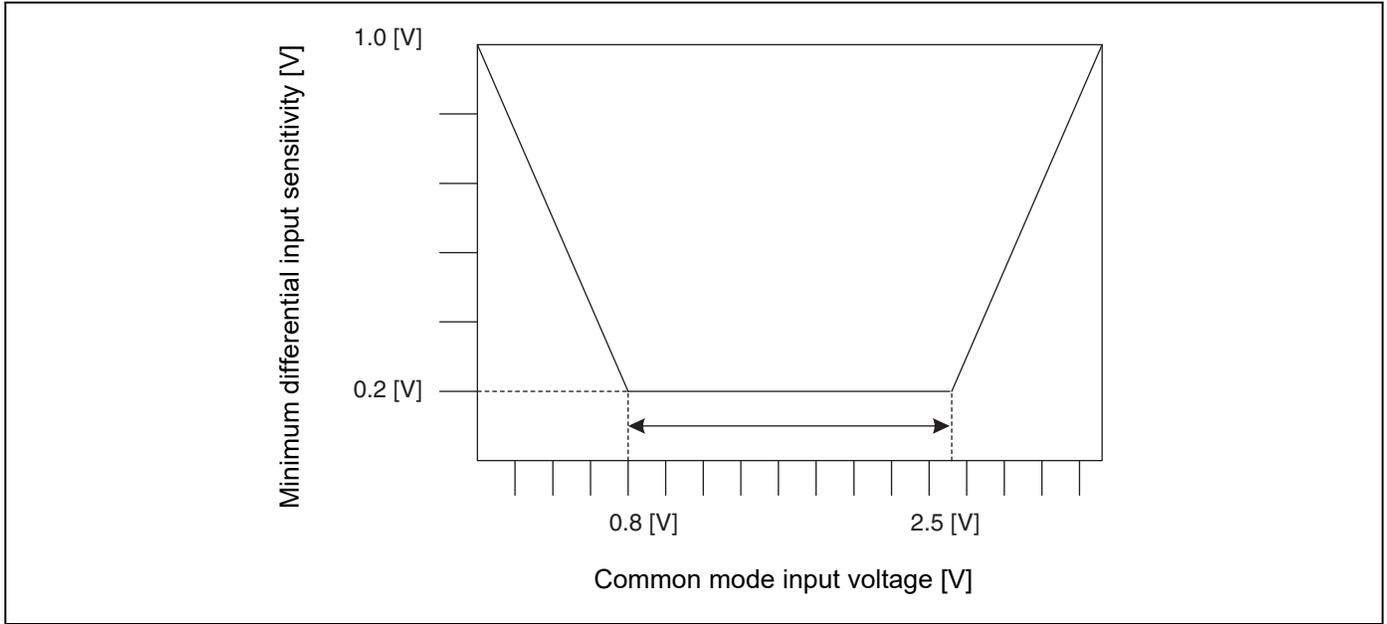
*3 : The output drive capability of the driver is below 0.3 [V] at Low-State (V_{OL}) (to 3.6 [V] and 1.5 kΩ load), and 2.8 [V] or above (to the V_{SS} and 1.5 kΩ load).

*4 : The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 [V] to 2.0 [V].
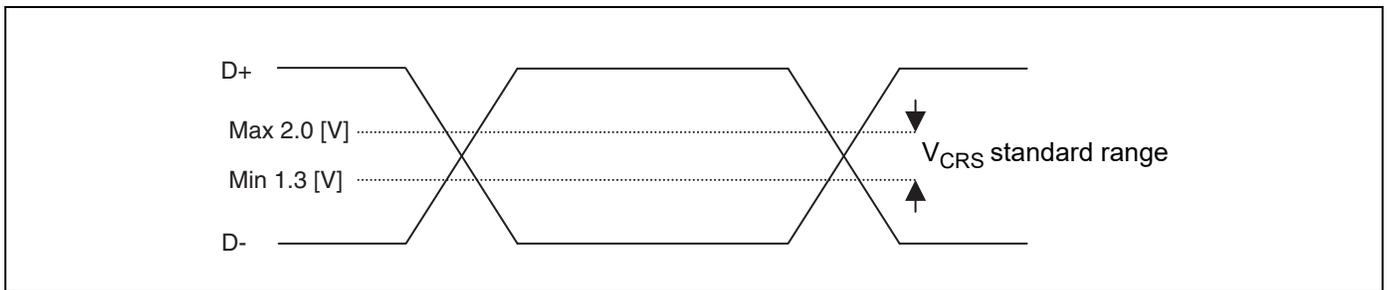
*5 : Regarding t_{FR} , t_{FF}, t_{RFM}
They indicate rise time (Trise) and fall time (Tfall) of the differential data signal.
They are defined by the time between 10% to 90% of the output signal voltage.
For full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ±10% to minimize RFI emission.
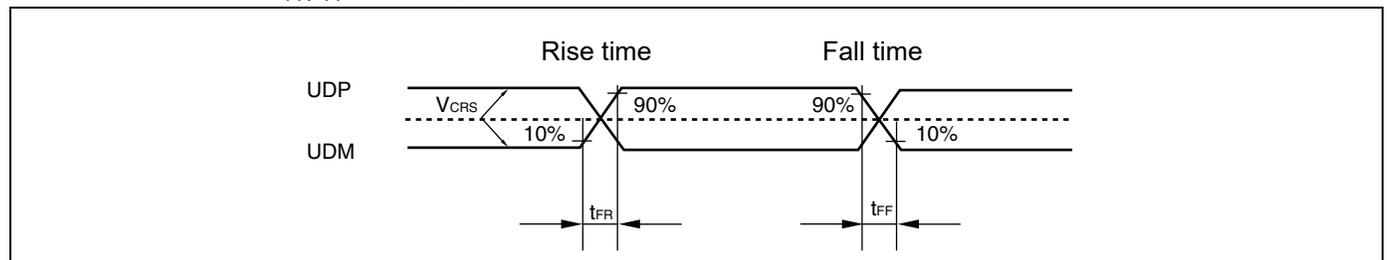
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*6 : The place to connect transceiver edge rate control capacitance C_{EDGE}

For this USB I/O, it is recommended to use C_{EDGE} control capacitor.

For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 to 50 [pF] (recommended value : 47 [pF] := 50[pF]) to D + and D − lines when implementing on the board.
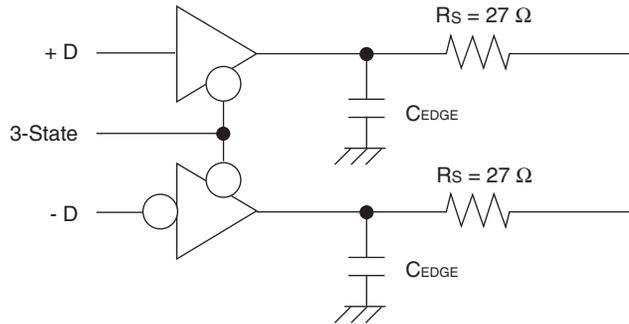
Driver output impedance 3 Ω to 19 Ω
Rs serial resistance value 25 Ω to 30 Ω
Please apply 27 Ω of serial resistance value as a recommended value.

14.6 Analog Digital Converter

$(T_A = -40\ °C\ to\ +125\ °C,\ 3.0\ V \leq AVRH - AVRL,\ V_{CC} = AV_{CC} = 3.0V\ to\ 5.5V,\ V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	$4.5V \leq AV_{CC} \leq 5.5V$
			2.0	-	-	µs	$3.0V \leq AV_{CC} < 4.5V$
Sampling time	-	-	0.5	-	-	µs	$4.5V \leq AV_{CC} \leq 5.5V$
			1.2	-	-	µs	$3.0V \leq AV_{CC} < 4.5V$
Analog port input current	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input current	I_{AIN}	ANn	-1	-	+1	µA	$T_A = 25\ °C$, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	$T_A = 125\ °C$, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

Nonlinearity error: Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.
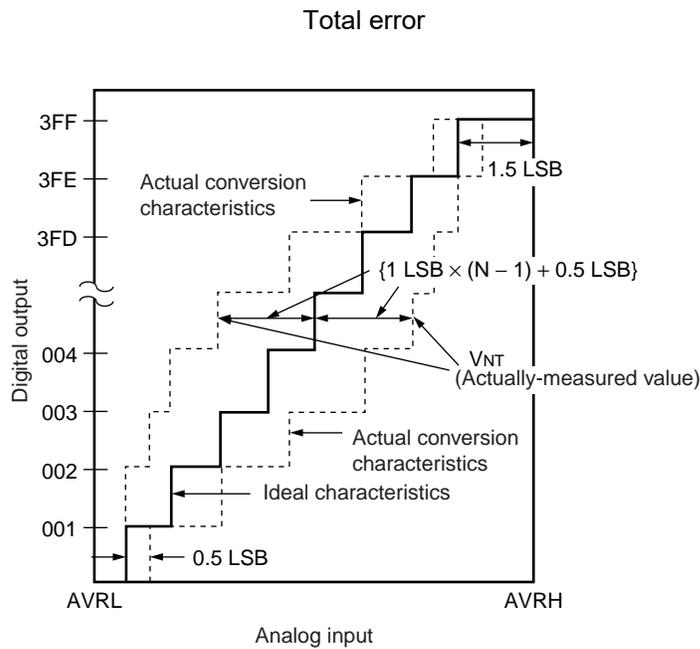
Total error

$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\,\text{LSB} \times (N - 1) + 0.5\,\text{LSB}\}}{1\,\text{LSB}}\quad[\text{LSB}]$$

$$1\,\text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\quad[\text{V}]$$

N: A/D converter digital output value

V_{OT} (Ideal value) $= AVRL + 0.5\,\text{LSB}$ [V]

V_{FST} (Ideal value) $= AVRH - 1.5\,\text{LSB}$ [V]

V_{NT} : A voltage at which digital output transitions from $(N - 1)$ to N.

Nonlinearity error
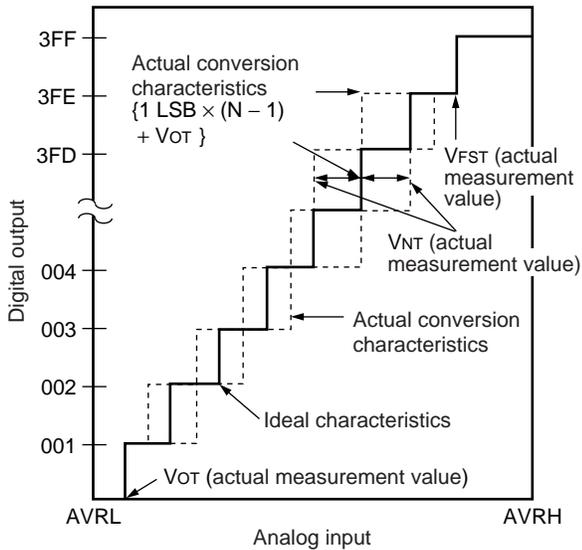
Differential nonlinearity error
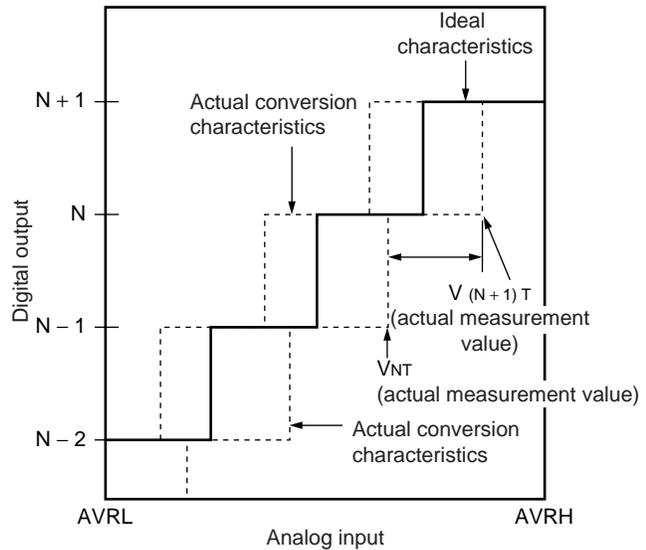
$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

Notes on A/D Converter Section

• About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

analog input circuit model:
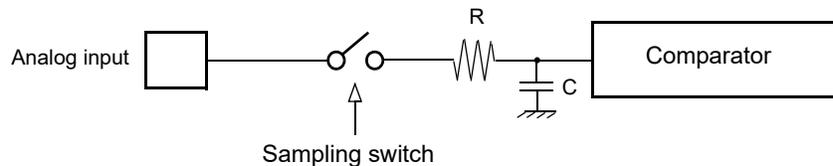
Reference value:
• C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where τ = RC. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = 7 × (R_{ext} + 2.6kΩ) × C for 4.5 ≤ AV_{cc} ≤ 5.5

T_{samp} [min] = 7 × (R_{ext} + 12.1kΩ) × C for 3.0 ≤ AV_{cc} ≤ 4.5

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

14.7 Alarm Comparator

$(T_A = -40\ °C\ \text{to}\ +125\ °C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}		-1	-	+1	µA	$T_A = 25\ °C$
			-3	-	+3	µA	$T_A = 125\ °C$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		$0.36 * AV_{CC}$ -0.25	$0.36 * AV_{CC}$ -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	$0.36 * AV_{CC}$ +0.1	$0.36 * AV_{CC}$ +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		$0.78 * AV_{CC}$ -0.25	$0.78 * AV_{CC}$ -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$	ALARM0, ALARM1		$0.78 * AV_{CC}$ +0.1	$0.78 * AV_{CC}$ +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	Threshold levels specified above are not guaranteed within this time
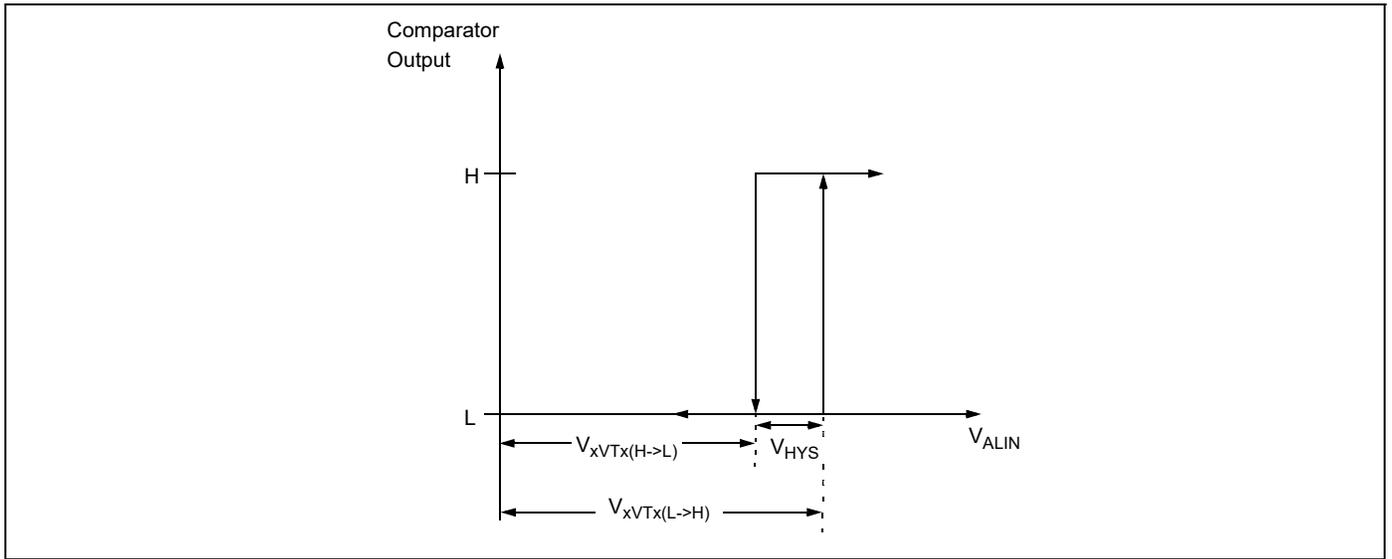
14.8 Low Voltage Detector characteristics

$(T_A = -40 \,°C \text{ to } +125 \,°C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)$

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	60	75	µs	
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\dfrac{dV}{dt}\right| \leq 0.004 \dfrac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.
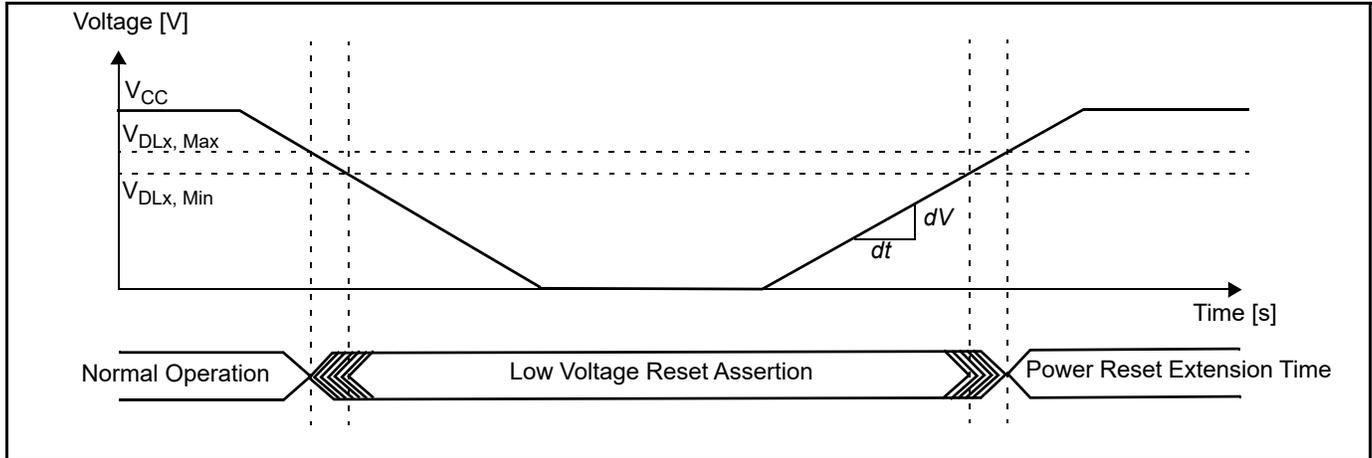
14.9 FLASH memory program/erase characteristics

$(T_A = -40°C \text{ to } 105°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Value			Unit	Remarks
	Min	**Typ**	**Max**		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

15. Package Dimension CY96(F)33x LQFP 144P

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

SECTION A-A'
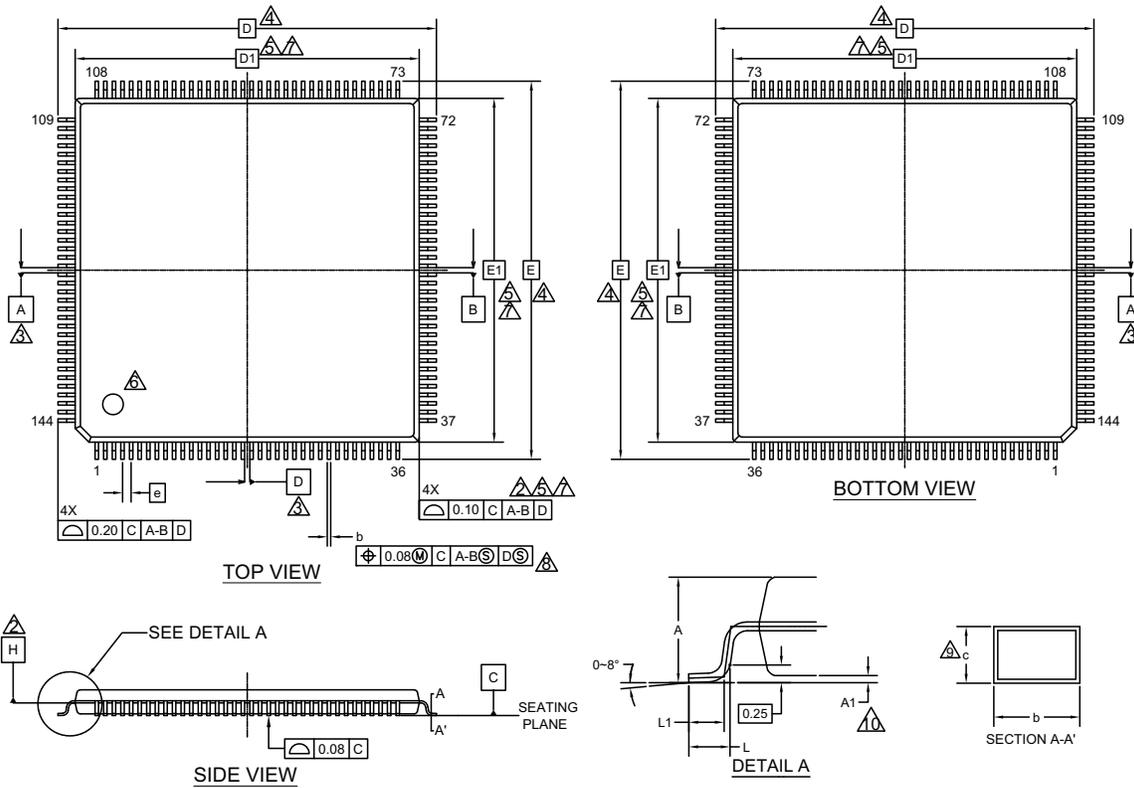
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS

2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.

4. TO BE DETERMINED AT SEATING PLANE C.

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.

8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *A

16. Ordering Information

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package	Remarks
CY96F336USAPMC-GS-UJE2	Flash A (288KB)	No	No	144 pin Plastic LQFP (LQS144)	with USB
CY96F338RSAPMC-GS-UJE2	Flash A (544KB)	No	No	144 pin Plastic LQFP (LQS144)	
CY96F338RSAPMCR-G-UJE2					
CY96F338RWAPMC-GS-UJE2		Yes			
CY96F338USAPMC-GS-UJE2	Flash A (544KB)	No	No	144 pin Plastic LQFP (LQS144)	with USB

17. Revision History

Revision	Date	Modification
Prelim 0.1	2007-05-23	Creation
Prelim 0.2	2007-08-14	- information about MB96F338U (with USB function) is added - DMA 8ch --> 16ch - ADC reference switch is removed
Prelim 0.3	2007-09-11	- Circuit Type of Device with "U" suffix is added - Circuit Type diagram: TTL input cell type was changed from NOR to NAND - IO Map, IRQ table are updated - Parallel Programing Flash Memory Control Signals is updated - DC/AC spec of USB I/O is added
Prelim 0.4	2007-09-24	- Block diagram for MB96F338U was corrected: USB PB1 -> PB3 - IRQ table was modified: Vector number 111 was inserted (reserved) - Pin assignment was corrected: not used resource name was removed
Prelim 0.5	2007-11-02	- Internal Max Freq 56MHz --> 48MHz - DMA 12ch --> 10ch - FPT-144P-M12 package was removed
Prelim 1	2007-12-20	Update of the block diagram to include USB block. Update DC characteristics to include all USB pins characteristics. IOMAP regenerated. Memory maps and Flash configuration reworked. Typos corrected across the document. Renaming of the Flash banks.

Prelim 2	2008-02-07	• Features:
		  - Removed ADC reference switch
		  - changed USB description
		• Lineup:
		  - option description added
		  - Part number names corrected
		  - Flash B removed
		  - RLT6 added
		• Block diagrams:
		  - Flash B removed
		  - OUT5_R -> OUT6_R
		  - TX2_R, RX2_R added
		  - SIN2_R, SOT2_R, SCK2_R and SOT9 added
		  - not existing TTGx, TTGx_R and PPGx_R pins deleted
		  - RLT6 added
		• Pin function description: relocated clock output and CAN pins added
		• I/O circuit types updated
		• Memory maps replaced by new standard maps
		• Parallel Flash programming pinning removed
		• IOMAP regenerated (naming style changed, all reserved registers added)
		• DC current limits updated with new setting and corrected frequencies
		• External bus timings: missing conditions added and readability improved
		• Alarm comparator spec updated (transition voltages defined)
		• Ordering information updated
		• Typos and formatting corrected

Revision	Date	Modification
Prelim 3	2008-11-24	• Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added) • Note about devices under development modified • I/O map: Note added about reserved addresses • Serial programming interface: Note about handshaking pins improved • specified AD converter channel offset to 4LSB • package code of MB96V300 corrected in ordering information • Added voltage condition to pull-up resistance spec • ROM devices removed from lineup, memory map and ordering information • Ordering information: column "Flash/ROM added" • Official package dimension drawing with additional notes added • Empty pages removed • adjusted Run and Sleep mode specifications according to evaluation results • Absolute maximum ratings: V_{IUSB} and V_{OUSB} corrected, permitted power dissipation spec added • DC characteristics: Output H/L voltage for USB pins: specified for load of 20mA • USB characteristics: updated according to MB91660 series • Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time newly added • Handling devices: Notes added about Serial communication and about using ceramic resonators. • Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor • AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz • New family member MB96F336U added • VOL3 spec improved: spec valid for 3mA load for full Vcc range

18. Major Changes

Page	Section	Change Results
Rev *A		
108	Electrical Characteristics 5. Analog Digital Converter	Changed the item for "Zero reading voltage" and "Full scale reading voltage".
Rev *B		
-		Marketing Part Numbers changed from an MB prefix to a CY prefix.
5	1. Product Lineup	Deleted the following comment. Note: MB96F336 and MB96F338 devices are under development and specification is preliminary. These products under development may change its specification without notice.
9 115 116	3. Pin Assignments 15. Package Dimension 16. Ordering Information	Package description modified to JEDEC description. (before) FPT-144P-M08 (after) LQS144
-	Example Characteristics	Removed 15. Example Characteristics section
116	16. Ordering Information	Deleted the following comment. *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice. Deleted the following parts number. - MB96F336USA PMC-GSE2 *1 - MB96F336UWA PMC-GSE2 *1 - MB96F338YSA PMC-GSE2 *1 - MB96F338RSA PMC-GSE2 *1 - MB96F338YWA PMC-GSE2 *1 - MB96F338RWA PMC-GSE2 *1 - MB96F338USA PMC-GSE2 *1 - MB96F338UWA PMC-GSE2 *1 - MB96V300BRB-ES (for evaluation) Revised the following parts number. (before) - MB96F336USA PMC-GSE2 *1 - MB96F338RSA PMC-GSE2 *1 - MB96F338RWA PMC-GSE2 *1 - MB96F338USA PMC-GSE2 *1 (after) - CY96F336USAPMC-GS-UJE2 - CY96F338RSAPMC-GS-UJE2 - CY96F338RWAPMC-GS-UJE2 - CY96F338USAPMC-GS-UJE2 Added the following parts number. - CY96F338RSAPMCR-G-UJE2

Document History

Document Title: CY96330 Series F^{2}MC-16FX 16-bit Proprietary Microcontroller **Document Number: 002-04586**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	AKIH	05/23/2007	Migrated to Cypress and assigned document number 002-04586. No change to document contents or format.
*A	5245336	AKIH	05/13/2016	Updated to Cypress template.
*B	6398080	GSHI	12/03/2018	Revised the following items: - Changed marketing part numbers from prefix MB to CY. - Updated package code as LQS144 on 3.Pin Assignments and 15.Package Dimension - Added 18. Major Changes For details, please see 18.Major Changes
*C	6580904	KSUN	05/24/2019	Updated to new template.

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