PerFET™ Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

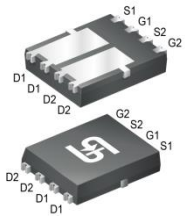
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	7.6	mΩ
	V_{GS} = 7V	9.1	
Q_g	V_{GS} = 10V	19	nC

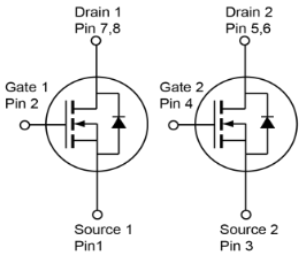
APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56U Dual





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	64	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	34	A
	T_C = 100°C		34	
	T_A = 25°C		15	
Pulsed Drain Current		I_{DM}	136	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	17	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	43.6	mJ
Total Power Dissipation	T_C = 25°C	P_D	55.6	W
	T_C = 125°C		18.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	2.7	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	2.4	3	3.6	V
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 40V T_J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 17A	$R_{DS(on)}$	--	6.5	7.6	mΩ
	V_{GS} = 7V, I_D = 17A		--	7.5	9.1	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 10A	g_{fs}	--	42	--	S
Dynamic						
Total Gate Charge	V_{GS} = 7V, V_{DS} = 20V, I_D = 15A	Q_g	--	13.6	--	nC
Total Gate Charge	V_{GS} = 10V, V_{DS} = 20V, I_D = 15A	Q_g	--	19	--	
Gate-Source Charge		Q_{gs}	--	5.7	--	
Gate-Drain Charge		Q_{gd}	--	3.8	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	C_{iss}	--	1217	--	pF
Output Capacitance		C_{oss}	--	235	--	
Reverse Transfer Capacitance		C_{rss}	--	17	--	
Gate Resistance	f = 1.0MHz	R_g	--	1.7	--	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 20V, I_D = 15A, R_G = 3.3Ω	$t_{d(on)}$	--	9.9	--	nS
Rise Time		t_r	--	49.3	--	
Turn-Off Delay Time		$t_{d(off)}$	--	18.2	--	
Fall Time		t_f	--	5	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 17A	V_{SD}	--	--	1.1	V
Reverse Recovery Time	I_S = 15A, di/dt = 100A/μs	t_{rr}	--	30	--	nS
Reverse Recovery Charge		Q_{rr}	--	23	--	nC

Notes:

1. Package current limit.
2. L = 0.3mH, V_{GS} = 10V, R_G = 25Ω, Starting T_J = 25°C.
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

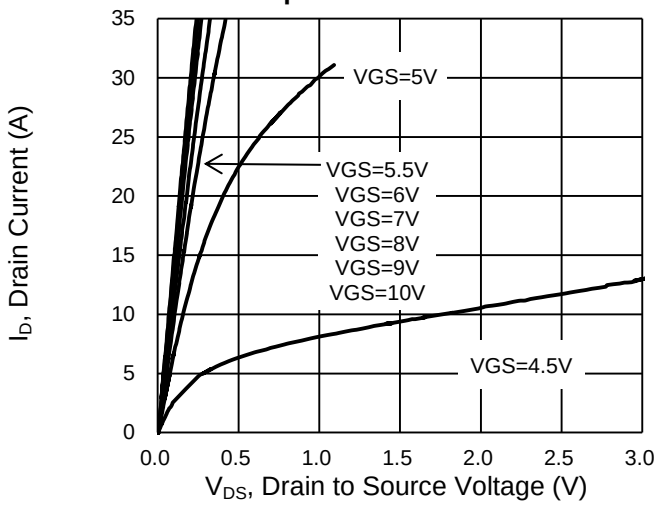
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM076NH04DCR RLG	PDFN56U Dual	2,500pcs / 13” Reel

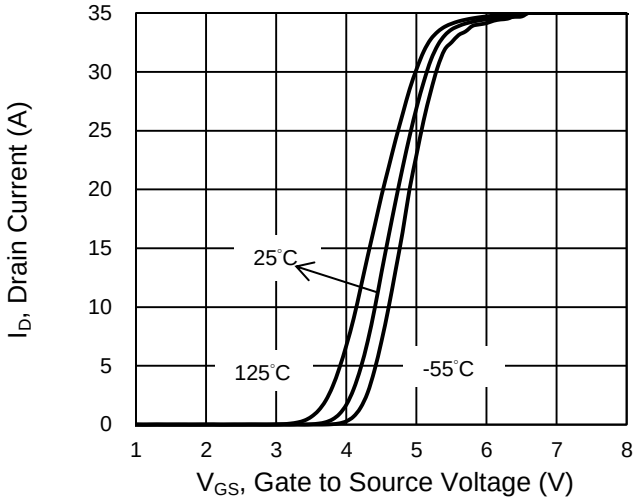
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

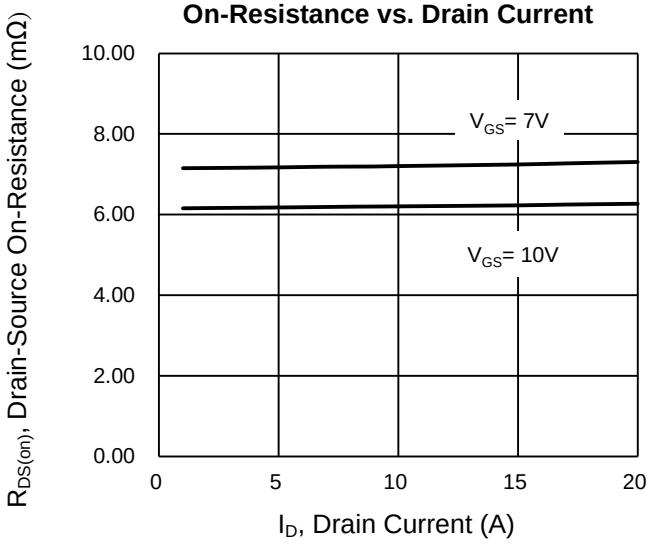
Output Characteristics



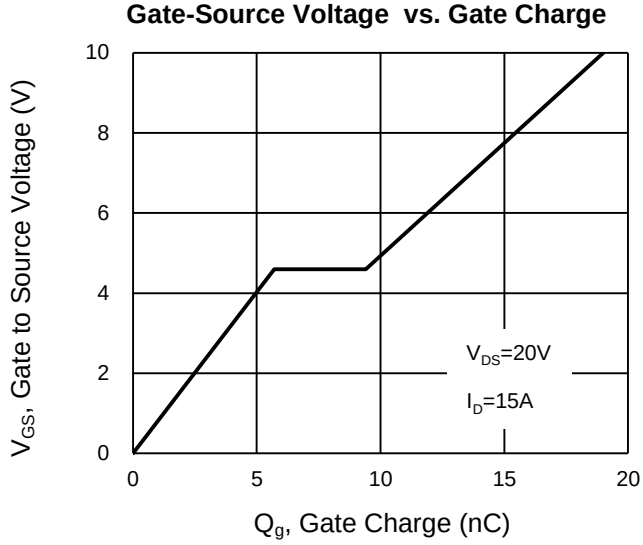
Transfer Characteristics



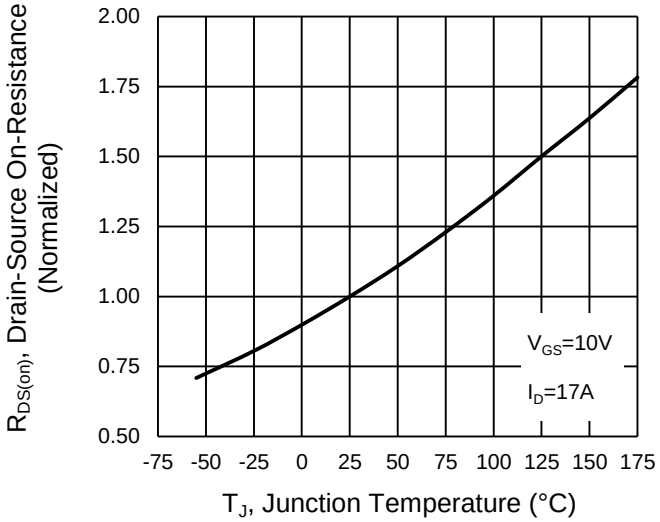
On-Resistance vs. Drain Current



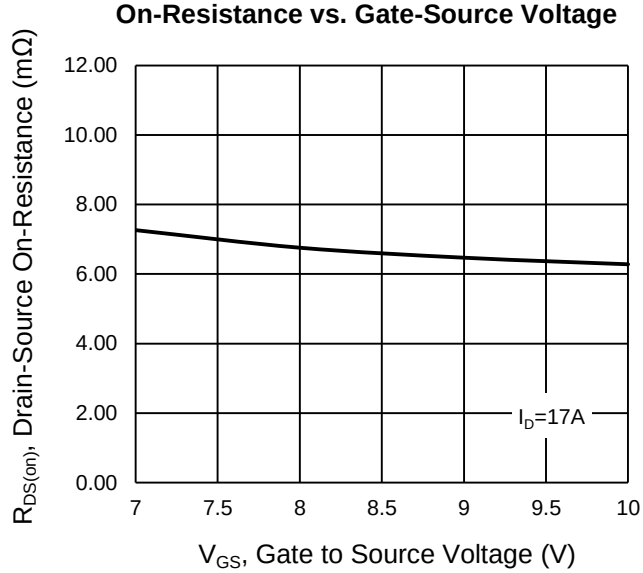
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



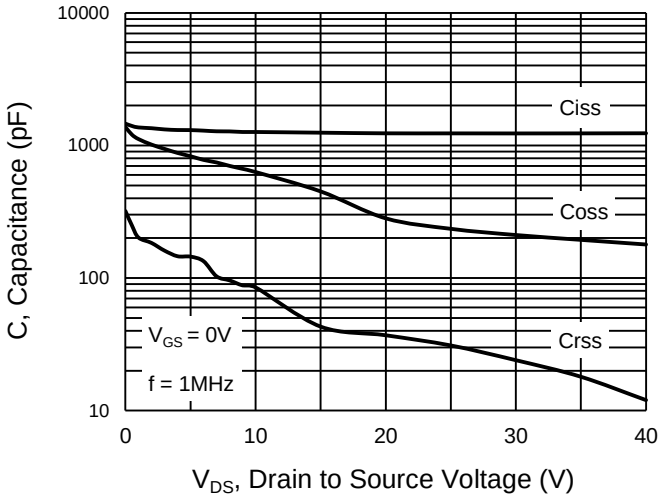
On-Resistance vs. Gate-Source Voltage



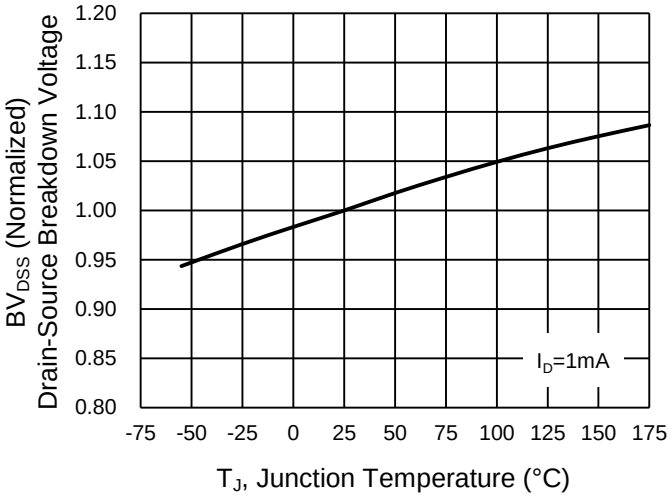
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

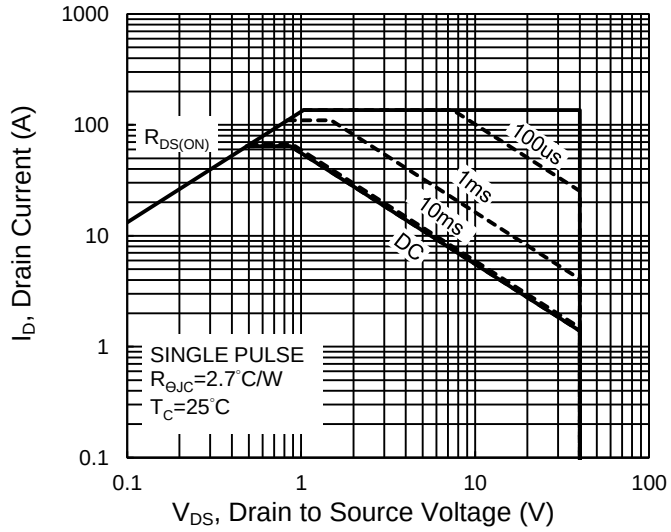
Capacitance vs. Drain-Source Voltage



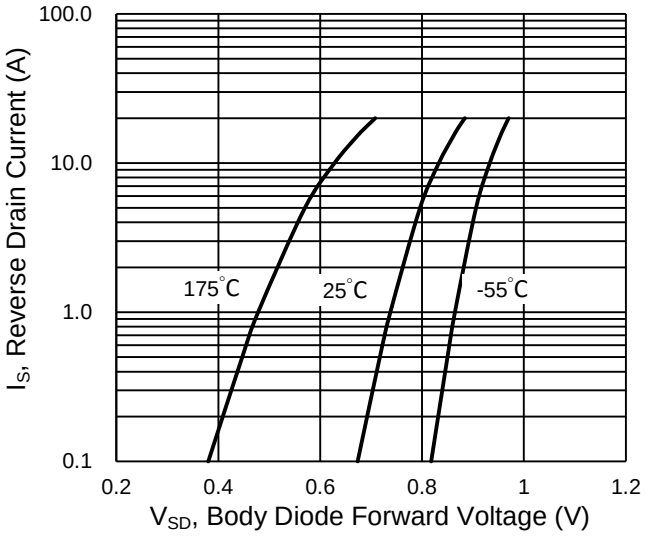
BV_{DSS} vs. Junction Temperature



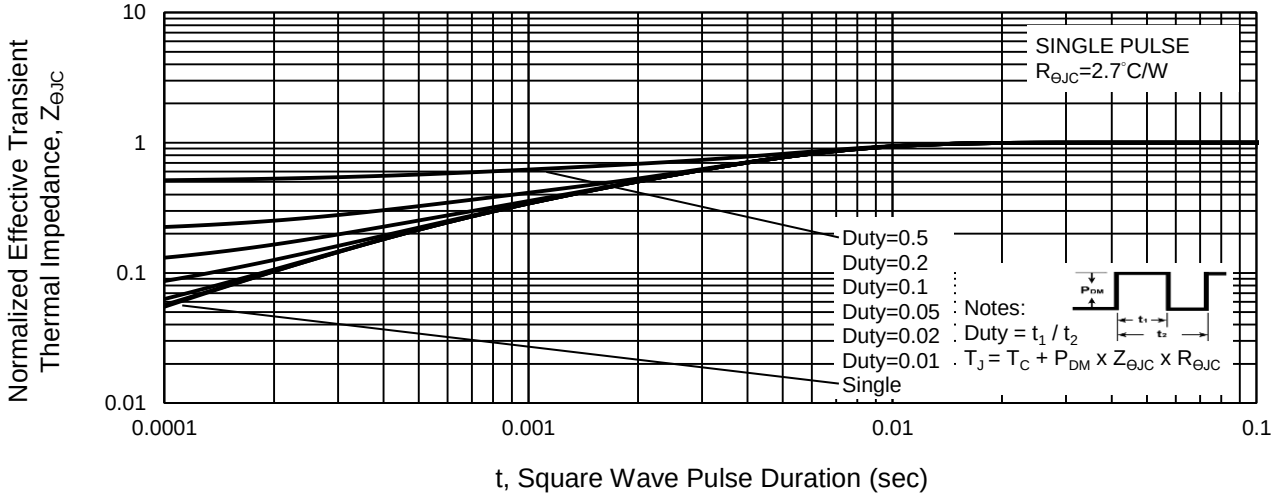
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



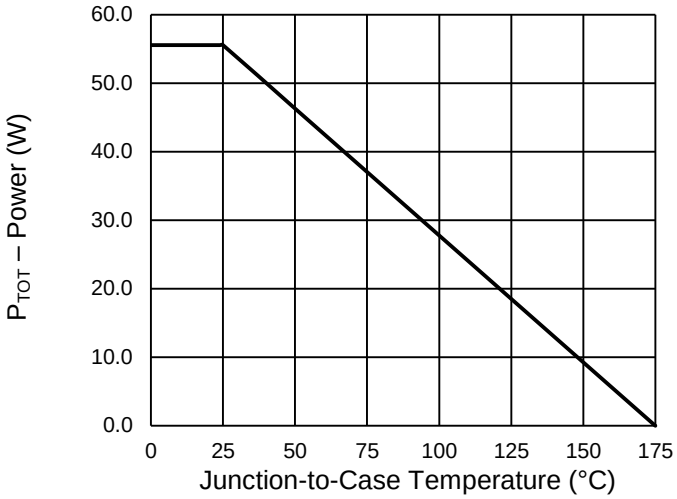
Normalized Thermal Transient Impedance, Junction-to-Case



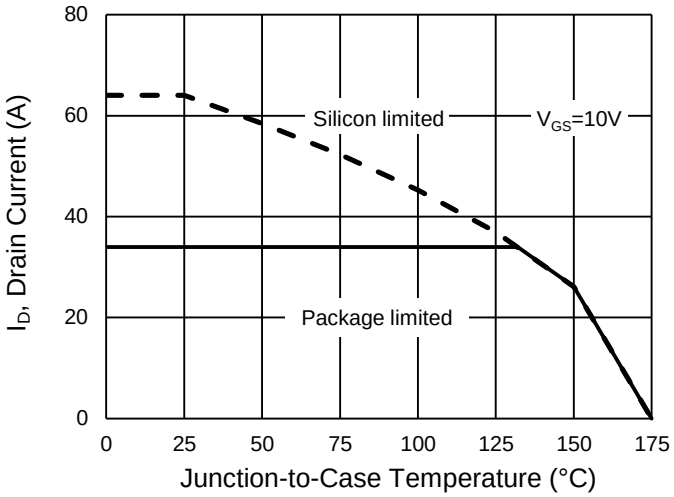
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

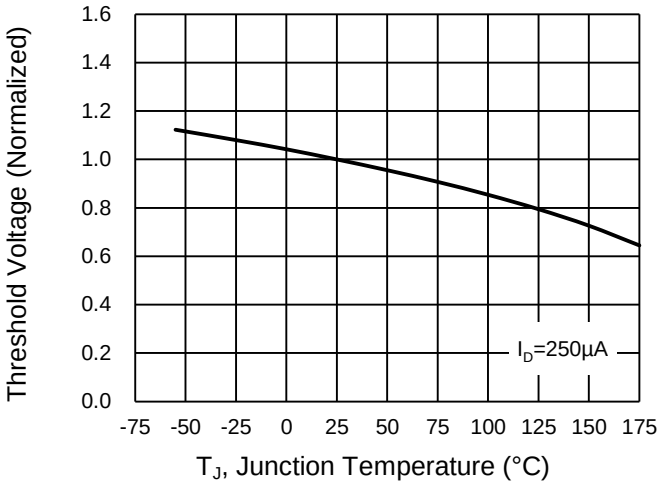
Power Dissipation



Drain Current

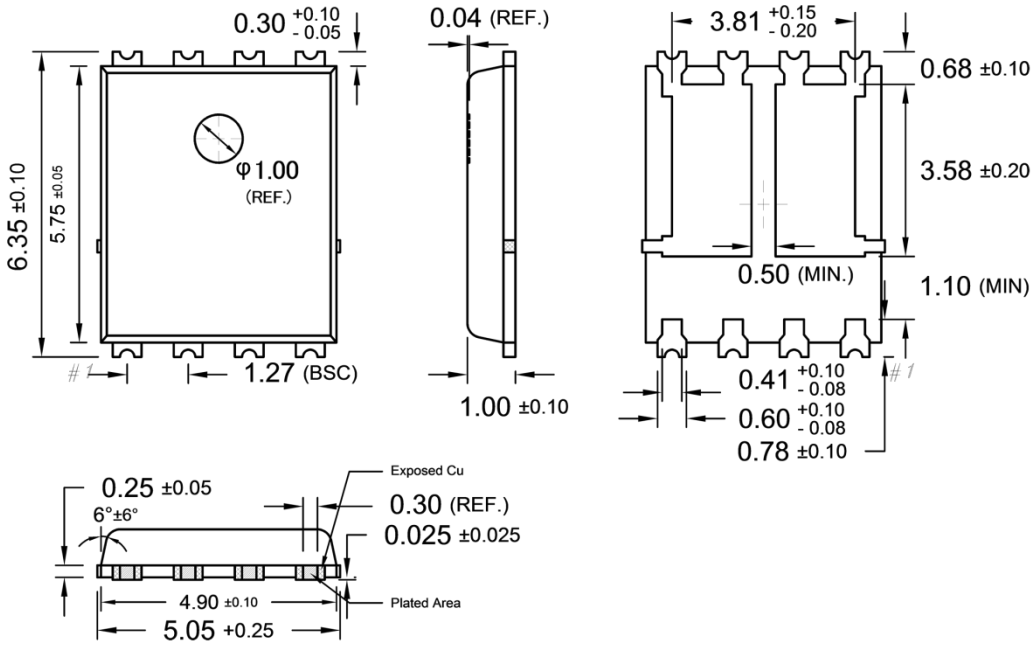


Normalized gate threshold voltage vs Temperature

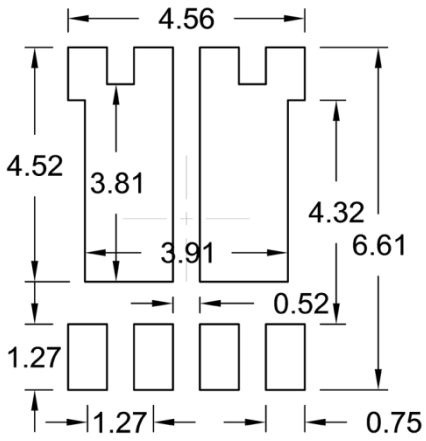


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

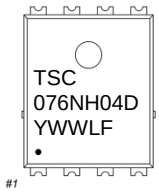
PDFN56U Dual



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Purchasers are solely responsible for the choice, selection, and use of TSC products and TSC assumes no liability for application assistance or the design of Purchasers' products.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.