Reference Design:

HFRD-18.0

Rev. 7; 11/09

REFERENCE DESIGN

High-Frequency XFP Host Board

(Includes Integrated RS-232 to I^2C Conversion)

Maxim Integrated Products

Reference Design: High-Frequency XFP Host Board

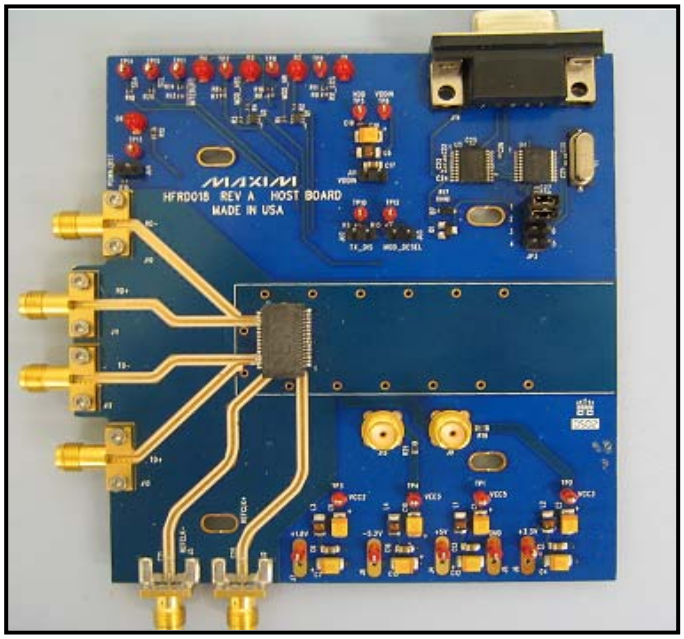
Table of Contents

1 Overview

High Frequency Reference Design (HFRD) 18.0 is an XFP host board designed on Rogers 3003 material. The host board can be used to test XFP fiber optic/copper transceiver modules in a clean test environment to more accurately define the modules' performance. The host board also includes an RS-232 to I^2C conversion controller to simplify communication and control of the XFP modules from a computer.

HFRD-18.0 provides micro-strip transmission lines and SMA connectors for transmitted and received data. Jumpers and LED's are used for monitoring and changing the low-speed digital I/O. Connections to the module board are made through a 30-pin XFP connector.

HFRD- 18.0



1.1 Features

- XFP MSA Compliant
- Documentation/Test Data
- SMA Connectors for High-Speed data
- Integrated RS-232 to I^2C Converter
- Schematics and Bill of Materials Provided
- Gerber Files Available

2 Obtaining Additional Information

Limited quantities of the XFP transmitter board (HFRD-18.0) are available. For more information about the reference design or to obtain an XFP host board please email to: https://support.maxim-ic.com/.

3 Reference Design Details

HFRD-18.0 was engineered to test fiber optic/ copper transceivers that comply with the XFP Multisource Agreement (MSA). The XFP MSA sets guidelines for the package outline, pin function, I/O interface and other aspects of the module design as well as the host board requirements and interface parameters. By complying with the standard, modules are mechanically and functionally interchangeable.

The HFRD-18.0 XFP host board is designed to simulate an ideal environment for XFP module testing using Rogers material and single-ended micro-strip transmission lines. These properties make the host board as electrically transparent as possible, allowing a more accurate assessment of the modules' actual performance. SMA connectors, jumpers and status LEDs are provided to simplify the testing and interfacing of XFP modules.

HFRD-18.0 also integrates an RS-232 to I^2C converter to provide software access and control of the modules memory, diagnostic and status information. Additionally, resistor jumpers can be placed to control/monitor the low speed digital control signals (LOS, TX_DISABLE, etc.) with a computer through the RS-232 serial port and the appropriate software.

The HFRD-18.0 RS232 to I^2C converter is compatible with software written for the DS3900 (see section 6.2). The HFRD-18.0 reference design can therefore be used with existing software that is often provided by Dallas Semiconductor for their XFP controller ICs. For more information on writing software for use with this reference design, see application note 206: *Using a PC's RS-232 Serial Port To Communicate with 2-Wire Devices*. Note: The microcontroller is pre-programmed with the firmware listed in the application note.

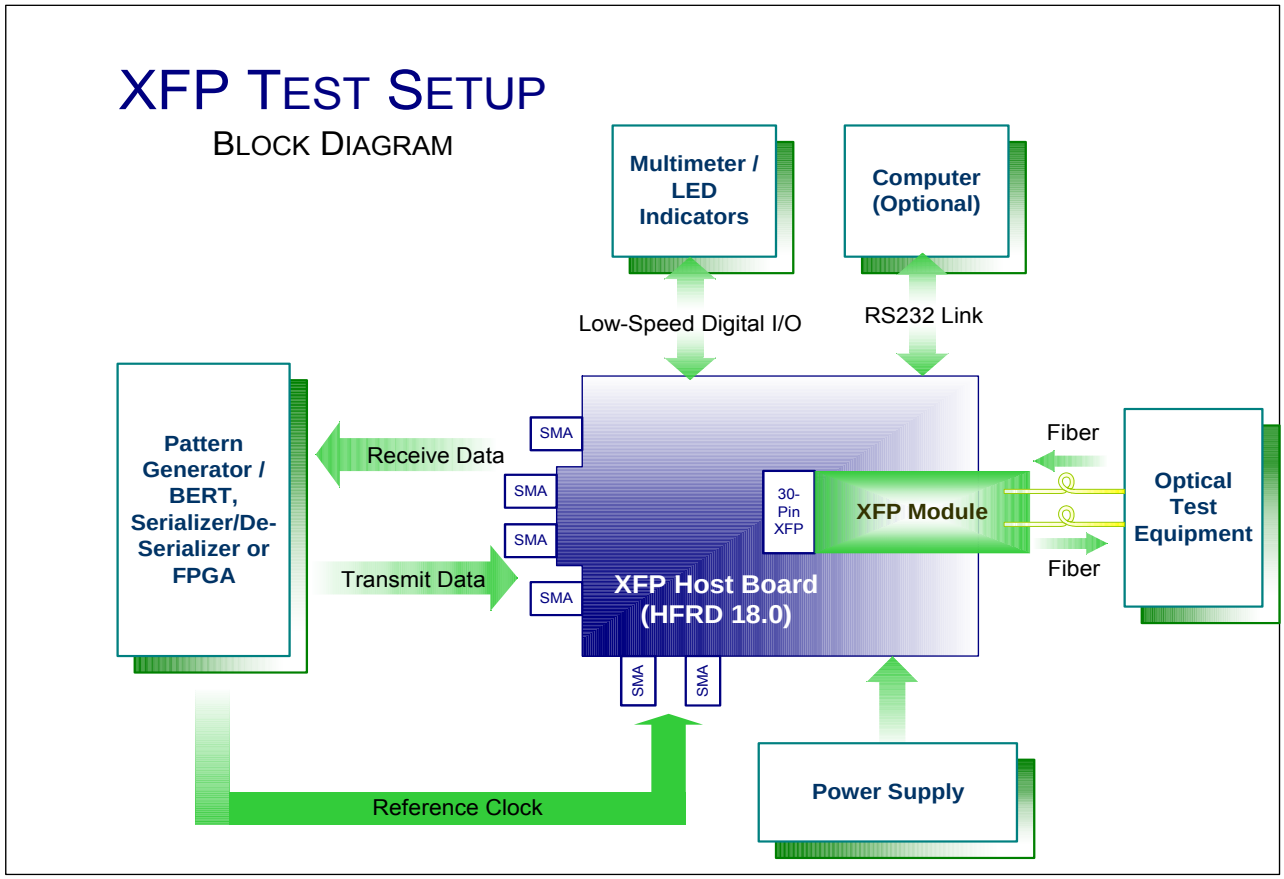


Figure 1. XFP Test Setup (Block Diagram)

4 Typical Reference Design Performance

(Typical values are measured at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Transmission line Characteristic Impedance	Z	Odd Mode Impedance	50 ±10%	Ω
Differential S11 Magnitude (Notes 1, 2)		f < 7.5GHz (notes 1, 2)	-10	dB
		f < 10GHz (notes 1, 2)	-5	
S21 f_{3dB} Point	f_{3dB}	Notes 1, 3	8	GHz
S21 f_{6dB} Point	f_{6dB}	Notes 1, 3	11	GHz

Note 1: S-Parameter measurements were made using a four-port network analyzer operating in differential mode.
Note 2: Measured at RD- and RD+ or TD+ and TD-SMA connections. Measurement includes the XFP connector with a 50Ω termination at end of an XFP adaptor test board (Figure 2).
Note 3: S21 measurement path includes the transmission loss added by the adaptor test board.

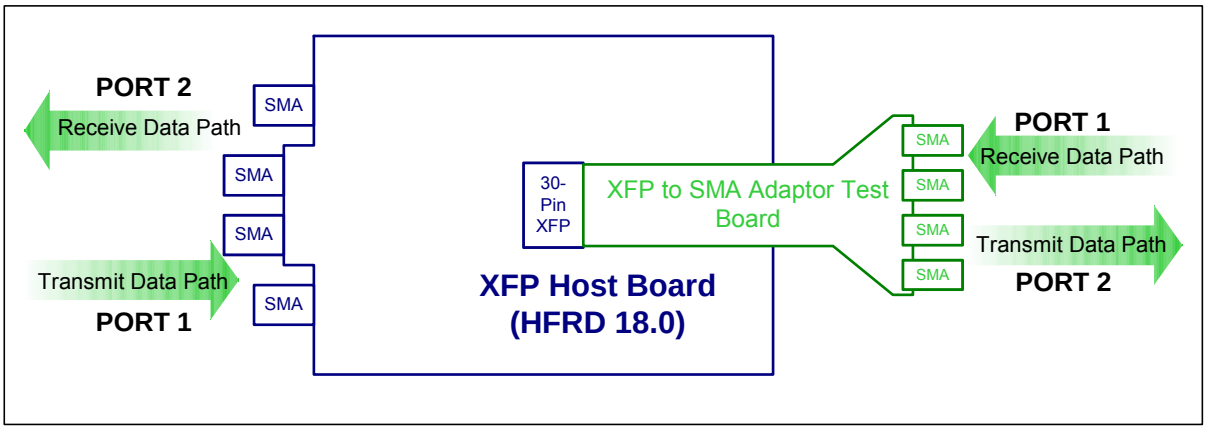


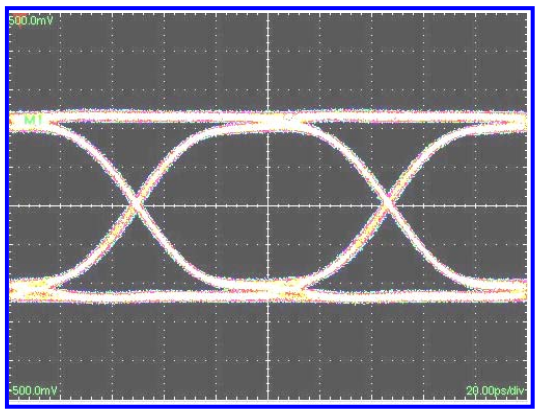
Figure 2. S11 and S21 Measurement Setup

5 Reference Design Characteristic Graphs

(Eye diagram was generated using a pattern generator input signal and an XFP to SMA adaptor test board.)

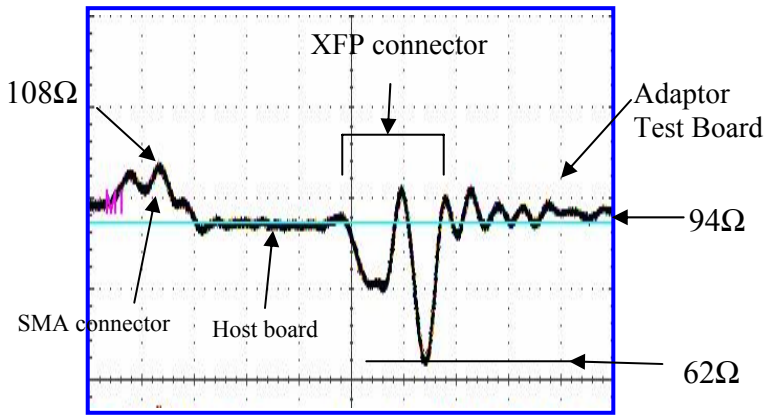
EYE DIAGRAM

(10.3125Gbps, Transmit or Receive Data Path)



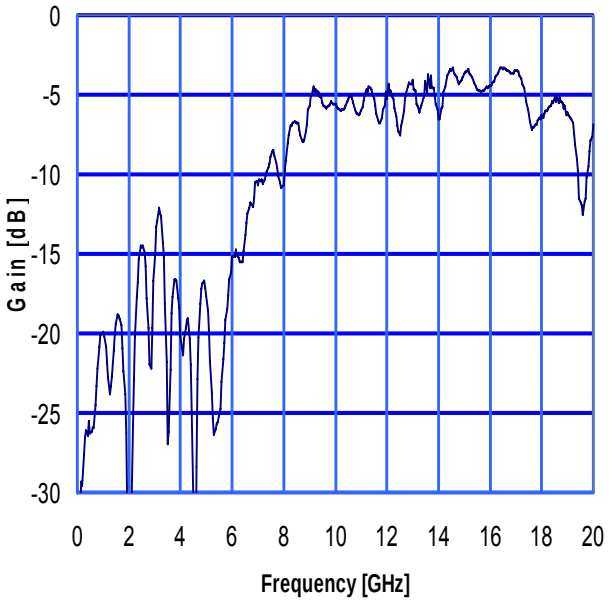
TDR

(Transmit or Receive Data Path)



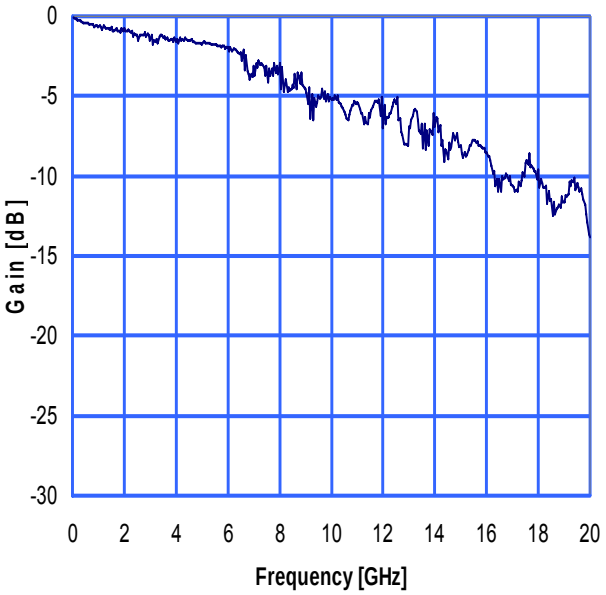
Differential S11 Magnitude

(Measured at Transmit or Receive Data ports)



Differential S21 Magnitude

(Measured on Transmit or Receive Data Path)



6 Application Information

6.1 Status LEDs

Status LEDs are connected to the low-speed output signals from the XFP module. (RX_LOS, MOD_NR, MOD_ABS, INT_BAR) The LED will illuminate when the signal is asserted. See sections 7 and 8 for more information.

6.2 DS3900 Compatibility

The DS3900 is a serial to I^2C converter developed by Dallas Semiconductor. The DS3900 is frequently used for programming digital potentiometer and controller ICs that are often used in optical modules. HFRD-18.0 uses similar hardware and the same firmware as the DS3900 for the serial to I^2C conversion. Therefore, the same software that was used with the DS3900 to control digital diagnostic ICs can be used with the HFRD 18.0 XFP host board.

6.3 Layout Considerations

Single-ended transmission lines (with a taper to differential near the XFP connector) are designed on the XFP host board. Changing the PCB layer profile (see Section 12) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

6.4 Supply Filter

The host board is required to provide power supply decoupling for transmitter and receiver supply voltages. HFRD-18.0 is designed with the recommend filters as per the XFP MSA.

7 I/O and Control Description

Component	NAME	FUNCTION
J2	REFCLK+	Reference Clock Non-Inverted Input, SMA Connector
J3	REFCLK-	Reference Clock Inverted Input, SMA Connector
J4	+5V	+5V Supply. Connect a +5V supply to J4.
J5	GND	Supply Ground
J6	+3.3V	+3.3V Supply. Connect a +3.3V supply to J6.
J7	+1.8V	+1.8V Supply. Connect a +1.8V supply to J7.
J8	-5.2V	-5.2V Supply. Connect the optional -5.2V supply to J8.
J9/J15		Optional V_{CC} SMA connections for 3.3 and 5.2 volts.
J10	RD-	Received Data Inverted Output, SMA Connector
J11	RD+	Received Data Non-Inverted Output, SMA Connector
J12	TD-	Transmitted Data Inverted Input, SMA Connector
J13	TD+	Transmitted Data Non-Inverted Input, SMA Connector
JU1		Placing a shunt on JU1 connects the digital power connections (V_{DDIN}) to the +3.3V supply voltage.
JU2	TX_DIS	Placing a shunt on JU2 enables the XFP module.
JU3	MOD_DESEL	Leaving JU3 open allows the XFP module to respond to the 2-Wire interface commands.
JU4	P_DOWN/RST	Leaving JU4 open places the module in power down mode. Placing the jumper will cause the device to operate in normal mode.
JP3		Micro programming jumper. ***For normal operation position 1/8 and 2/7 should be connected. Position 3/6 should be open***. Position 4/5 may be open or short.
D1	RX_LOS	LED illuminates when RX_LOS asserts.
D2	MOD_NR	LED illuminates when MOD_NR asserts.
D3	MOD_ABS	LED illuminates when MOD_ABS asserts.
D4	$\overline{\text{INTERRUPT}}$	LED illuminates when $\overline{\text{INTERRUPT}}$ asserts.
D6		Led blinks when communication is established between the PC and the Host board.
TP5	V_{DDIN}	+3.3V Host Board Digital Supply Voltage. Use JU1 to connect V_{DDIN} to +3.3V supply.
TP7	MOD_ABS	Monitoring Test Point for MOD_ABS signal.
TP8	MOD_NR	Monitoring Test Point for MOD_NR signal.
TP9	RX_LOS	Monitoring Test Point for RX_LOS signal.
TP11	$\overline{\text{INTERRUPT}}$	Monitoring Test Point for $\overline{\text{INTERRUPT}}$ signal.
TP12	MOD_DESEL	Test point for MOD_DESEL signal
TP14	SDA	Test Point for SDA signal. This test point can be used to apply and read the SDA signal to the module or monitor the SDA signal when using the DS3900.
TP15	SCL	Test Point for SCL signal. This test point can be used to apply the SCL signal to the module or monitor the SCL signal when using the DS3900.

8 XFP Signal Definitions (30-Pin XFP Connector, J1)

I/O Direction assumes the XFP module as the reference. See XFP MSA section 2.3: *Pin Definitions* for the official definitions and more detailed information.

Connector Pin (J1)	I/O Type	NAME	Definition
1, 7, 15, 16, 19, 23, 26, 27, 30		GND	Module Ground
2		VEE5	Optional -5.2V Power Supply Connection
3	LVTTL INPUT	MOD_DESEL	Module De-select. Asserting this pin to a logic zero allows the module to respond to 2-wire serial interface commands.
4	LVTTL OUTPUT	$\overline{\text{INTERRUPT}}$	$\overline{\text{INTERRUPT}}$. When asserted, Indicates the presence of an important condition that can be read over the 2-Wire serial interface (Note 1).
5	LVTTL INPUT	TX_DIS	Transmitter Disable. When high the transmitter optical output is disabled.
6		VCC5	+5V Power Supply Connection
8, 9		VCC3	+3.3V Power Supply Connection
10	LVTTL INPUT	SCA	2-Wire Serial Interface Clock Line (Note 1)
11	LVTTL INPUT / OUTPUT	SDA	2-Wire Serial Interface Bi-Directional Data Line (Note 1)
12	LVTTL OUTPUT	MOD_ABS	Module Absent. Indicates that the module is not present. MOD_ABS is connected to GND inside the module (Note 1).
13	LVTTL OUTPUT	MOD_NR	Module Not Ready. Indicates there is an operational fault in the module (Note 1).
14	LVTTL OUTPUT	RX_LOS	Receiver Loss of Signal. Indicates the received optical power has dropped below a defined level. (Note 1)
17	CML OUTPUT	RD-	Inverted Received Data Output
18	CML OUTPUT	RD+	Non-Inverted Received Data Output
20, 22		VCC2	+1.8V Power Supply Connection
21	LVTTL INPUT	P_Down/RST	Power Down. Module is required to limit power consumption to 1.5W or below when this pin is high. 2-Wire serial interface must be functional in power down mode. Reset. The falling edge initiates a complete reset of the XFP module including the serial interface. Equivalent to a power cycle.
24	PECL INPUT	REFCLK+	Non-Inverted Reference Clock Input, AC-coupled on host board.
25	PECL INPUT	REFCLK-	Inverted Reference Clock Input, AC-coupled on host board.
28	CML INPUT	TD-	Inverted Transmitter Data Input
29	CML INPUT	TD+	Non-Inverted Transmitter Data Input

Note 1: Open collector outputs that must be pulled high (+3 to +3.6V) on host board through a 4.7kΩ to 10kΩ resistor.

9 Component List

Reference	Qty	Value	Description
C1-2 C4 C7 C9-10 C12 C15	8	22uF	TANTALUM CAPACITOR (B CASE)
C19	1	10uF	TANTALUM CAPACITOR (B CASE)
C3 C8 C11 C14 C18 C20-21 C22 C26-27	10	0.1uF	CERAMIC CAPACITOR (0402)
C5-6 C13 C16-17	5	0.1uF	CERAMIC CAPACITOR (0805)
C23-25 C28	4	1uF	CERAMIC CAPACITOR (0402)
C29-30	2	27pF	CERAMIC CAPACITOR (0402)
D1-4 D6	5		LED RED T1 PKG DIGIKEY 160-1078-ND
D7	1		MA2YD15 PANASONIC (DIODE MINITYPE2)
J1	1		XFP 30 PIN RECEPTICAL TYCO 788862-1
J2-3	3		SMA SIDE MOUNT TAB CONTACT JOHNSON 142-0701-851
J10-13	4		ROSENBERGER 32K243-40M
J9 J15	2		SMA PCB MOUNT JOHNSON 142-701-231
J14	1		NORCOMP 182-009-212-161 (DB9-HF)
JP3	1		HEADER 2 X 4 0.1" SPACING DIGIKEY S1012-36-ND
JU1-4	4		JUMPER BLOCK, 2 PINS 0.1" SPACING
L1-4 L6	5	4.7uH	CHIP INDUCTOR (1008) TAIYO YUDEN CBC32254R7M
Q1	1		MOSFET 2N7002 (SOT23)
R1-4 R12	5	301	RESISTOR (0402)
R5 R7-9 R13 R15-16 R19 R21	9	0	RESISTOR (0402)
R6 R10-11 R14 R18 R20	6	10K	RESISTOR (0402)
R17	1	2.21K	SURFACE MOUNT RESISTOR (0603)
TP1-15 J4-J8	20		TESTPOINT DIGI-KEY 5000K-ND
U1-2	2		FAIRCHILD NC7WZ04P6X DUAL INVERTER
U4	1		PIC16F628-04I/SS (SSOP20)
U3	1		MAX3223EAP (SSOP20)
Y1	1		CTX501-ND CRYSTAL 3.68MHZ
JP3 JU1-4	7		SHUNTS DIGI-KEY S2000

10 Schematic

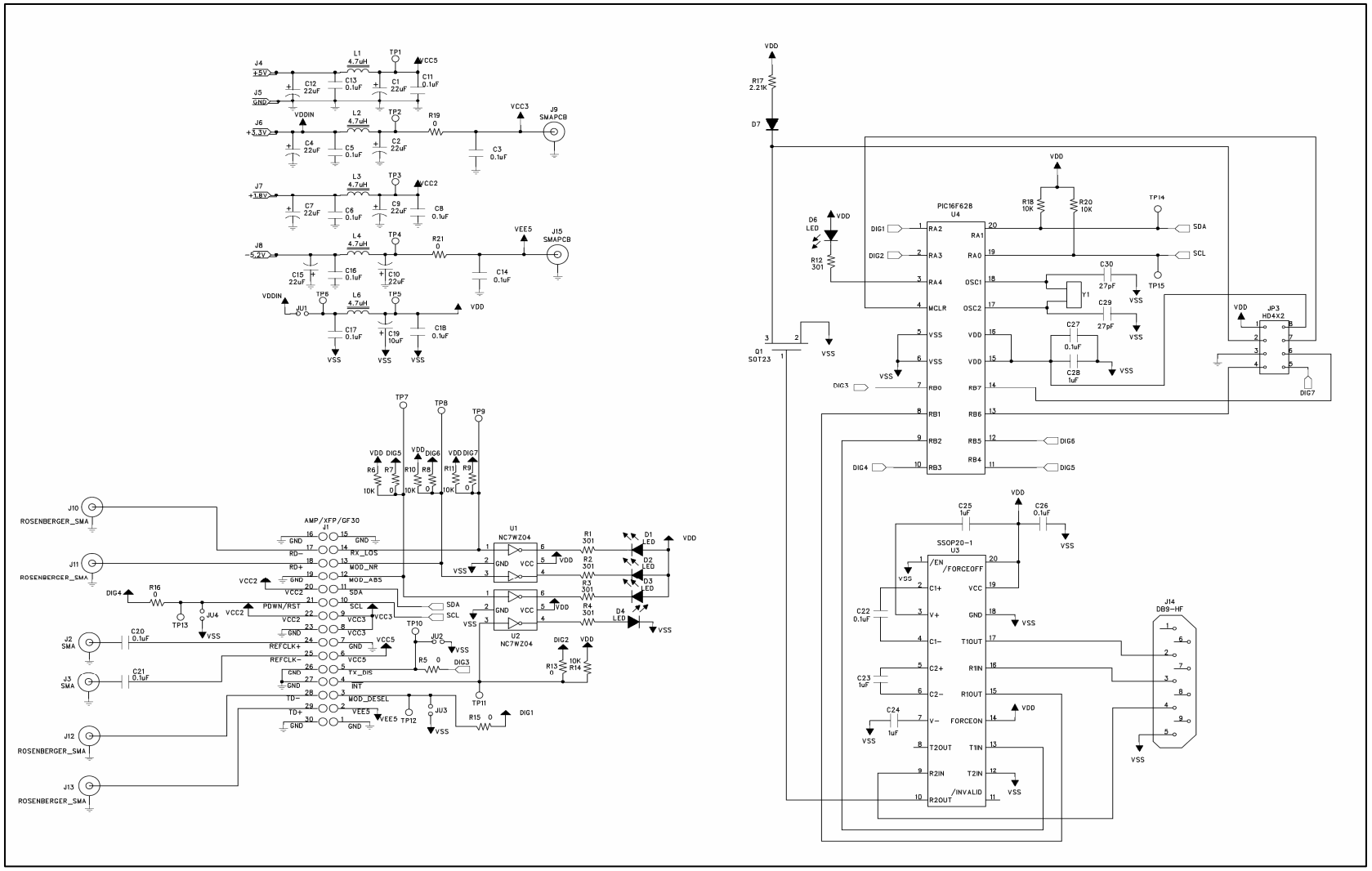


Figure 3. HFRD-18.0 XFP Host Board Schematic

11 Board Dimensions/Layout

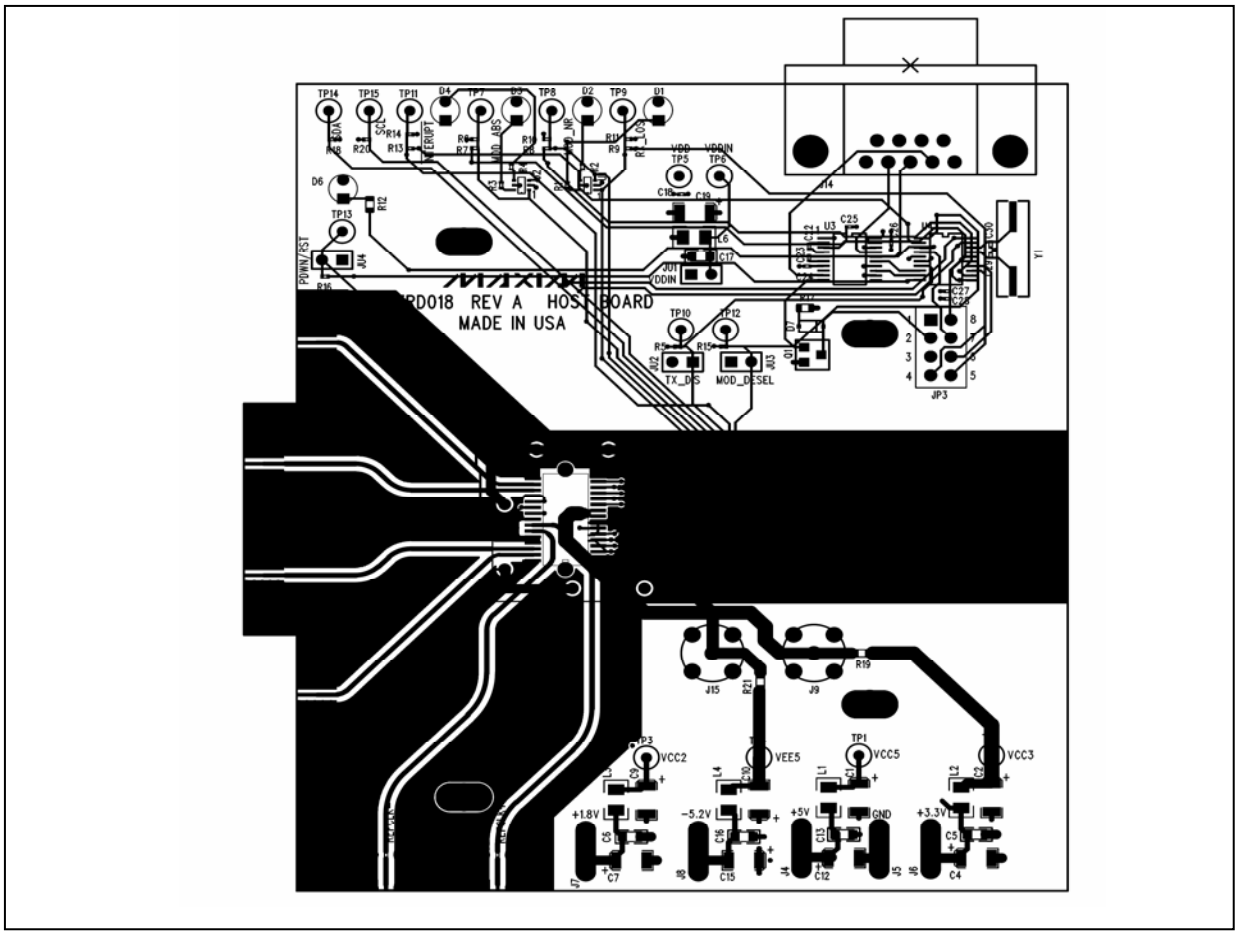


Figure 4. Host Board Dimensions/Layout

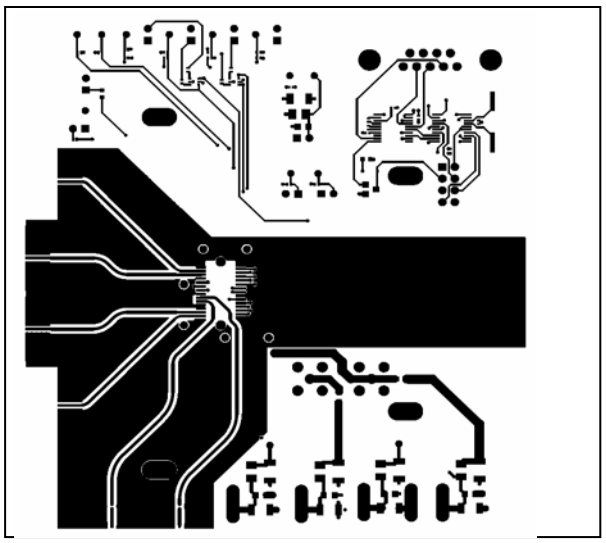


Figure 5. PC Board Layout–Component Side

Figure 6. PC Board Layout–Ground Plane

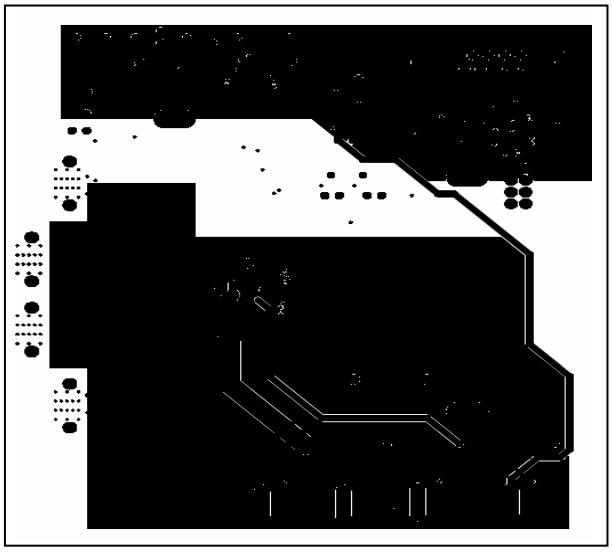


Figure 7. PC Board Layout–Power Plane

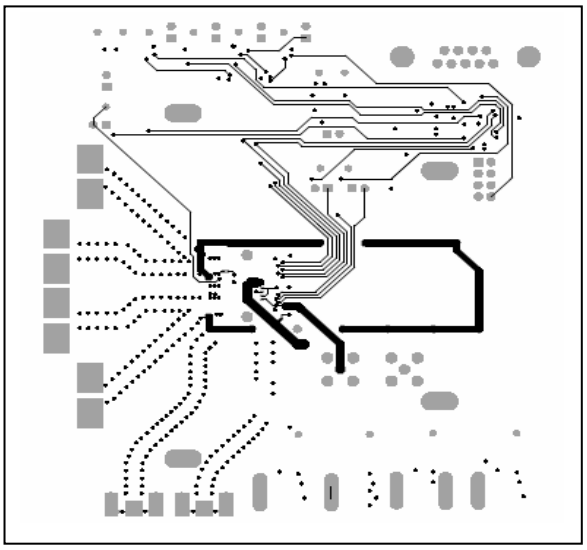


Figure 8. PC Board Layout–Solder Side

12 Layer Profile

The HFRD-18.0 XFP host board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is Rogers 3003 with a dielectric constant of ~3
2. 1oz copper foil

	SINGLE ENDED	COUPLED
A	26mil	20mil
B	> 50mil	12mil
C	10mil	20mil
D	As Needed	As Needed

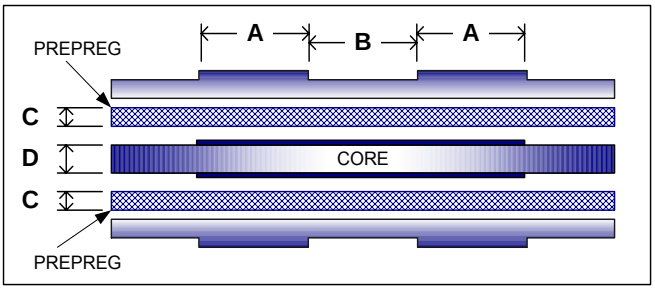


Figure 9. Layer Profile