PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-MID/13/8157
Dated 28 Oct 2013

MANUFACTURING IMPROVEMENTS APPLIED TO LEOPARD FAMILY

Table 1. Change Implementation Schedule

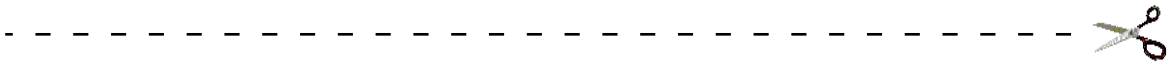
Forecasted implementation date for change	15-May-2014
Forecasted availability date of samples for customer	09-Dec-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Apr-2014
Estimated date of changed product first shipment	15-Jul-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	SPC56xxx family
Type of change	Waferfab additional location
Reason for change	Corporate Process Roadmap
Description of the change	Qualification of Crolles as additional diffusion plant and qualification of CuPd wire bonding in Malta. See details.
Change Product Identification	Dedicated marking traceability on products and labels
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APG-MID/13/8157**
Please sign and return to STMicroelectronics Sales Office	**Dated 28 Oct 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

.....

.....

.....

.....

.....

.....

.....

.....

DOCUMENT APPROVAL

Name	Function
Duncan, Martin Russell	Marketing Manager
Brambilla, Daniele Alfred	Product Manager
Mervic, Alberto	Q.A. Manager

MANUFACTURING IMPROVEMENTS APPLIED TO LEOPARD FAMILY

WHAT:

In order to meet the forecasted increase of demand for CMOSM10 products (90 nm), we are going to put in place the following initiatives:

1) activate Crolles 12” plant as a second and high volumes manufacturing source beside Rousset R8 8” . The above manufacturing plant activation has been already communicated through PCN APG-MID/13/7698 issued in March 2013.

2) introduce the CuPd wire bonding as an alternative to Au wire bonding.

WHY:

Corporate Process Roadmap
On customer request the above mentioned PCNs has been split by product family keeping unchanged the overall Company strategy.

HOW:

Here attached are the qualification reports for the process test vehicles: FP50 (Pictus 512K) & FA80 (Andorra 4M).

We forecast to complete the two changes (qualification of the products in Crolles and the CuPd wire bonding) by end of Q1/2014.

Traceability will be granted by ST system. A dedicated code marked on the parts will enable to distinguish between diffusion sites (see attached document).

See below list of relevant commercial products with the changes to be applied.

WHEN:

Sampling: on customer request starting December 2013
PPAP in April 2014
Production & shipment progressively from Q2 2014

NEW BILL OF MATERIAL	
LQFP 100 14x14x1.4	**LQFP 144 20X20X1.4**
GLUE QMI9507-1A1	GLUE ABLEBOND 3280T
RESIN SUMITOMO EME-G700LS	RESIN SUMITOMO EME-G700LS
WIRE CuPd D0.7	WIRE CuPd D0.7

Involved products

	Activation of Crolles as high volume manufacturing source	Introduction of CuPd wire	Introduction of Kirkop plant as main source for QFP 64/100 pin	Introduction of Rousset as 2nd source for EWS	Design fix
SPC564L54L3x	YES	YES			
SPC564L60L3x	YES	YES			
SPC56EL54L3x	YES	YES			
SPC56EL60L3x	YES	YES			
SPC564L64L3x	YES	YES			
SPC564L70L3x	YES	YES			
SPC56EL64L3x	YES	YES			
SPC56EL70L3x	YES	YES			
SPC564L54L5x	YES	YES			
SPC564L60L5x	YES	YES			
SPC56EL54L5x	YES	YES			
SPC56EL60L5x	YES	YES			
SPC564L64L5x	YES	YES			
SPC564L70L5x	YES	YES			
SPC56EL64L5x	YES	YES			
SPC56EL70L5x	YES	YES			

PCN APG-MRD/13/8157
Leopard Family Ordering Code and Marking info

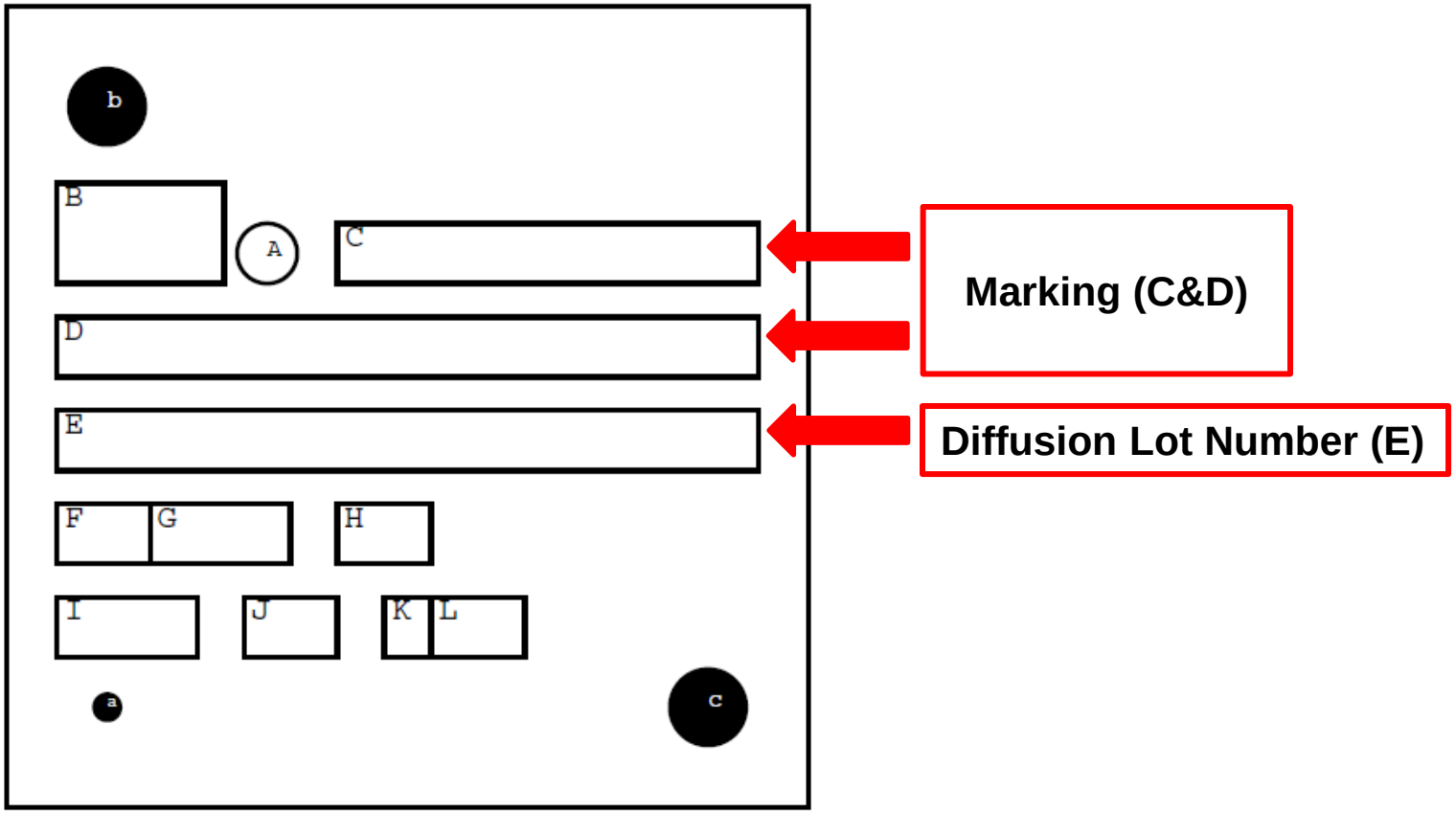
APG

MRD Microcontroller

life.augmented

Marking Detail

PACKAGE FACE : TOP



Leopard 1M info Cut3.2 Crolles with CuPd

	Leopard 1M Cut3.1 (Rousset Au)	Leopard 1M Cut3.2 (Crolles CuPd)
Ordering code	SPC564L54L3BCFQR	
Finish Good code	64L54L3B8CFQR000	64L54L3B**B**CFQR000
Silicon code	FL60CBG	FL60C**C**Q
Diff Lot Number (E)	VG------	V**Q**------
Marking (C)	CB-Q	C**C**-Q
Marking (D)	SPC564L54L3	SPC564L54L3

	Leopard 1M Cut3.1 (Rousset Au)	Leopard 1M Cut3.2 (Crolles CuPd)
Ordering code	SPC564L60L3BCOQR	
Finish Good code	64L60L3B8COQR000	64L60L3B**B**COQR000
Silicon code	FL60CBG	FL60C**C**Q
Diff Lot Number (E)	VG------	V**Q**------
Marking (C)	CB-Q	C**C**-Q
Marking (D)	SPC564L60L3	SPC564L60L3

	Leopard 1M Cut3.1 (Rousset Au)	Leopard 1M Cut3.2 (Crolles CuPd)
Ordering code	SPC564L60L5BCOQR	
Finish Good code	64L60L5B8COQR000	64L60L5B**B**COQR000
Silicon code	FL60CBG	FL60C**C**Q
Diff Lot Number (E)	VG------	V**Q**------
Marking (C)	CB-Q	C**C**-Q
Marking (D)	SPC564L60L5	SPC564L60L5

Leopard 2M codes for Cut 2.0 Crolles with CuPd

	Leopard 2M Cut2.0 (Rousset Au)	Leopard 2M Cut2.0 (Crolles CuPd)
Ordering code	SPC56EL70L5CBZY	
Finish Good code	6EL70L5B9CBZY000	6EL70L5B**A**CBZY000
Diff Lot Number (E)	VG------	V**Q**------
Silicon code	FL62BAG	FL62BA**Q**
Marking (C)	BA-S	BA-S
Marking (D)	SPC56EL70L5	SPC56EL70L5

Red digit: *differentiation for new silicon cut*

Reliability Report
Andorra 4M
FAB transfer

General Information	
Product Line	*FA80*
Product Description	*Andorra 4M cut 3.0*
Commercial Product	SPC564A80
Product Group	*APG*
Product division	*MID*
Silicon process technology	*CMOS M10*

Locations	
Wafer fab location	*Crolles 2*

Final Assessment	
Reliability assessment	*Qualification Passed as per Q100 rev G grade 1*

DOCUMENT HISTORY

Version	Date	Author	Comment
1.0	30/04/2013	M. De Tomasi	First Document release

RELEASED DOCUMENT

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the reliability trials results of Andorra 4M Cut 3.0 qualification.

Andorra 4M cut 3.0 is processed in Crolles FAB using CMOS M10 (90 nm) technology and it is assembled in Malta-ST assy line for LQFP176 package with gold wire.

The M10 (90nm technology) process was qualified in Rousset R8 Fab in wk922 using three logic test chips and a Flash test chip as test vehicles. Andorra 4M cut 2.0 was qualified in Rousset in Q1 2011.

Considering that Andorra4M is the first M10 product with 6 metal layers and FLS Flash diffused in Crolles, no similarity with other qualified products could be considered.

The qualification exercise will be based on 3 diffusion lots coming from Crolles: assy reports required on all qualification lots.

The qualification exercise is in respect of Q100 rev G specification.

1.2 Conclusions

All qualification trials have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.

Package oriented tests have not put in evidence any criticality.

On the ground of the overall positive results we can conclude that Andorra 4M cut 3.0 in LQFP176 can be qualified in accordance to AEC-Q100 Grade1 RevG.

2 TRACEABILITY

2.1 Wafer fab information

DIE FEATURES	
Diffusion Site	*Crolles 2*
Wafer Diameter (inches)	12
Process Technology	*CMOS M10*
Passivation	PSG - Nit UV
Die finishing back side	Lapped Silicon

2.2 Package outline/Mechanical data

	LQFP 176
Package Description	*LQFP 176 24x24x1.4*
Assembly Site	*ST KIRKOP – MALTA*
Die Attach material	ABLEBOND 3280T
Molding compound	SUMITOMO EME-G700LS
Substrate/Leadframe	LQFP 176L 24SQ RgAg
Wires bonding materials/diameters	WIRE Au 2N GPG2 D0.9

2.3 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	:	ST KIRKOP – MALTA
Tester	:	Teradyne J750

3 RELIABILITY PLAN AND TESTS RESULTS

3.1 Conditions

Room test temperature is 25°C
Hot test temperature is 150°C
Cold test temperature is -40°C

3.2 Tables entry legend

Symbol	How to read
☐	Action or condition has not to be considered
☒	The action/condition has been done/applied during the trial
N.P.	The trial or readout is not in the Qualification Plan and thus has not been performed

3.3 Accelerated Environmental Stress Test (Q100 Group A)

Test			Step	RESULTS			Notes
N	TEST NAME	CONDITIONS [SPEC]		LOT 1	LOT 2	LOT 3	
1	**Pre Conditioning MSL 3**	[J-STD-020] ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ 100 Temperature Cycles 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp	**Pre**	0/231	0/231	0/231	
			Post	0/231	0/231	0/231	
2	**THB** Temperature Humidity Bias	[JESD22-A101/A110] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold Ta=85°C, 85%RH, 1000hrs	**500 hrs**	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	
3	**AC** Autoclave	[JESD22-A102/A118] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold P=2.08atm Ta=121°C, 96hrs	**96 hrs**	0/77	0/77	0/77	
4	**TC** Temperature Cycling	[JESD22-A104] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post Ta=-50°C /+150 °C 1000 cyc	**500 cyc**	0/77	0/77	0/77	
			1000 cyc	0/77	0/77	0/77	

5	**PTC** Power Temperature Cycle	[JESD22-A105] ☐ After Jedec PC MSL3 ☐ Testing at Room ☐ Testing at Hot ☐ Testing at Cold Ta=-40°C /+125 °C 1000 cyc	**1000 cyc**	N.P.	N.P.	N.P.	**Not required on Andorra 4M**
6	**HTSL** High Temperature Storage Lifetime	[JESD22-A103] Ta= 150ºC 1000hrs (*2000hrs monitoring*)	**1000 hrs**	N.P.	N.P.	N.P.	**See HTDR trial**

3.4 Accelerated Lifetime Simulation Test (Q100 Group B)

Test			Step	Results			Notes
N	TEST NAME	CONDITIONS [SPEC]		Lot 1	Lot 2	Lot 3	
1	**HTOL** High Temp. Operating Life	[JESD22-A108] ☒ After Jedec PC MSL3 ☒ After 1k W/E cyc @125°C ☒ Testing at Room, Hot, Cold ☒ Drift Analysis on Key parameters at Room, Hot, Cold Ta=125ºC, Tj=150°C VDD+20% 1000hrs	**168 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	
2	**ELFR** Early Life Failure Rate	[AEC Q100-008] ☒ Testing at Room, Hot, Cold Ta= 125ºC, Tj=150°C, 24+24hrs	**24hrs**	0/77	0/77	0/77	
			48hrs	0/77	0/77	0/77	
3	**HTDR** High Temp. Data Retention	[AEC Q100-005] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ After 1k W/E cyc @125°C ☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 2000hrs	**168 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	
			2000 hrs	0/77	0/77	0/77	
4.a	**FET @25°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 25ºC 100k Write/Erase cyc	**10k cyc**	0/77	N.P.	N.P.	
			50k cyc	0/77	N.P.	N.P.	
			100k cyc	0/77	N.P.	N.P.	
4.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	0/77	N.P.	N.P.	
5.a	**FET @125°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 125ºC 100k Write/Erase cyc	**10k cyc**	0/77	0/77	0/77	
			50k cyc	0/77	0/77	0/77	
			100k cyc	0/77	0/77	0/77	
5.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	0/77	0/77	0/77	

6.a	**FET @-40°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= -40ºC 100k Write/Erase cyc	**10k cyc**	N.P.	0/77	N.P.	
			50k cyc	N.P.	0/77	N.P.	
			100k cyc	N.P.	0/77	N.P.	
6.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	0/77	N.P.	
7	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 1k W/E cyc @25°C Ta= 60ºC, All0 Pattern 2000hrs	**500 hrs**	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
8	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 10k W/E cyc @25°C Ta= 60ºC, All0 Pattern 2000hrs	**500 hrs**	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
9	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 100k W/E cyc @25°C Ta= 60ºC, All0 Pattern 2000hrs	**500 hrs**	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
10	**Flip Bit**	[AEC Q100-005] ☒ Vth Drift Analysis After 1 W/E cyc @25°C Ta= 25ºC, Chk Pattern 1000hrs	**168 hrs**	N.P.	0/77	N.P.	
			500 hrs	N.P.	0/77	N.P.	
			1000 hrs	N.P.	0/77	N.P.	
11	**Read Disturb**	After 10 W/E cyc @25°C Ta= 25ºC; 4,5V Stress <1ppm after 6000hrs with ECC	**Final**	N.P.	0/77	N.P.	
12	**Read Disturb**	After 10k W/E cyc @25°C Ta= 25ºC; 4,5V Stress <1ppm after 1 sec with ECC	**Final**	N.P.	N.P.	0/77	

3.5 Package Assembly Integrity Test (Q100 Group C)

Test			Step	Results			Notes
N	TEST NAME	CONDITIONS [SPEC]		LQFP176	LQFP144	LQFP100	
1	**WBS** Wire Bond Shear	[AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices	**Final result**	Done	Done	Done	Assy report
2	**WBP** Wire Bond Pull	[MIL-STD883 method 2011] 30 bonds x 5 devices	**Final result**	Done	Done	Done	Assy report
3	**SD** Solderability	[JEDEC JEDES22-B102] > 95% lead coverage	**Final result**	Done	Done	Done	Assy report
4	**PD** Physical Dimension	[JEDEC JEDES22-B100 and B108]	**Final result**	Done	Done	Done	Assy report
5	**SBS** Solder Ball Shear	[AEC Q100-010]	**Final result**	N.A.	N.A.	N.A.	Not applicable
6	**LI** Lead Integrity	[JEDEC JEDES22-B105]	**Final result**	N.A.	N.A.	N.A.	Not applicable

3.6 Die Fabrication Reliability Test (Q100 Group D)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
1	**EM** Electromigration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
2	**TDDB** Time Dependent Dielectric Breakdown	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
3	**HCI** Hot Carrier Injection	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
4	**NBTI** Negative Bias Temperature Instability	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
5	**SM** Stress Migration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification

3.7 Electrical Verification Test (Q100 Group E)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS [AEC Q100]			
1.a	**ESD HBM**	HBM = 2kV	**Final result**	**PASSED**	
1.b	**ESD MM**	MM = 200V	**Final result**	**PASSED**	
1.c	**ESD CDM**	CDM = 500V / 750V corner only	**Final result**	**PASSED**	
2.a	**LU**	Class II - Level A (+/- 100mA)	**Final result**	**PASSED**	
2.b	**LU**	Class II - Level A (1,5 x Vmax)	**Final result**	**PASSED**	
3	**ED** Electrical Distribution	[AEC Q100-009] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	DONE	
4	**FG** Fault Grading	[AEC Q100-007] FG shall be = or > 90% for qual units	**Final result**	DONE by Similarity	Andorra 4M cut 2.0
5	**CHAR** Characterization	[AEC Q103] Performed on new technologies and part families. ☐ Testing at Room ☐ Testing at Hot ☐ Testing at Cold	**Final result**	N.P.	Not required by Q100
6	**GL** Electrothermally-Induced Gate Leakage	[AEC Q100-006] Test before and after GL at room temperature within 96hours of GL stress completion	**Final result**	DONE	
7	**EMC** Electromagnetic Compatibility	[SAE J1752/3 – radiated Emission]	**Final result**	N.P.	Not required by Q100
8	**SC** Short Circuit Characterization	[AEC Q100-012] Applicable to all smart power devices. This test and statistical evaluation shall be performed per agreement between user and supplier on a case-by-case basis.	**Final result**	N.A.	Not applicable to Microcontroller
9	**SER** Soft Error Rate	[JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3] Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed	**Final result**	DONE	

3.8 Defect Screening Test (Q100 Group F)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
1	**PAT** Process Average testing	[AEC Q101]	**Final result**	IMPLEMENTED	
2	**SBA** Statistical Bin/Yield Analysis	[AEC Q102]	**Final result**	IMPLEMENTED	

Reliability Report
Pictus 512K
Fab Transfer

General Information	
Product Line	*FP50xx*
Product Description	*Pictus 512k cut 3.5*
Commercial Product	*SPC560P50xx, SPC560P44xx*
Product Group	*APG*
Product division	*MID*
Silicon process technology	*CMOS M10*

Locations	
Wafer fab location	*Crolles 2*

Final Assessment	
Reliability assessment	**Qualification Passed as per Q100 rev G grade 1**

DOCUMENT HISTORY

Version	Date	Author	Comment
0.1	29/01/2013	L. Cola	First document draft
0.5	07/02/2013	L. Cola	First document release with preliminary results available
0.6	22/02/2013	L. Cola	Document Format review
1.0	26/06/2013	R. Enrici Vaion	Cut3.5 qualification strategy
1.1	1/07/2013	R. Enrici Vaion	General Information updated

RELEASED DOCUMENT

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the reliability trials results achieved on Pictus 512k Cut 3.4 and Cut 3.5 qualification exercise, in order to release the device to production volume in Crolles.

Pictus 512k is processed in Crolles2 FAB using CMOS M10 (90 nm) technology and it is assembled in Malta-ST assy in LQFP144 package.

Pictus 512k embeds the ST Flash module.

Considering that Pictus 512K is the first M10 product with 4 metal layers and ST Flash diffused in Crolles, no similarity with other products could be considered.

The qualification exercise is based on three diffusion lots of Cut 3.4 coming from Crolles2.

Pictus512k Cut3.5, diffused in Crolles, is qualified by similarity taking into account results achieved with Rousset silicon Pictus 512K cut 3.5 (RR003612AG6050), being a pure design fix independent on process transfer.

Package qualification has been run on one assembly lot using similarity with qualification done on Rousset silicon on Pictus 512K and Bolero512K products, considering that from Back End point of view the differences between Rousset and Crolles Fab have to be considered minor.

The qualification exercise for this new product is in respect of Q100 revG.

1.2 Conclusions

Qualification trials have been completed with positive results on Cut3.4. Neither functional nor parametric rejects were detected at final electrical testing.

Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.

Package trials with Au-wire concluded with positive results.

Pictus 512k Cut3.5 is qualified by similarity without any additional trial required.

2 TRACEABILITY

2.1 Wafer fab information

DIE FEATURES	
Diffusion Site	*Crolles 2*
Wafer Diameter (inches)	12
Process Technology	*CMOS M10*
Passivation	PSG - Nit UV
Die finishing back side	Lapped Silicon

2.2 Package outline/Mechanical data

	LQFP 144
Package Description	*LQFP 144 20x20x1.4*
Assembly Site	*ST KIRKOP – MALTA*
Die Attach material	GLUE ABLEBOND 3280T
Molding compound	SUMITOMO EME-G700LS
Substrate/Leadframe	LQFP 144L RgAg
Wires bonding materials/diameters	WIRE Au 2N GPG2 D0.9

2.3 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	**:**	ST KIRKOP – MALTA
Tester	**:**	Teradyne J750

3 RELIABILITY PLAN AND TESTS RESULTS

3.1 Conditions

Room test temperature is 25°C
Hot test temperature is 125°C
Cold test temperature is -40°C

3.2 Tables entry legend

Symbol	How to read
☐	Action or condition has not to be considered
☒	The action/condition has been done/applied during the trial
N.P.	The trial or readout is not in the Qualification Plan and thus has not been performed

3.3 Environmental stress test (Q100 group A)

Test			Step	Notes	
N	TEST NAME	CONDITIONS [SPEC]		LQFP144	
1	**PC Pre-Conditioning** **MSL 3**	[J-STD-020] ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☐ 100 Temperature Cycles 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp	**Pre**	0/77 x3 x1 Pictus 512K Crolles 0/77 x 3 x 1 Pictus 512K Rousset 0/77 x 3 x 2 Bolero 512K Rousset	Similarity with Pictus 512K and Bolero 512K diffused in Rousset and assembled in Malta
			Post	0/77 x3 x1 Pictus 512K Crolles 0/77 x 3 x 1 Pictus 512K Rousset 0/77 x 3 x 2 Bolero 512K Rousset	
2	**THB** Temperature Humidity Bias	[JESD22-A101/A110] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold Ta=85°C, 85%RH, 1000hrs	**500 hrs**	0/77 Pictus 512K Crolles 0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	Similarity with Pictus 512K and Bolero 512K diffused in Rousset and assembled in Malta
			1000 hrs	0/77 Pictus 512K Crolles 0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	

3	**AC** Autoclave	[JESD22-A102/A118] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☐ Die visual inspection post trial P=2.08atm Ta=121°C, 96hrs	**96 hrs**	0/77 Pictus 512K Crolles 0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	Similarity with Pictus 512K and Bolero 512K diffused in Rousset and assembled in Malta
4	**TC** Temperature Cycling	[JESD22-A104] ☒ AfterJedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post *Ta=-65°C /+150 °C 500 cyc Ta=-50°C /+150 °C 1000 cyc	**500 cyc**	*0/77 Pictus 512K Crolles 0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	Similarity with Pictus 512K and Bolero 512K diffused in Rousset and assembled in Malta
			1000 cyc	0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	
5	**PTC** Power Temperature Cycling	[JESD22-A105] ☐ AfterJedec PC MSL3 ☐ Testing at Room ☐ Testing at Hot ☐ Testing at Cold Ta=-40°C /+125 °C 1000 cyc	**1000 cyc**	N.P.	Not required on Pictus512K
6	**HTSL** High Temperature Storage Lifetime	[JESD22-A103] ☐ AfterJedec PC MSL3 ☐ After 100 TC ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☐ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☐ Die visual inspection post trial ☐ Die cross section post trial *Ta= 175ºC 336hrs *(500hrs monitor)* Ta= 150ºC 1000hrs	**336 hrs**	*0/77 Pictus 512K Crolles	Similarity with Pictus 512K and Bolero 512K diffused in Rousset and assembled in Malta
			500hrs	*0/77 Pictus 512K Crolles 0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	
			1000hrs	0/77 Pictus 512K Rousset 0/77 x 2 Bolero 512K Rousset	

3.4 Lifetime stress test (Q100 Group B)

Test			Step	Results			Notes
N	TEST NAME	CONDITIONS [SPEC]		Lot 1	Lot 2	Lot 3	
1	**HTOL** High Temp. Operating Life	[JESD22-A108] ☒ After Jedec PC MSL3 ☐ After 100 TC ☒ After 1k W/E cyc @125°C ☒ Testing at Room, Hot, Cold ☒ Drift Analysis on Key parameters at Room, Hot, Cold Ta=125ºC, Tj=150°C VDD+20% 1000hrs	**0 hrs**	0/77	0/77	0/77	
			168 hrs	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	
2	**ELFR** Early Life Failure Rate	[AEC Q100-008] ☒ Testing at Room, Hot, Cold Ta= 125ºC, Tj=150°C, 48 hrs	**48hrs**	0/800	0/800	0/800	
3	**HTDR** High Temp. Data Retention	[AEC Q100-005] ☒ After Jedec PC MSL3 ☒ After 1k W/E cyc @125°C ☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 1000hrs (*2000hrs monitoring*)	**0 hrs**	0/77	0/77	0/77	
			168 hrs	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	
			2000 hrs	0/77	0/77	0/77	
4.a	**FET @25°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 25ºC 100k Write/Erase cyc	**10k cyc**	0/77	0/77	0/77	
			50k cyc	0/77	0/77	0/77	
			100k cyc	0/77	0/77	0/77	
4.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	0/77	0/77	0/77	

Test			Step	Results			Notes
N	TEST NAME	CONDITIONS [SPEC]		Lot 1	Lot 2	Lot 3	
5.a	**FET @125°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 125ºC 100k Write/Erase cyc	**10k cyc**	0/77	N.P.	N.P.	
			50k cyc	0/77	N.P.	N.P.	
			100k cyc	0/77	N.P.	N.P.	
5.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	0/77	N.P.	N.P.	
6.a	**FET @-40°C**	[AEC Q100-005] ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= -40ºC 100k Write/Erase cyc	**10k cyc**	0/77	N.P.	N.P.	
			50k cyc	0/77	N.P.	N.P.	
			100k cyc	0/77	N.P.	N.P.	
6.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	0/77	N.P.	N.P.	
7	**LTDR** Low Temp. Data Retention	[AEC Q100-005] After 1k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs (*2000hrs monitoring*)	**0 hrs**	0/77	N.P.	N.P.	
			500 hrs	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
8	**LTDR** Low Temp. Data Retention	[AEC Q100-005] After 10k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs (*2000hrs monitoring*)	**0 hrs**	0/77	N.P.	N.P.	
			500 hrs	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
9	**LTDR** Low Temp. Data Retention	[AEC Q100-005] After 100k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs (*2000hrs monitoring*)	**0 hrs**	0/77	N.P.	N.P.	
			500 hrs	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	
			2000 hrs	0/77	N.P.	N.P.	
10	**Flip Bit**	[AEC Q100-005] After 1 W/E cyc @25°C Ta= 25ºC, Chk Pattern 1000hrs	**0 hrs**	0/77	N.P.	N.P.	
			168 hrs	0/77	N.P.	N.P.	
			500 hrs	0/77	N.P.	N.P.	
			1000 hrs	0/77	N.P.	N.P.	

Test			Step	Results			Notes
N	TEST NAME	CONDITIONS [SPEC]		Lot 1	Lot 2	Lot 3	
11.a	**Read Disturb**	After 10 W/E cyc @125°C Ta= 25ºC; 4,5V Stress 220hrs	**Final**	0/77	N.P.	N.P.	
11.b	**Read Disturb**	After 10k W/E cyc @125°C Ta= 25ºC; 4,5V Stress 1s	**Final**	0/77	N.P.	N.P.	

3.5 Package Assembly Integrity Test (Q100 Group C)

Test			Step	Results	Notes
N	TEST NAME	CONDITIONS [SPEC]			
1	**WBS** Wire Bond Shear	[AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices	**Final result**	Done	Assy report
2	**WBP** Wire Bond Pull	[MIL-STD883 method 2011] 30 bonds x 5 devices	**Final result**	Done	Assy report
3	**SD** Solderability	[JEDEC JEDES22-B102] > 95% lead coverage	**Final result**	Done	Assy report
4	**PD** Physical Dimension	[JEDEC JEDES22-B100 and B108]	**Final result**	Done	Assy report
5	**SBS** Solder Ball Shear	[AEC Q100-010]	**Final result**	N.A.	Not applicable
6	**LI** Lead Integrity	[JEDEC JEDES22-B105]	**Final result**	N.A.	Not applicable

3.6 Die Fabrication Reliability Test (Q100 Group D)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
1	**EM** Electromigration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
2	**TDDB** Time Dependent Dielectric Breakdown	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
3	**HCI** Hot Carrier Injection	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
4	**NBTI** Negative Bias Temperature Instability	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
5	**SM** Stress Migration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification

3.7 Electrical verification test (Q100 Group E)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
1.a	**ESD HBM**	HBM = 2kV	**Final result**	**PASSED**	
1.b	**ESD MM**	MM = 200V	**Final result**	**PASSED**	
1.c	**ESD CDM**	CDM = 500V / 750V corner only	**Final result**	**PASSED**	
2.a	**LU**	Current Injection = Level B +/- 100 mA	**Final result**	**PASSED**	
2.b	**LU**	Supply Voltage = Level B 1.5xVmax	**Final result**	**PASSED**	
3	**ED** Electrical Distribution	[AEC Q100-009] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	DONE	
4	**FG** Fault Grading	[AEC Q100-007] FG shall be = or > 90% for qual units	**Final result**	DONE by Similarity	Pictus 512K Rousset
5	**CHAR** Characterization	[AEC Q103] Performed on new technologies and part families. ☐ Testing at Room ☐ Testing at Hot ☐ Testing at Cold	**Final result**	N.P.	Not required by Q100

6	**GL** Electrothermally-Induced Gate Leakage	[AEC Q100-006] Test before and after GL at room temperature within 96hours of GL stress completion	**Final result**	DONE	
7	**EMC** Electromagnetic Compatibility	[SAE J1752/3 – radiated Emission]	**Final result**	N.P.	Not required by Q100
8	**SC** Short Circuit Characterization	[AEC Q100-012] Applicable to all smart power devices. This test and statistical evaluation shall be performed per agreement between user and supplier on a case-by-case basis.	**Final result**	N.A.	Not applicable to Microcontroller
9	**SER** Soft Error Rate	[JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3] Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed	**Final result**	DONE	

3.8 Defect Screening Test (Q100 Group F)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
1	**PAT** Process Average testing	[AEC Q101]	**Final result**	IMPLEMENTED	
2	**SBA** Statistical Bin/Yield Analysis	[AEC Q102]	**Final result**	IMPLEMENTED	

4 REVISION TRACKING

Rev 1.1:

1. Added similarity for package trials in pag. 5,6
2. Added Package Assembly Integrity Test (Q100 Group C) table in page 9
3. Added die Fabrication Reliability Test (Q100 Group D) table in page 10
4.

Rev 1.0:

1. Package lot inserted in pag.4
2. Table of package trials added in pag.5,6
3: Cut 3.5 qualification strategy pag.3

Rev 0.6:

1. Format adjustment on header
2. Added Qualification ongoing statement (page 3)

Rev 0.5:

3. First document release with incomplete results available.

Rev 0.1: First document draft

SPC56 - M10 technology PCNs description

October 2013

life.augmented

ReV 4

LIST OF CHANGES

- Front End (wafer diffusion):
  - High volume manufacturing source activation: M10 process & product transfer from Rousset 8” to Crolles 12”
- EWS (electrica wafer sort):
  - Activation of second testing site in Rousset where not yet qualified
- Back End (assembly):
  - LQFP64/100 main source activation: package transfer from Muar to Malta
  - CuPd wire introduction

SPC56 32 Bit - M10 90 nm
Manufacturing Improvements

Device	Mem size	Package	C300	CuPd	Assy Muar to Malta	EWS Agr to R8	Design Fix
Pictus	256K	LQFP 64	X	X	X		
		LQFP 100	X	X	X		
		KGD + OPM					
	512K	LQFP 100	X	X	X		
		LQFP 144	X	X			
	1M	LQFP 100	X	X	X		
		LQFP 144	X	X			
Bolero	256K	QFN					
		LQFP 64	X	X	X		
		LQFP 100	X	X	X		
	512K	QFN					X
		LQFP 64	X	X	X		X
		LQFP 100	X	X	X		X
		LQFP 144	X	X			X
	1.5M	LQFP 100	X	X	X	X	X
		LQFP 144	X	X		X	X
		LQFP 176	X	X		X	X
	3M	LQFP 176	X	X			X
		LQFP 208	X	X			X
		BGA					X

Device	Mem size	Package	C300	CuPd	Assy Muar to Malta	EWS Agr to R8	Design Fix
Leopard	1M	LQFP 100	X	X			
		LQFP 144	X	X			
	2M	LQFP 100	X	X			
		LQFP 144	X	X			
		BGA 257					
Monaco	1.5M	LQFP 144	X	X			X
		LQFP 176	X	X			X
Andorra	2M	BGA 324	X				X
		LQFP 176	X	X			X
	4M	BGA 324	X				X

SPC56 32 Bit - M10 90 nm
Manufacturing Improvements master plan

2012	2013												2014												2015				2016	2017
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	Q1	Q2	Q3	Q4		

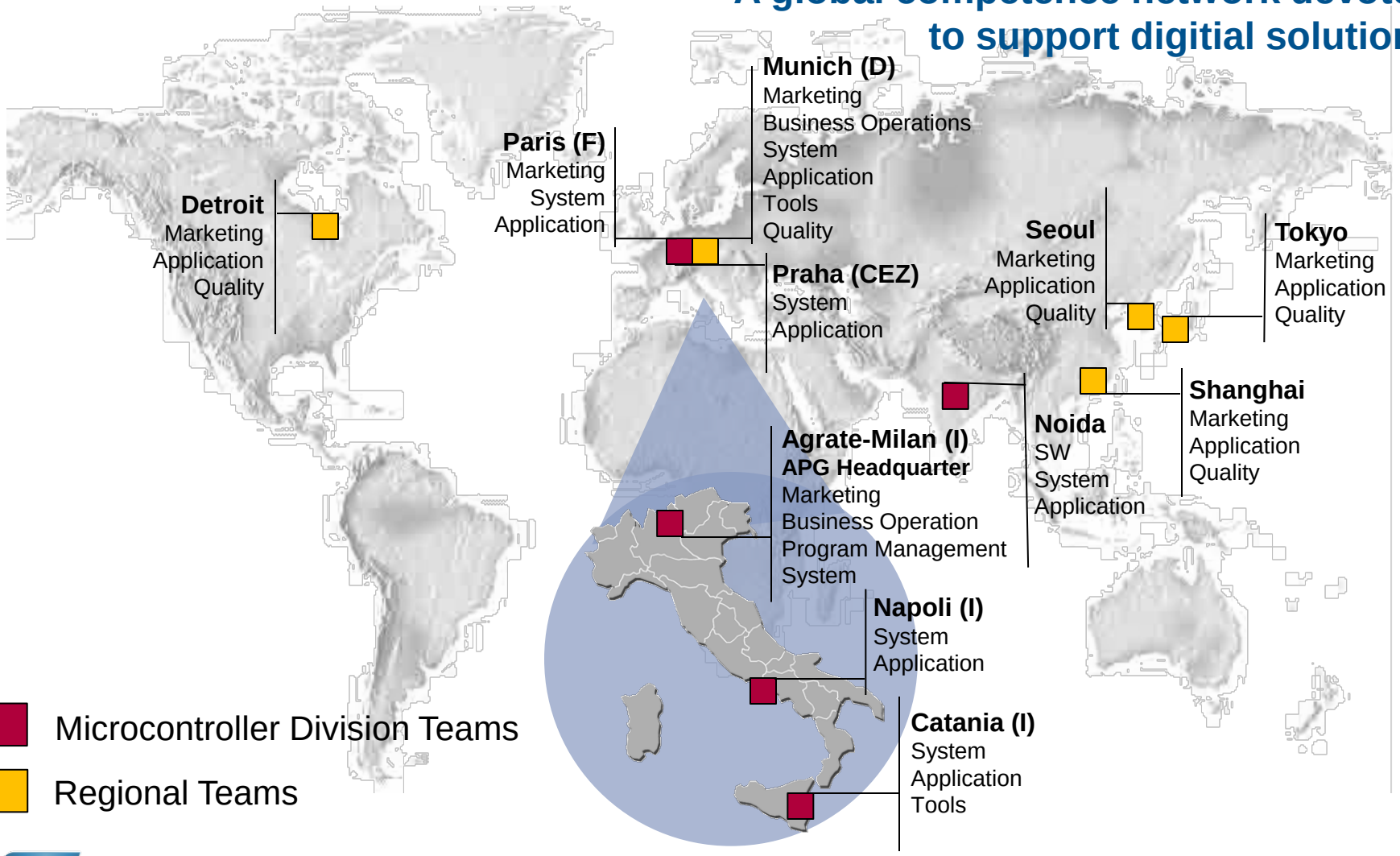
- Bolero 1.5M EWS testing in Rousset
- Pictus / Bolero LQFP 64 & 100 pin assembly in Kirkop
- Andorra BGA assembly in Kirkop

- Wafer diffusion
- CuPd wire bonding
- Bolero 1.5M EWS testing in Rousset
- Pictus / Bolero LQFP 64 & 100 pin assembly in Kirkop
- Andorra BGA assembly in Kirkop

APG – Microcontroller & ADAS Business Unit

Main Locations Sites

A global competence network devoted to support digitial solutions

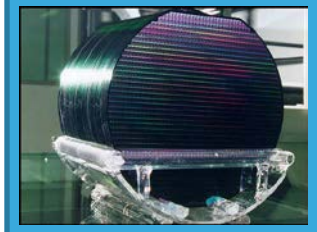


SPC56 32 Bit - M10 90 nm
Supply Chain structure

WAF

Business forecasting

WAFER MANUFACTURING



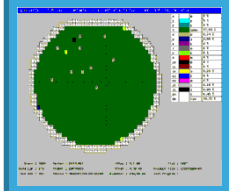
DUAL Source

90 nm:
- Rousset 8''
- Crolles 12''
- Agrate 8'' (BEOL)

55 nm:
- Crolles 12''
- *Foundry 12''*

40 nm:
- Crolles 12''
- *Foundry 12''*

EWS
electrical wafer sort



DUAL Source:

- Rousset
- Agrate

Front End

DICE

Buffer Stock

ASSY

DUAL Source:

QFP:
- Malta
- Muar
- ASE (subcon)

BGA:
- Malta
- Muar

Final Test

Double Source:

- Malta
- KYEC (subcon)

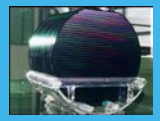
Back End

FG

Buffer stock

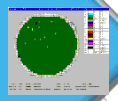
ST Manufacturing Strategy for advanced Automotive Microcontrollers is to use a main internal source and dual source capabilities (internal or subcon) to support large volumes, improve flexibility and secure business.

SPC56 32 Bit - M10 90 nm
ST Manufacturing sites - FE

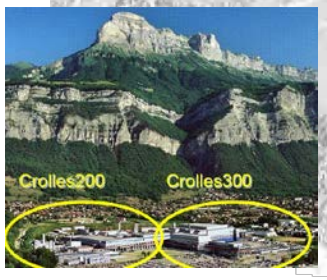


Front End
Wafer fab diffusion

EWS
Electrical Wafer Sort



Back End
Assembly
Finishing
Packing



Crolles (France) 8” & 12”

Rousset (France) 8”

Agrate (Italy) 8”

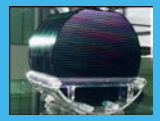
Catania (Italy) 6” & 8”

AMK (Singapore) 6” & 8”

Microcontroller manufacturing sites

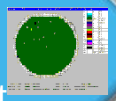
Although ST manufacturing facilities are worldwide diffused, microcontroller manufacturing is concentrated in Europe where the highest level of engineering competencies is kept by the Company

SPC56 32 Bit - M10 90 nm
ST Manufacturing sites - BE



Front End
Wafer fab diffusion

EWS
Electrical Wafer Sort



Back End
Assembly
Finishing
Packing

Grenoble (France)

Bouskoura (Marocco)

Kirkop (Malta)

Shenzhen (China)

Calamba (Philippines)

Muar (Malaysia)

Microcontroller manufacturing sites

Although ST manufacturing facilities are worldwide diffused, microcontroller manufacturing is concentrated in Europe where the highest level of engineering competencies is kept by the Company

SPC56 32 Bit - M10 90 nm Manufacturing strategy

- ST new process and product introduction strategy is to focus and stabilize industrialization and first months of production in an internal wafer fab
  - Rousset R8 8“ for 90nm eNVM process (M10)
  - Crolles 300 12“ for 55nm eNVM process (M55)

- A second wafer fab is enabled and qualified when production ramp up has been completed in the leading wafer fab and sufficient volumes are foreseen

- M10 90nm process used for the SPC56 family in Rousset R8 is now mature. To support the very high volumes expected over the next years Crolles 300 has been qualified
  - Crolles 300 (12“ wafers): M10 technology qualified. Two products already qualified.
    Product qualification end by Q1 2013

SPC56 32 Bit - M10 90 nm Manufacturing strategy

Technology	FAB A	FAB B	FAB C
BCD3	AMK6		
BCD4	AMK6	AG8	
BCD5	AMK6	AG8	
BCD6	AG8 + R2	CTN M5	
BCD8	CTN M5	AG8 + R2	
ViPM05	AMK6	CTN L1	CTN M5
ViPM07	CTN M5		
M10 (NVM 90nm)	R8	C300	R8 + R2
M55 (NVM 55nm)	C300	Foundry	
H11/H12	C300	Foundry	

Dual source strategy is applied inside ST on all technology families for automotive products thanks to in-house manufacturing capability

Secured Supply Chain

A true case study: ST managing Japan earthquake crisis

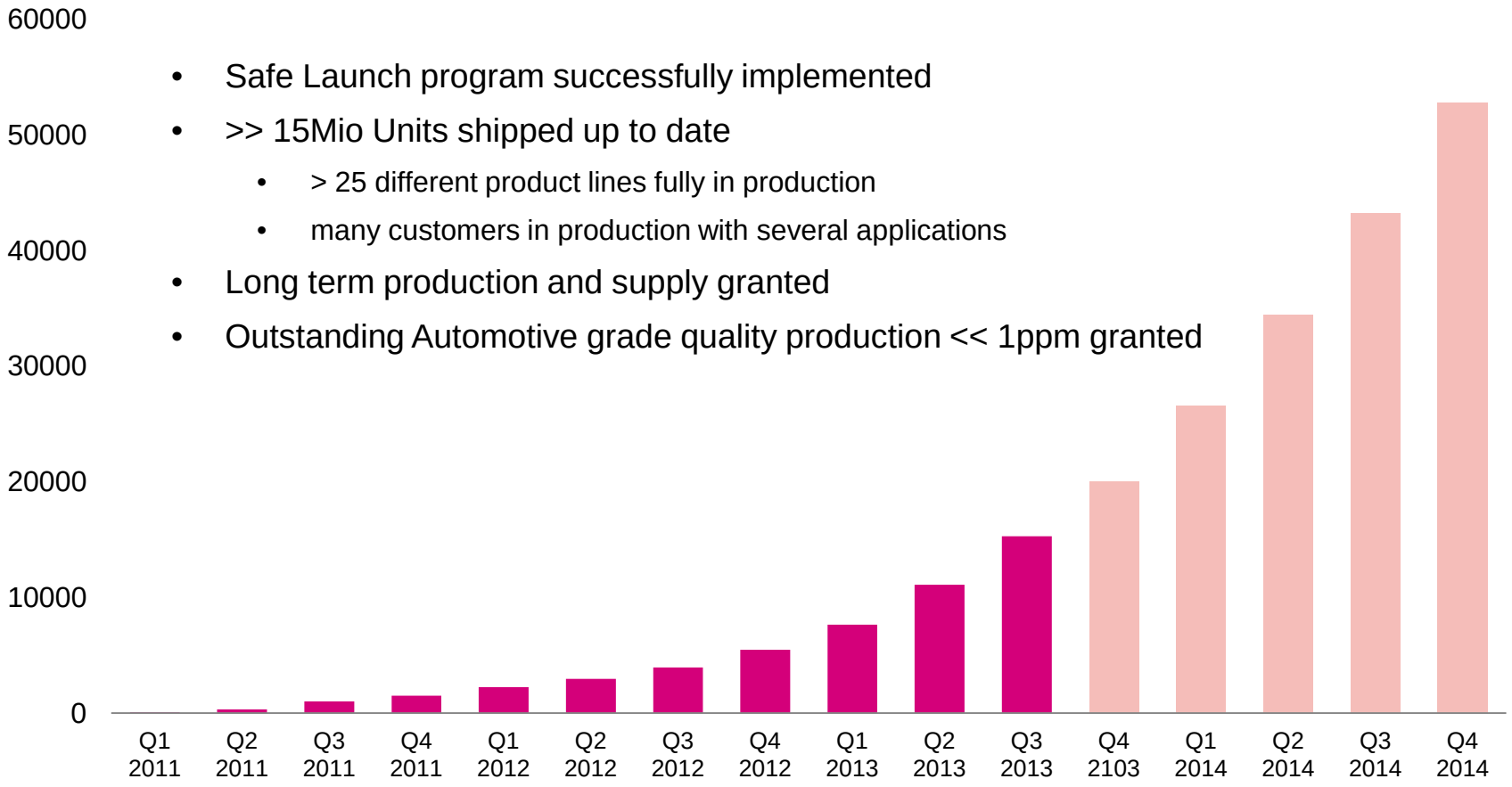
- ST vs our SUPPLIERs
  - Crisis Management Team established at Corporate level
  - Two main task forces: FE & BE
    - team members from Purchasing, Manufacturing, Quality, Planning
    - daily update to Corporate Management
  - Communication to ST customers managed by PCN
  - ***NO IMPACT ON ST DELIVERY***

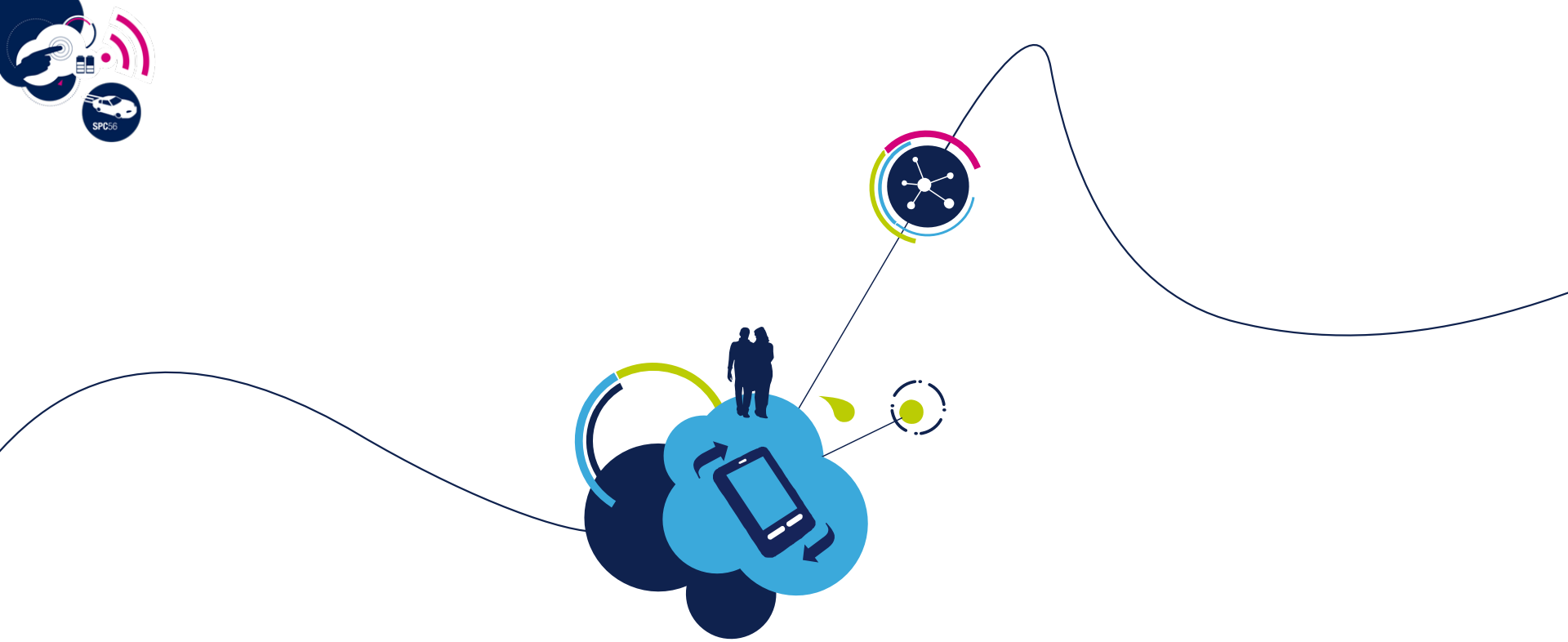
- ST vs our CUSTOMERs
  - ST directly involved by two major car makers to support with uC shipments as a back up for their Tier 2/3 impacted by Japan earthquake in Power Train and Safety related applications :
    - 1st extraordinary delivery after 5 weeks from 1st contact
    - 50% of customer run rate demand reached after 10 weeks
    - **100% of customer run rate demand scheduled after 15 weeks**
    - **NO CUSTOMER RETURN AFTER 3 YEAR AND 1M pcs SHIPPED IN THE FIRST YEAR**

90nm eNVM Production ramp-up Quality Performance

SPC56 ramp up in Automotive (K cumulate pcs)

- Safe Launch program successfully implemented
- >> 15Mio Units shipped up to date
  - > 25 different product lines fully in production
  - many customers in production with several applications
- Long term production and supply granted
- Outstanding Automotive grade quality production << 1ppm granted





M10 Front End Dual Sourcing

PCN APG-MID/13/7698

life.augmented

Crolles transfer global qualification strategy

- M10 TECHNOLOGY MAT30 done
- M10 TV (Pictus 512K, Andorra 4M) MAT30 done
- Similarity will be applied to qualify the M10 products, taking into account that Pictus 512K and Andorra 4M are already qualified:

CMOSM10 Crolles process: qualification plan

Product	Package	# lots Micro	similarity	# lots Flash	Similarity
Pictus 256K	LQFP100 LQFP64	1	Pictus 512K	1	Pictus 512K
Pictus 512K	LQFP144 LQFP100	3	No	3	No
Pictus 1M	LQFP100 LQFP144	1	Pictus 512K	1	Pictus 512K
Bolero 256K	LQFP100 LQFP64	1	Pictus 512K	1	Pictus 512K
Bolero 512K	LQFP144 LQFP100 LQFP64	1	Pictus 512K	1	Pictus 512K
Bolero 1.5M	LQFP176	1	Pictus 512K	1	Pictus 512K
Bolero 3M	LQFP176	1	Pictus 512K	1	Pictus 512K
Monaco 1.5M	LQFP100 LQFP144 LQFP176	3	No	3	No
Andorra 2M	LQFP176	1	Andorra 4M Leopard 1M	1	Andorra 4M Leopard 1M Leopard 2M
Andorra 4M	LQFP176	3	No	3	No
Leopard 1M	LQFP100 LQFP144	1	Andorra 4M Andorra 2M	1	Andorra 2M Andorra 4M Leopard 2M
Leopard 2M	LQFP100 LQFP144	1	Andorra 4M Andorra 2M	1	Andorra 2M Andorra 4M Leopard 1M

SPC56 32-Bit M10 90 nm FE Manufacturing Dual Source strategy

2012	2013												2014												2015				2016	2017
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	Q1	Q2	Q3	Q4		

1 MU shipped

15 MU shipped

Rousset R8 8": current production site for 4 & 6 metal SPC56 (M10 – 90nm) products

M10 90nm 4&6 Metals volume production

Crolles C300 12": high capacity production site for 4 & 6 metal SPC56 (M10 – 90nm) products

M10 90nm high volume production

M10 90nm 6 Metals ramp up

M10 90nm 4 Metals ramp up

Agrate R2 8": additional site for back end of line (contact / metal / vias) steps on Rousset wafers

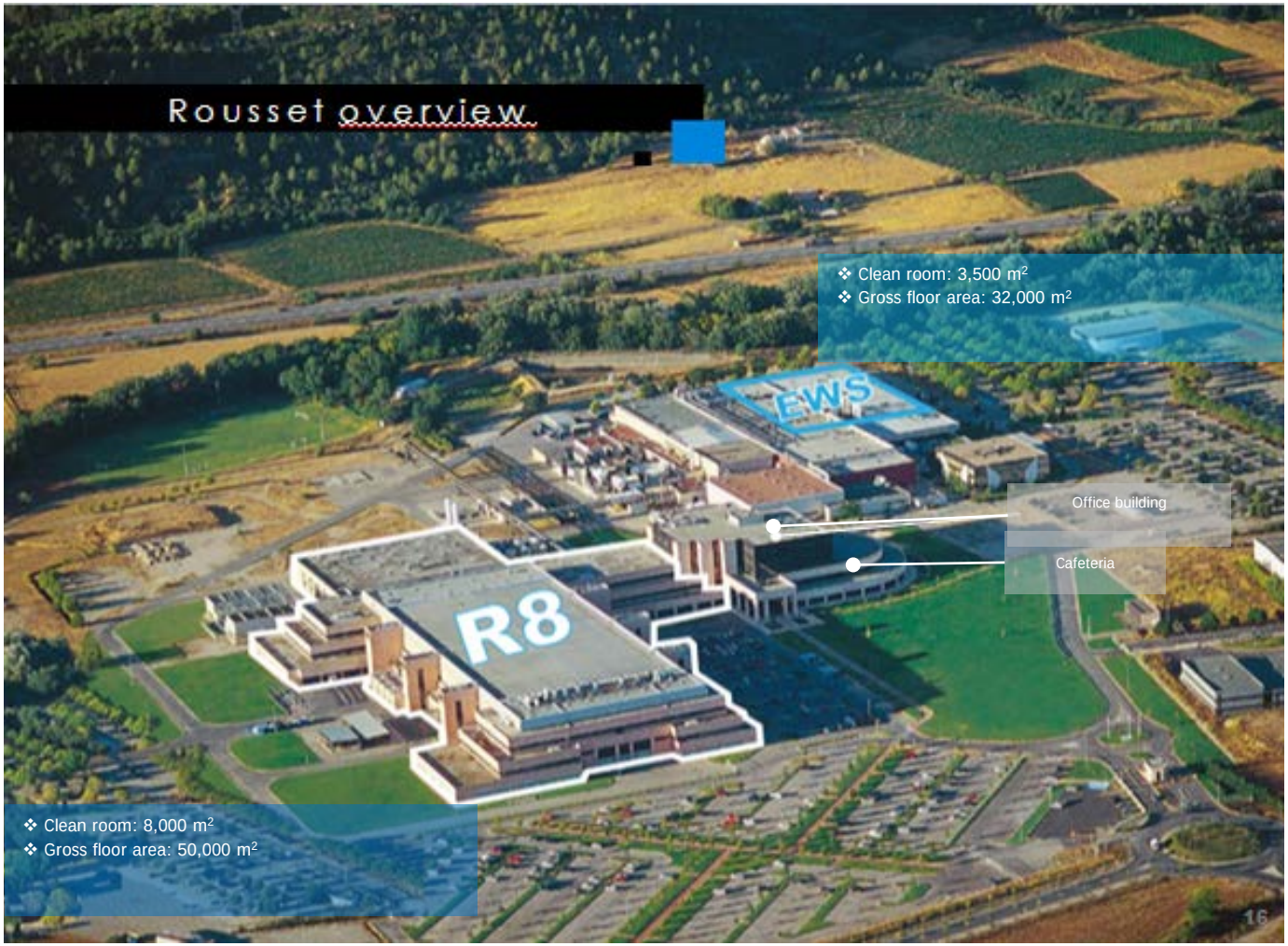
M10 90nm Rousset FEOL + Agrate BEOL 4 Metal products

SPC56 32 Bit - M10 90 nm
Internal FE Manufacturing sites

Rousset	Current	Potential
8" /200mm Capacity	7500 wafers/week	6000 wafers/week full Cu
Product Start	CY2000	
Clean room	7300m²	9500m²
Investissement to date	$1.8 B	
Technologies in production	0.35µm to 90nm	65/55nm
Class	Mini environnement concept (class 1)	
Employees	2722 (total site, including EWS, Divisions and Support Functions)	

Crolles300	Current	Potential
12" /300mm Capacity	3500 wafers/week	4500 wafers/week
Product Start	CY2003	
Clean room	10000m²	
Investissement to date	$1.55 B	
Technologies in production	90nm down to 40nm	32nm down to 22nm
Class	Mini environnement concept (class 1)	
Employees	>5000 (total site, including contractors, partners, and R&D)	

SPC56 32 Bit - M10 90 nm
Rousset plant



SPC56 32 Bit - M10 90 nm
Crolles 300 mm

Embedded non-volatile memory

Technology & Manufacturing Challenges

- Change in eFlash technology development & manufacturing environment
  - Very few companies in the world able to develop & manufacture eFlash
  - Stand-alone NVM manufacturers more and more separated from eFlash manufacturers
  - Very few Auto eFlash MCU supplier keep in-house production capabilities

"Nano2017" R&D Program Announced at STMicroelectronics' Crolles Site

Five-year strategic R&D program led by ST to further advance the company's leadership in key embedded processing solutions and technologies

ST recently announced a dedicated investment plan for Crolles 12" (C300) wafer fab

SPC56 32 Bit - M10 90 nm

Leadership in embedded flash technology

65 kgates / mm2
6 ML / 1.8V

0.18 µm

0.37 µm² Flash cell

M8

ST10-Family

6 – 9 ML / 1.0-1.2 V
290 kgates / mm2

90 nm

0.18 µm² Flash cell

M10

PPC-Family

6 – 10 ML / 0.9-1.0 V
450 kgates / mm2

55 nm

0.135 µm² Flash cell

M55

PPC-Family

6 – 10 ML

40 nm

0.06 µm² Flash

M40

Mass production

Technology qualified
Products in qual.

Technology under development

ST has been a major player in the stand alone flash memory market prior to integrate them inside MCU device
ST is a global player in embedded MCU since 25 years over three different technology node: M6Y, M8, M10

SPC56 32 Bit - M10 90 nm
Crolles300 : Facilities

- **Clean room**
  - surface: 10 000 m² class ISO4 @ 0.1 µm + 2000 m² B2 building
    Foup + mini-environnement class ISO2 @0.1 µm
  - air conditioning: 6.500.000 m3 / h
    21.5°C +/- 0.5 °C temperature
    45% +/- 2 % hygrometry
  - vibration: 3 µm / s (V+H) RMS

- **Fluids**
  - Ultra-pure water: 18.2 Mohm.cm
    1 ppb pour le TOC
    20 ppt pour les chlorures
  - Gases: 100 ppt (O2: 1 ppb)
  - Chemicals: 1-10 ppb

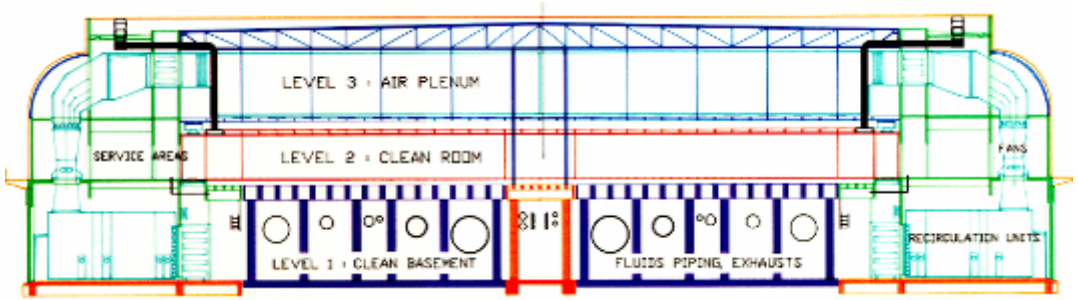
- **Power supply**
  - average: 25 MW
  - UPS: 17 MW

300 mm FOUP

~ 9 kg with 25 wafers

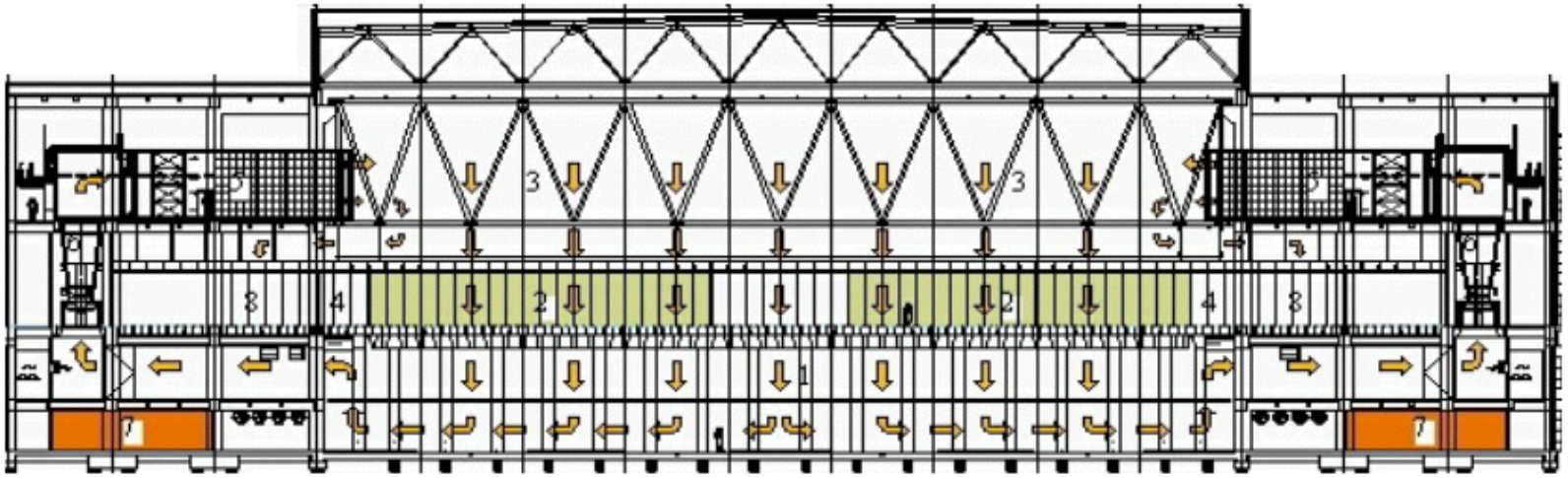
SPC56 32 Bit - M10 90 nm

Crolles 300 mm vs. Crolles 200 mm



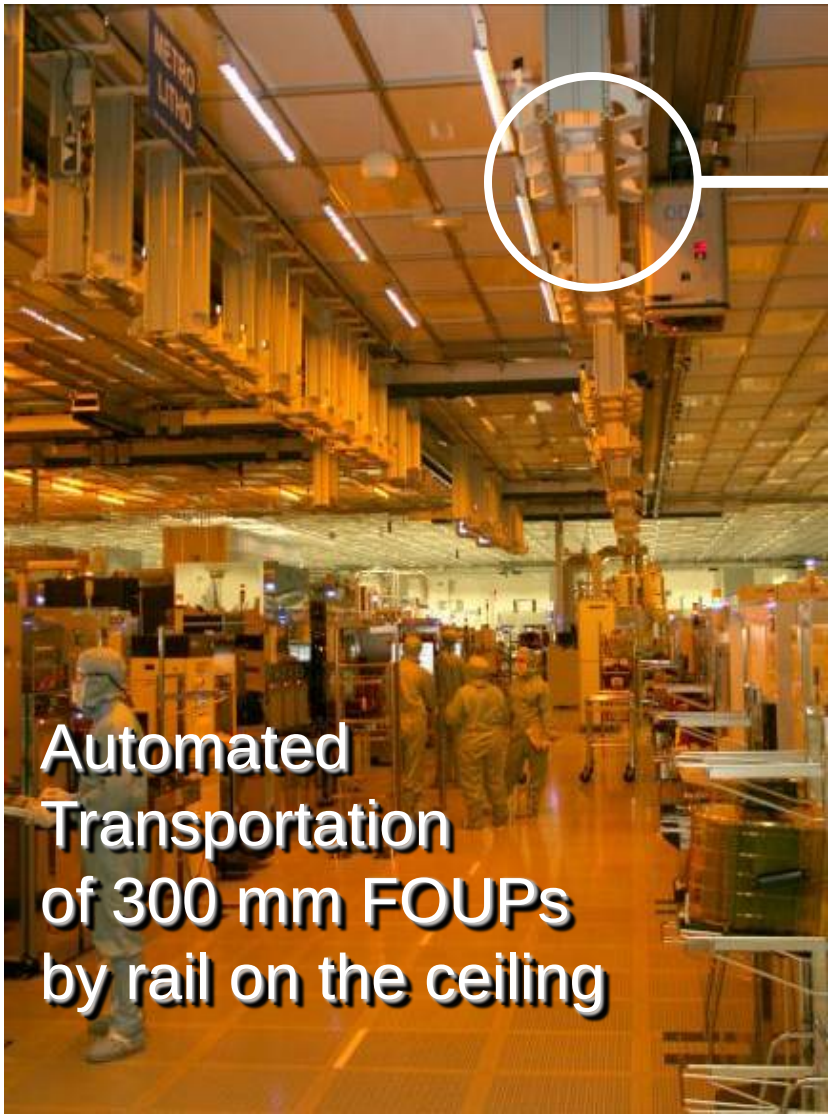
Crolles200 : from 0.35 µm to 0.12 µm

Crolles300 : from 90 nm to 22 nm



SPC56 32 Bit - M10 90 nm
Clean Room 300 mm

SPC56 32 Bit - M10 90 nm
Clean Room 300 mm



SPC56 32 Bit - M10 90 nm
Crolles300 Facilities Overview

Process exhausts
580 000 m³/h

Power:

Installed = 39 MVA

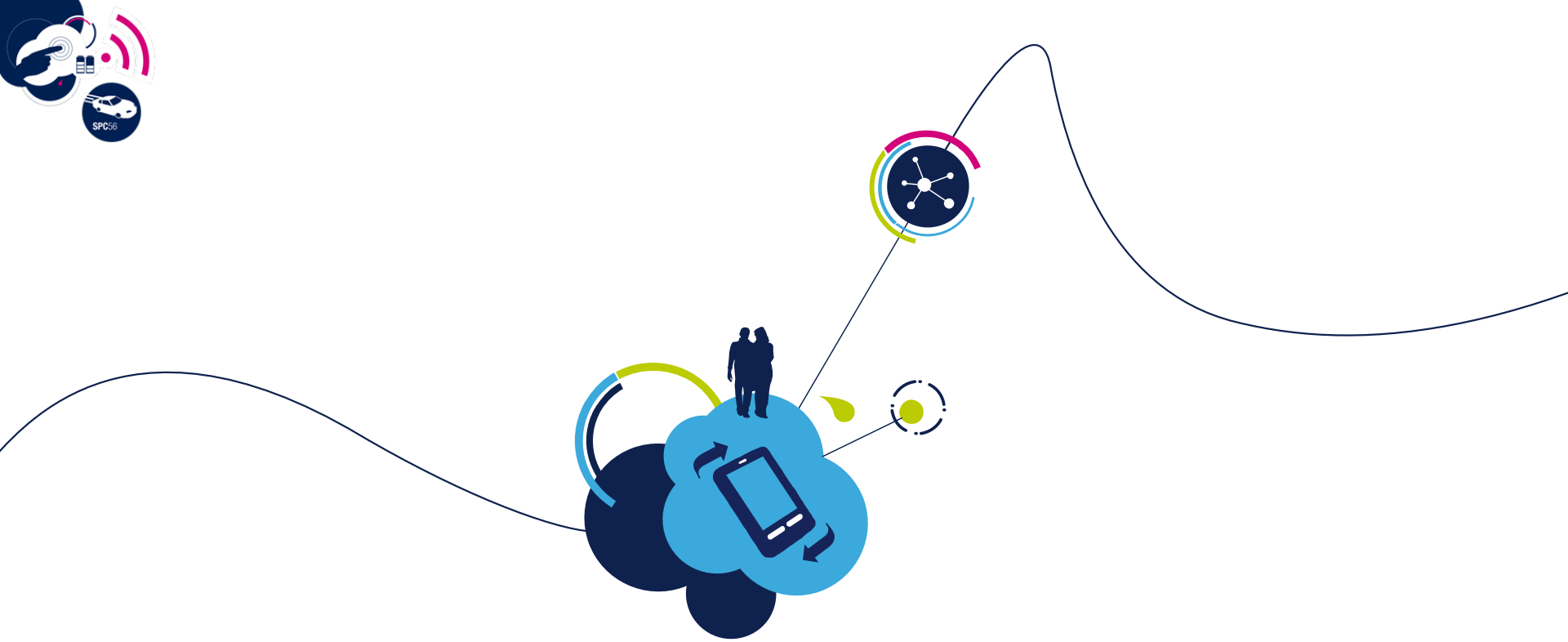
Peak demand = 15.6 MVA

Fab demand = 7.5 MVA

Facilities = 8.1 MVA

80 m³/h Ultra Pure Water Plant

30 MW cooling capacity



M10 EWS Dual Sourcing

PCN APG-MID/13/7996

life.augmented

SPC56 32 Bit - M10 90 nm
EWS in Rousset

- M10 products are tested either in Rousset and/or in Agrate
- Bolero 1.5M is currently tested in Agrate and Rousset site has been qualified as a second EWS (electrical wafer sorting) plant
- Main purposes of this improvement are:
  - Maintain full service level in terms of production capacity
  - Protect running production through strategic choice of a second wafer probing location
- ST Rousset site is ISO/TS 16949 certified and already in use for automotive products including SPC56 devices: since 2010 more than 3K wafers of Bolero 512K were tested in Rousset
- Same hardware equipment (brand & model) will be adopted, based on a copy exactly approach of the whole testing environment
- Qualification activity done on cut 2.1 (SB64221Z)
- PCN APG-MID/13/7996 release in July 2013

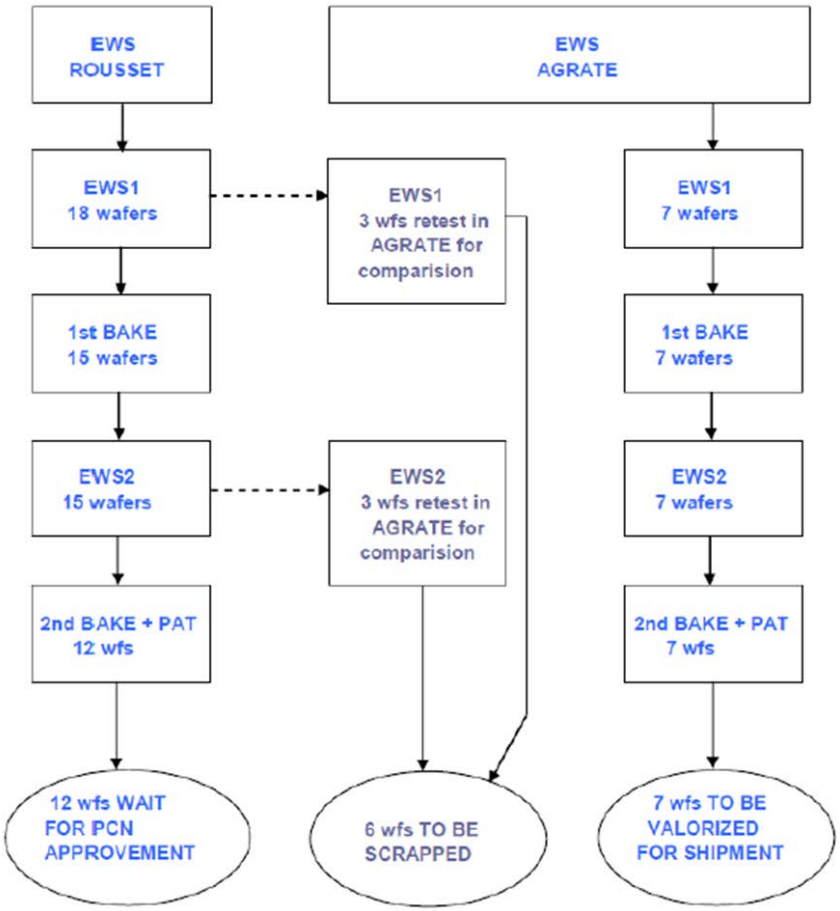
SPC56 32 Bit - M10 90 nm
EWS Agrate – Rousset comparison

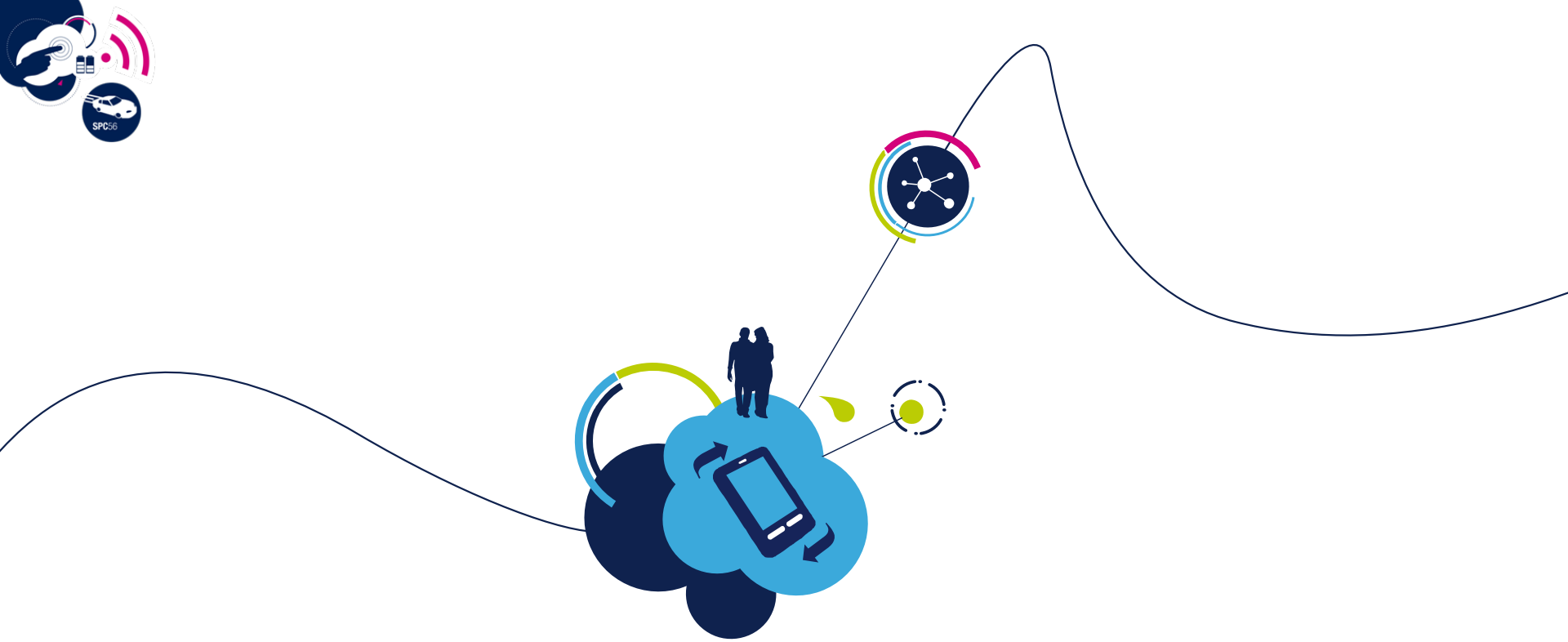
	Agrate	Rousset	Comment & Risk
Device	Bolero 1.5M cut 2.1	Bolero 1.5M cut 2.1	NO CHANGE
Tester used	Teradyne J750	Teradyne J750	NO CHANGE
Prober	ACCRETECH UF3000	ACCRETECH UF3000	NO CHANGE
Probe cards	Vertical tips – MEMS technology	Vertical tips – MEMS technology	NO CHANGE
EWS Flow	CD00295217 Product Specification for SB64221Z in manufacturing phase EWS Plant AF6E Agrate	CD00363150 Product Specification for SB64221Z in manufacturing phase EWS Plant RS8E Rousset	Same Test Flow, Visual Inspection steps detailed differently, see next slides
SOPs	SOP 7069710 and 8132384	SOP 7069710 and 8132384	NO CHANGE

SPC56 32 Bit - M10 90 nm
EWS in Rousset qualification

- The qualification flow maximizes the level of comparison:
  - different wafers of the same lot tested in AGR and ROU
  - same wafers tested in ROU and retested in eng mode for AGR

- CONCLUSION:
  - Testing results in Rousset EWS plant are aligned with those of Agrate
  - Bolero 1.5M EWS test in Rousset is qualified





M10 Back End Dual Sourcing

PCN APG-MID/13/7972

life.augmented

SPC56 32-Bit M10 90 nm
BE Manufacturing Dual Source strategy

2012	2013												2014												2015				2016	2017
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	Q1	Q2	Q3	Q4		

LQFP 100 (14x14) ULA / 144 (20x20) / 176 (24x24) volume production

Kirkop: current production site for high pin count QFP & BGA

BGA 15x15 / 17x17 / 23x23

LQFP 64 (10x10) / 100 (14x14) volume production

Muar

BGA 15x15 / 17x17 / 23x23

LQFP 64 (10x10) / 100 (14x14)

Muar

LQFP 208 (28x28)

SPC56 32 Bit - M10 90 nm
LQFP64 / 100 dual Source Back End

- ST has successfully executed the first step of its manufacturing strategy for assembly with the industrialization and ramp-up of SCP56 family in Malta (QFP high pin count: 100, 144, 176 pins) and Muar (QFP low pin count: 64, 100 pin)

- With the projected growth of SPC56 production volumes and to secure Customer deliveries in case emergency situations, ST is now aggressively qualifying and ramping-up production of:

LQFP64 (10x10) & 100 (14x14) in Malta

  - Process has been qualified
  - ST will introduce CuPd wires on some of its packages

SPC56 32 Bit - M10 90 nm
Similarity for Product Family

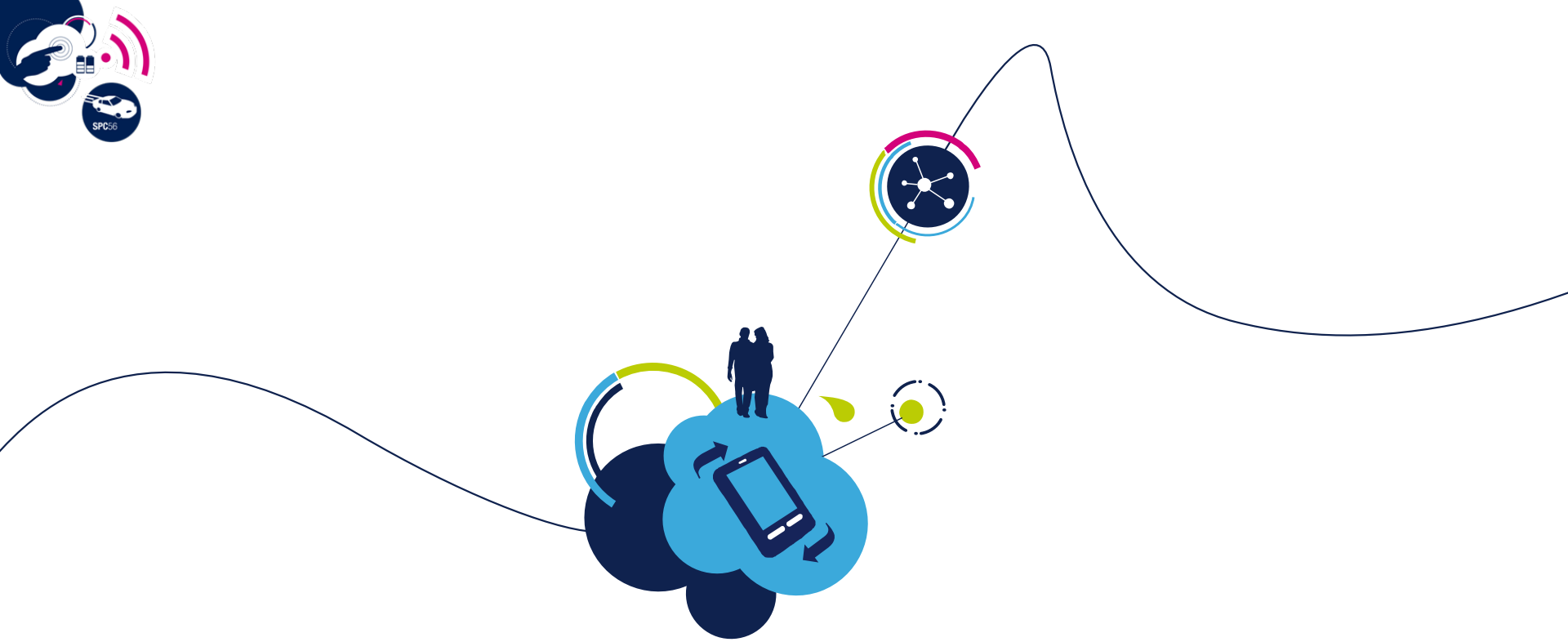
LQFP100 (14x14)

- Package already qualified and in production on FL60 (Leopard 1M)
- FL60 Package reliability report is included in PCN.
- Similarity criteria (defined by an ST specification: ADCS 7028386) for package qualification have been verified and met.
- FL60, FP40, FP50, FP60, FB50 and FB64 microcontrollers belong to the same product family.
- LQFP-100 14x14 Package qualification in Malta using FL60 is extended to FP40, FP50, FP60, and FB50 and FB64 microcontrollers.

LQFP64 (10x10)

- Dedicated qualification exercise based on available similarities

Trial	Conditions	Samples x Assy Lot
HTOL	1k cyc @ 125°C + 168hrs HTOL@125°C (1000hrs monitor)	77 x 1
ELFR	BI + 24hrs	800 x 1
TC	1000cyc -50°C/+150°C	77 x 3
AC	96h	77 x 3
THB	1000h 85°C/85%	77 x 3
HTS	1000hrs@150°C	77 x 1
CA	---	on 3 assy lots



Copper wire qualification

PCN APG-MID/13/7698

life.augmented

SPC56 32 Bit - M10 90 nm
Cu wire qualification

- CuPd wire will be used in M10 products
- Qualification exercise has to be run both on 4 metal and 6 metal option
- Similarities can be used evaluating bonding parameters and bill of material between:
  - 4 metal products (Pictus, Bolero)
  - 6 metal products (Andorra, Monaco, Leopard, Bolero 3M)

SPC56 32 Bit - M10 90 nm
CuPd qualification status

- 6 metal process option
  - Mat 10 (feasibility assessment) — done
  - Mat 20**:** three assembly lots with bonding corner conditions — running
  - Mat 30 for 6M1T process option — running

  Similarity between LQFP176 and LQFP144 packages:
    - Same complexity from process point of view, both are 6M1T
    - Same pad class and same Bond Pad Opening = 52um
    - Same assembly line
    - Line stressing planned on 30K parts to assess manufacturability

- 4 metal process option
  - Mat 10 — done
  - Mat 20**:** three assembly lots with bonding corner conditions — running
  - Mat 30: three assembly lots in standard bonding condition — running
    - Line stressing planned on 30K parts to assess manufacturability

- Samples
  - On customer request starting from — Q4 2013

4 Metal M10 Products in LQFP: QUAL PLAN for CuPd introduction

Products	LQFP Packages	Qualifications	Comments
Pictus512k	LQFP100	PACKAGE VALIDATION + Q100	Full qualification
	LQFP144	Q100	By similarities with Monaco 1.5M LQFP144 and Andorra 4M LQFP176
Pictus256k	LQFP64	PACKAGE VALIDATION + Q100	Full qualification
	LQFP100	NO TRIALS REQUIRED	Similarities with Pictus 512K LQFP100
Pictus1M	LQFP100	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 512K LQFP100
	LQFP144	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 512K LQFP144
Bolero256k	LQFP64	NO TRIALS REQUIRED	Similarities with Pictus 256K LQFP64
	LQFP100	NO TRIALS REQUIRED	Similarities with Pictus 512K LQFP100
Bolero512k	LQFP64	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 256K LQFP64
	LQFP100	NO TRIALS REQUIRED	Similarities with Pictus 512K LQFP100
	LQFP144	NO TRIAL REQUIRED	Similarities with Pictus 512K LQFP144
Bolero1M5	LQFP100	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 512K LQFP100
	LQFP144	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 512K LQFP144
	LQFP176	1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	By similarities with Andorra 4M LQFP176 and Pictus 512K LQFP144

6 Metal M10 Products in LQFP: QUAL PLAN for CuPd introduction

Products	Packages	Qualifications	Comments
Andorra 4M	LQFP176	PACKAGE VALIDATION + Q100	Shared with Monaco1M5 LQFP144
Monaco 1M5	LQFP144	PACKAGE VALIDATION + Q100	Shared with Andorra 4M LQFP176
	LQFP100	PACKAGE VALIDATION + Q100	Package similarities with LQFP100 4 metal option qualification
	LQFP176	NO TRIALS REQUIRED	By similarities with Monaco 1.5M LQFP144 and Andorra 4M LQFP176
Andorra 2M	LQFP176	NO TRIALS REQUIRED	By similarities with Monaco 1.5M LQFP144 and Andorra 4M LQFP176
Leopard 1M	LQFP100	NO TRIALS REQUIRED	Similarity with Leopard 2M
	LQFP144	NO TRIALS REQUIRED	Similarity with Leopard 2M
Leopard 2M	LQFP100	PACKAGE VALIDATION + Q100	Package similarities with LQFP100 4 metal option qualification
	LQFP144	PACKAGE VALIDATION + ONLY 1 LOT OF TC REQUIRED BECAUSE BIGGER DIE SIZE	Similarities with Pictus 512K and Monaco 1.5M LQFP144
Bolero 3M	LQFP176	NO TRIALS REQUIRED	Similarities with Pictus 512K, Leopard 1M and Andorra 4M

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR ‘‘AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL’’ INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

RESTRICTIONS OF USE AND CONFIDENTIALITY OBLIGATIONS:

THIS DOCUMENT AND ITS ANNEXES CONTAIN ST PROPRIETARY AND CONFIDENTIAL INFORMATION. THE DISCLOSURE, DISTRIBUTION, PUBLICATION OF WHATSOEVER NATURE OR USE FOR ANY OTHER PURPOSE THAN PROVIDED IN THIS DOCUMENT OF ANY INFORMATION CONTAINED IN THIS DOCUMENT AND ITS ANNEXES IS SUBMITTED TO ST PRIOR EXPRESS AUTHORIZATION. ANY UNAUTHORIZED REVIEW, USE, DISCLOSURE OR DISTRIBUTION OF SUCH INFORMATION IS EXPRESSLY PROHIBITED.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com