74HC4851; 74HCT4851

8-channel analog multiplexer/demultiplexer with injection-current effect control

Rev. 4 — 15 May 2023 Product data sheet

1. General description

The 74HC4851; 74HCT4851 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7A.

The 74HC4851; 74HCT4851 are 8-channel analog multiplexers/demultiplexers with three digital select inputs (S0 to S2), an active-LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The devices feature injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

2. Features and benefits

- Injection-current cross coupling < 1 mV/mA
- Wide supply voltage range from 2.0 V to 6.0 V for 74HC4851
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- Low ON-state resistance:
  - 400 Ω (typical) at V_{CC} = 2.0 V
  - 215 Ω (typical) at V_{CC} = 3.0 V
  - 120 Ω (typical) at V_{CC} = 3.3 V
  - 76 Ω (typical) at V_{CC} = 4.5 V
  - 59 Ω (typical) at V_{CC} = 6.0 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4851D 74HCT4851D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4851PW 74HCT4851PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4851BQ 74HCT4851BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1

5. Functional diagram

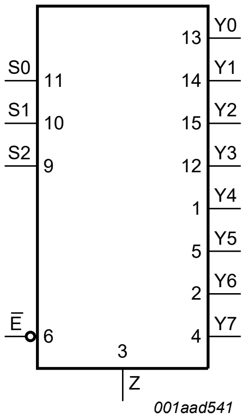


Fig. 1. Logic symbol

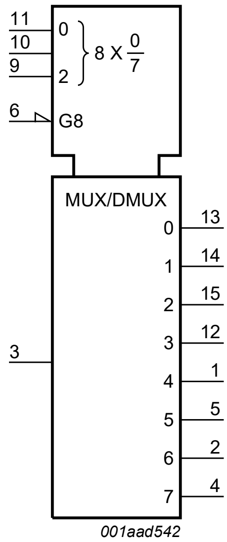


Fig. 2. IEC logic symbol

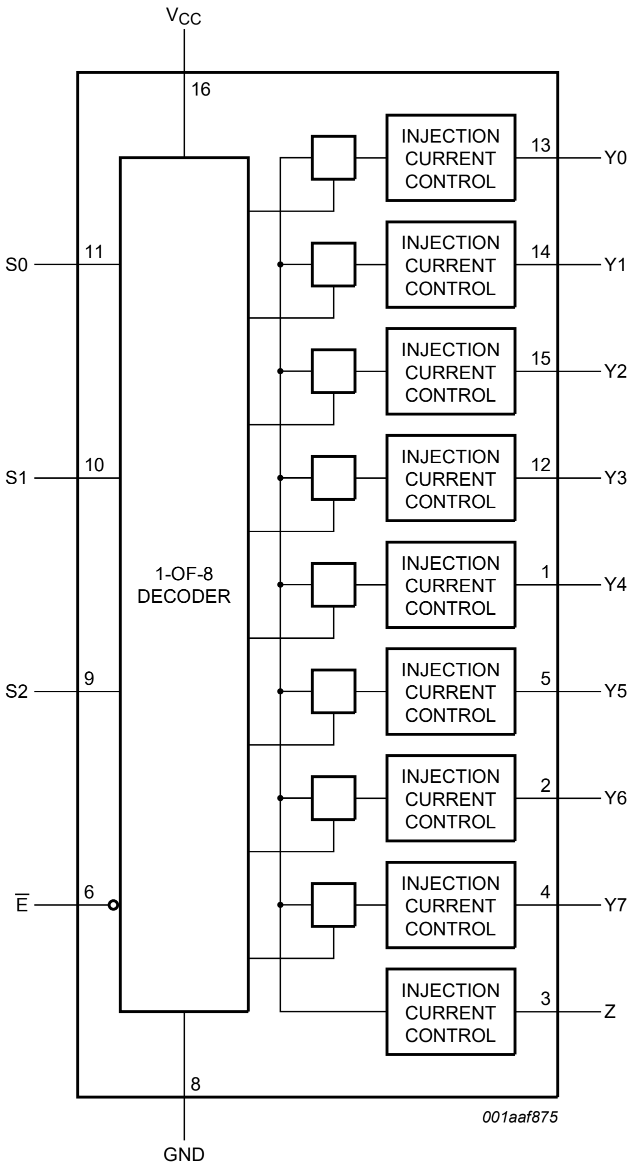
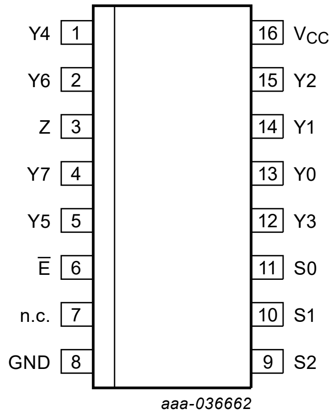


Fig. 3. Functional diagram

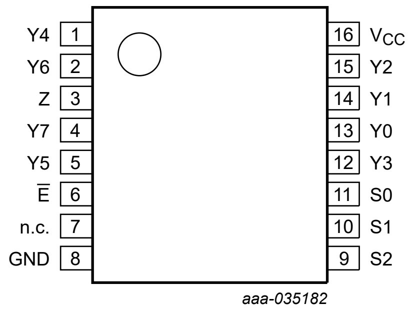
6. Pinning information

6.1. Pinning

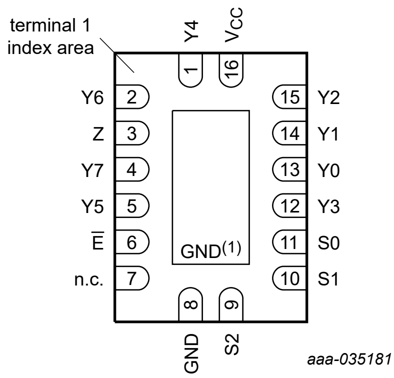
D package
SOT109-1 (SO16)



PW package
SOT403-1 (TSSOP16)



BQ package
SOT763-1 (DHVQFN16)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Y4, Y6, Y7, Y5, Y3, Y0, Y1, Y2	1, 2, 4, 5, 12, 13, 14, 15	independent input/output
Z	3	common input/output
E̅	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S2, S1, S0	9, 10, 11	select input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Channel ON
$\overline{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	V_{CC} + 0.5	V
V_{SW}	switch voltage	[2]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{SK}	switch clamping current	V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V	-	±20	mA
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.
[2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4851			74HCT4851			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	-	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	6.0	1000	-	-	-	ns/V
		V_{CC} = 3.0 V	-	6.0	800	-	-	-	ns/V
		V_{CC} = 3.3 V	-	6.0	800	-	-	-	ns/V
		V_{CC} = 4.5 V	-	6.0	500	-	6.0	500	ns/V
		V_{CC} = 6.0 V	-	6.0	400	-	-	-	ns/V

10. Static characteristics

Table 6. R_{ON} resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4851										
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\overline{E} = V_{IL}$								
		V_{CC} = 2.0 V; I_{SW} = 2 mA	-	400	650	-	670	-	700	Ω
		V_{CC} = 3.0 V; I_{SW} ≤ 2 mA	-	215	330	-	360	-	380	Ω
		V_{CC} = 3.3 V; I_{SW} ≤ 2 mA	-	120	270	-	305	-	345	Ω
		V_{CC} = 4.5 V; I_{SW} ≤ 2 mA	-	76	210	-	240	-	270	Ω
		V_{CC} = 6.0 V; I_{SW} ≤ 2 mA	-	59	195	-	220	-	250	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}$; $\overline{E} = V_{IL}$								
		V_{CC} = 2.0 V; I_{SW} = 2 mA	-	4	10	-	15	-	20	Ω
		V_{CC} = 3.0 V; I_{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V_{CC} = 3.3 V; I_{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V_{CC} = 4.5 V; I_{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V_{CC} = 6.0 V; I_{SW} ≤ 2 mA	-	3	9	-	13	-	18	Ω
74HCT4851										
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\overline{E} = V_{IL}$								
		V_{CC} = 4.5 V; I_{SW} ≤ 2 mA	-	76	210	-	240	-	270	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}$; $\overline{E} = V_{IL}$								
		V_{CC} = 4.5 V; I_{SW} ≤ 2 mA	-	2	8	-	12	-	16	Ω

Table 7. Injection current coupling

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see Fig. 7.

Symbol	Parameter	Conditions	74HC4851			74HCT4851			Unit
			Min	Typ [1]	Max	Min	Typ [1]	Max	
T_{amb} = -40 °C to +125 °C									
ΔV_O	output voltage variation	$\lvert I_{SW}\rvert \leq 1$ mA; $R_S \leq 3.9$ kΩ [2] [3]							
		V_{CC} = 3.3 V	-	0.05	1	-	-	-	mV
		V_{CC} = 5.0 V	-	0.03	1	-	0.03	1	mV
		$\lvert I_{SW}\rvert \leq 10$ mA; $R_S \leq 3.9$ kΩ							
		V_{CC} = 3.3 V	-	0.55	5	-	-	-	mV
		V_{CC} = 5.0 V	-	0.27	5	-	0.27	5	mV
		$\lvert I_{SW}\rvert \leq 1$ mA; $R_S \leq 20$ kΩ							
		V_{CC} = 3.3 V	-	0.04	2	-	-	-	mV
		V_{CC} = 5.0 V	-	0.03	2	-	0.03	2	mV
		$\lvert I_{SW}\rvert \leq 10$ mA; $R_S \leq 20$ kΩ							
		V_{CC} = 3.3 V	-	0.56	20	-	-	-	mV
		V_{CC} = 5.0 V	-	0.48	20	-	0.48	20	mV

[1] Typical values are measured at T_{amb} = 25 °C.
[2] ΔV_O here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.
[3] I_{SW} = total current injected into all disabled channels.

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V);

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4851										
V_{IH}	HIGH-level input voltage	control inputs								
		V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 3.3 V	2.3	-	-	2.3	-	2.3	-	V
		V_{CC} = 4.5 V	3.15	-	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	-	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	control inputs								
		V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 3.3 V	-	-	1.0	-	1.0	-	1.0	V
		V_{CC} = 4.5 V	-	-	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	control inputs; V_I = GND or V_{CC}; V_{CC} = 6.0 V	-	-	±0.1	-	±0.1	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$\overline{E}$ = V_{IH}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Fig. 4								
		per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
$I_{S(ON)}$	ON-state leakage current	$\overline{E}$ = V_{IL}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Fig. 5	-	-	±0.1	-	±0.5	-	±1.0	μA
I_{CC}	supply current	V_I = GND or V_{CC}; V_{CC} = 6.0 V	-	-	2.0	-	5.0	-	20.0	μA
C_I	input capacitance	S0, S1, S2 and $\overline{E}$	-	2	10	-	10	-	10	pF
C_{sw}	switch capacitance	Z; OFF-state	-	15	40	-	40	-	40	pF
		Yn; OFF-state	-	3	15	-	15	-	15	pF
74HCT4851										
V_{IH}	HIGH-level input voltage	control inputs; V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	control inputs; V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
I_I	input leakage current	control inputs; V_I = GND or V_{CC}; V_{CC} = 5.5 V	-	-	±0.1	-	±0.1	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$\overline{E}$ = V_{IH}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 5.5 V; see Fig. 4								
		per channel	-	-	±0.1	-	±0.5	-	±1.0	μA
		all channels	-	-	±0.2	-	±2.0	-	±4.0	μA
$I_{S(ON)}$	ON-state leakage current	$\overline{E}$ = V_{IL}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 5.5 V; see Fig. 5	-	-	±0.1	-	±0.5	-	±1.0	μA
I_{CC}	supply current	V_I = GND or V_{CC}; V_{CC} = 5.5 V	-	-	2.0	-	5.0	-	20.0	μA
ΔI_{CC}	additional supply current	control inputs; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	300	-	370	-	370	μA
C_I	input capacitance	S0, S1, S2 and $\overline{E}$	-	2	10	-	10	-	10	pF
C_{sw}	switch capacitance	Z; OFF-state	-	15	40	-	40	-	40	pF
		Yn; OFF-state	-	3	15	-	15	-	15	pF

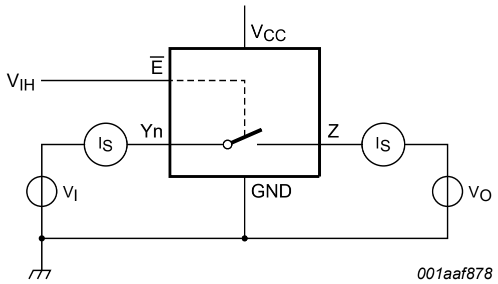
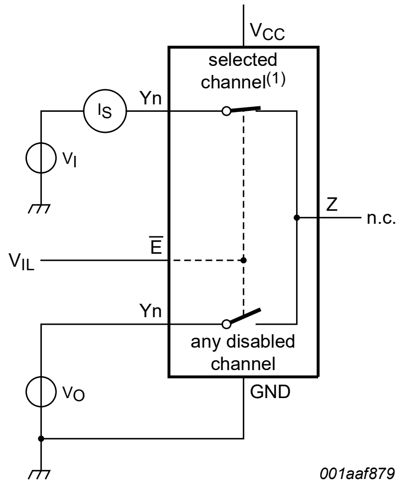
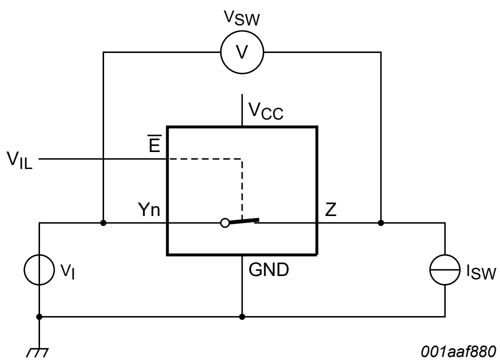


Fig. 4. Test circuit for measuring OFF-state leakage current



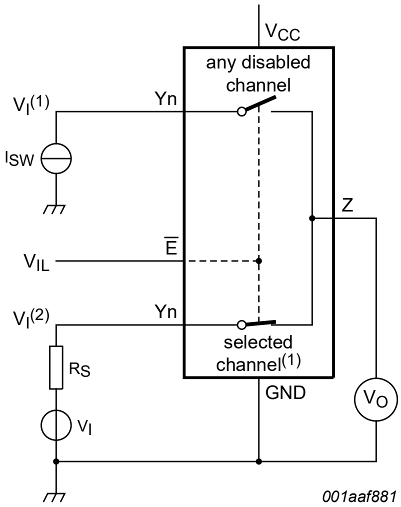
(1) Channel is selected by S0, S1 and S2.

Fig. 5. Test circuit for measuring ON-state leakage current



$R_{ON} = V_{SW} / I_{SW}$.

Fig. 6. Test circuit for measuring ON resistance



(1) Channel is selected by S0, S1 and S2.

$V_I(1)$ < GND or $V_I(1) > V_{CC}$.

GND < $V_I(2) < V_{CC}$.

Fig. 7. Test circuit for injection current coupling

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 12.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4851										
t_{pd}	propagation delay	Z to Yn, Yn to Z; see Fig. 8 [1]								
		V_{CC} = 2.0 V	-	10.0	25	-	29	-	32	ns
		V_{CC} = 3.0 V	-	6.0	15.5	-	17.5	-	19.5	ns
		V_{CC} = 3.3 V	-	5.0	14.5	-	16.5	-	18.5	ns
		V_{CC} = 4.5 V	-	4.0	11.5	-	12.5	-	13.5	ns
		V_{CC} = 6.0 V	-	3.0	10	-	11	-	12	ns
		Sn to Z, Sn to Yn; see Fig. 9 [1]								
		V_{CC} = 2.0 V	-	18.0	32	-	35	-	40	ns
		V_{CC} = 3.0 V	-	9.5	17.5	-	20	-	23	ns
		V_{CC} = 3.3 V	-	8.5	16.5	-	19	-	22	ns
		V_{CC} = 4.5 V	-	6.5	13	-	15	-	17	ns
		V_{CC} = 6.0 V	-	5.0	12.5	-	14.5	-	16.5	ns
t_{en}	enable time	$\overline{E}$ to Z, $\overline{E}$ to Yn; see Fig. 10 [2]								
		V_{CC} = 2.0 V	-	-	95	-	105	-	115	ns
		V_{CC} = 3.0 V	-	-	90	-	100	-	110	ns
		V_{CC} = 3.3 V	-	-	85	-	95	-	105	ns
		V_{CC} = 4.5 V	-	-	80	-	90	-	100	ns
		V_{CC} = 6.0 V	-	-	78	-	80	-	80	ns
t_{dis}	disable time	$\overline{E}$ to Z, $\overline{E}$ to Yn; see Fig. 10 [3]								
		V_{CC} = 2.0 V	-	-	99	-	105	-	115	ns
		V_{CC} = 3.0 V	-	-	90	-	100	-	110	ns
		V_{CC} = 3.3 V	-	-	85	-	95	-	105	ns
		V_{CC} = 4.5 V	-	-	80	-	90	-	100	ns
		V_{CC} = 6.0 V	-	-	78	-	80	-	80	ns
C_{PD}	power dissipation capacitance	per channel; see Fig. 11 [4]								
		V_{CC} = 3.3 V	-	28	-	-	-	-	-	pF
		V_{CC} = 5.0 V	-	33	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HCT4851											
t_{pd}	propagation delay	Z to Yn, Yn to Z; see Fig. 8	[1]								
		V_{CC} = 4.5 V		1.6	3.7	11.5	1.1	12.5	1.1	13.5	ns
		Sn to Z, Sn to Yn; see Fig. 9	[1]								
		V_{CC} = 4.5 V		3.2	8.0	13	2.3	15	2.3	17	ns
t_{en}	enable time	$\overline{E}$ to Z, $\overline{E}$ to Yn; see Fig. 10	[2]								
		V_{CC} = 4.5 V		4.2	8.6	25	3.0	30	3.0	35	ns
t_{dis}	disable time	$\overline{E}$ to Z, $\overline{E}$ to Yn; see Fig. 10	[3]								
		V_{CC} = 4.5 V		28.5	64.7	80	28.2	90	28	100	ns
C_{PD}	power dissipation capacitance	per channel; see Fig. 11	[4]								
		V_{CC} = 5.0 V		-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L + C_{sw}) \times V_{CC}^2 \times f_o$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\sum(C_L + C_{sw}) \times V_{CC}^2 \times f_o$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit

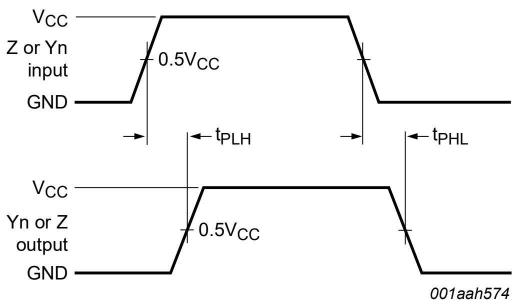
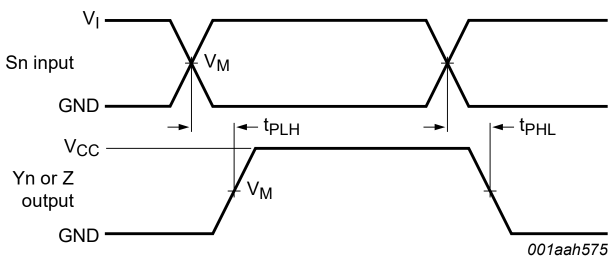
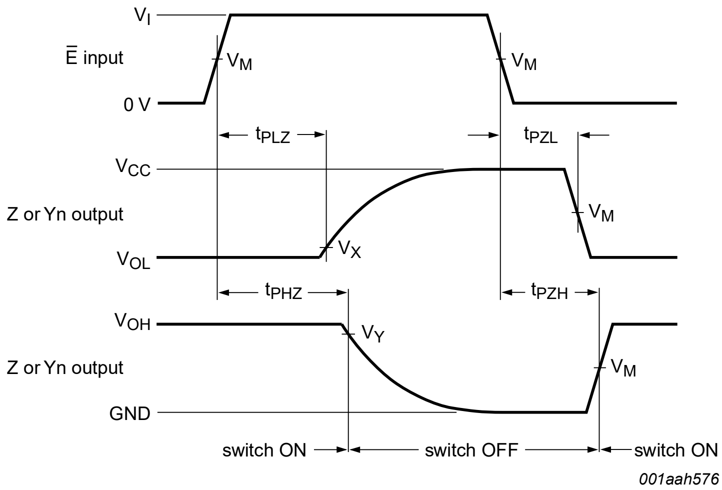


Fig. 8. Input (Z, Yn) to output (Yn, Z) propagation delays



Measurement points are given in Table 10.

Fig. 9. Input (Sn) to output (Yn, Z) propagation delays



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. Enable and disable times

Table 10. Measurement points

Type	Input		Output		
	V_M	V_I	V_M	V_X	V_Y
74HC4851	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}	V_{OL} + 0.1 × (V_{CC} - V_{OL})	0.9 × V_{OH}
74HCT4851	1.3 V	3.0 V	0.5 × V_{CC}	V_{OL} + 0.1 × (V_{CC} - V_{OL})	0.9 × V_{OH}

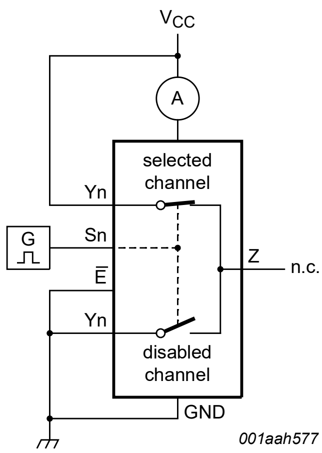
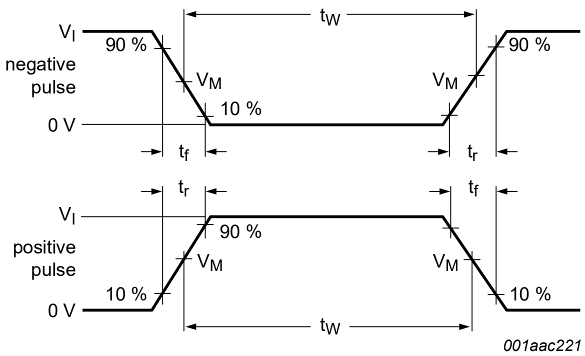
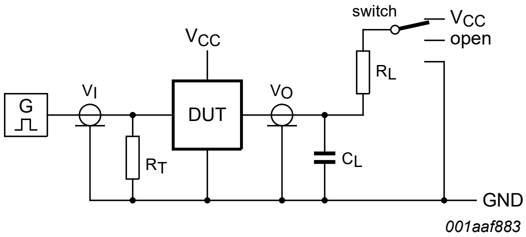


Fig. 11. Test circuit for measuring power dissipation capacitance



a. Input pulse definition



Test data is given in Table 11.

Definitions for test circuit:

R_L = load resistance;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

b. Test circuit

Fig. 12. Test circuit for measuring switching times

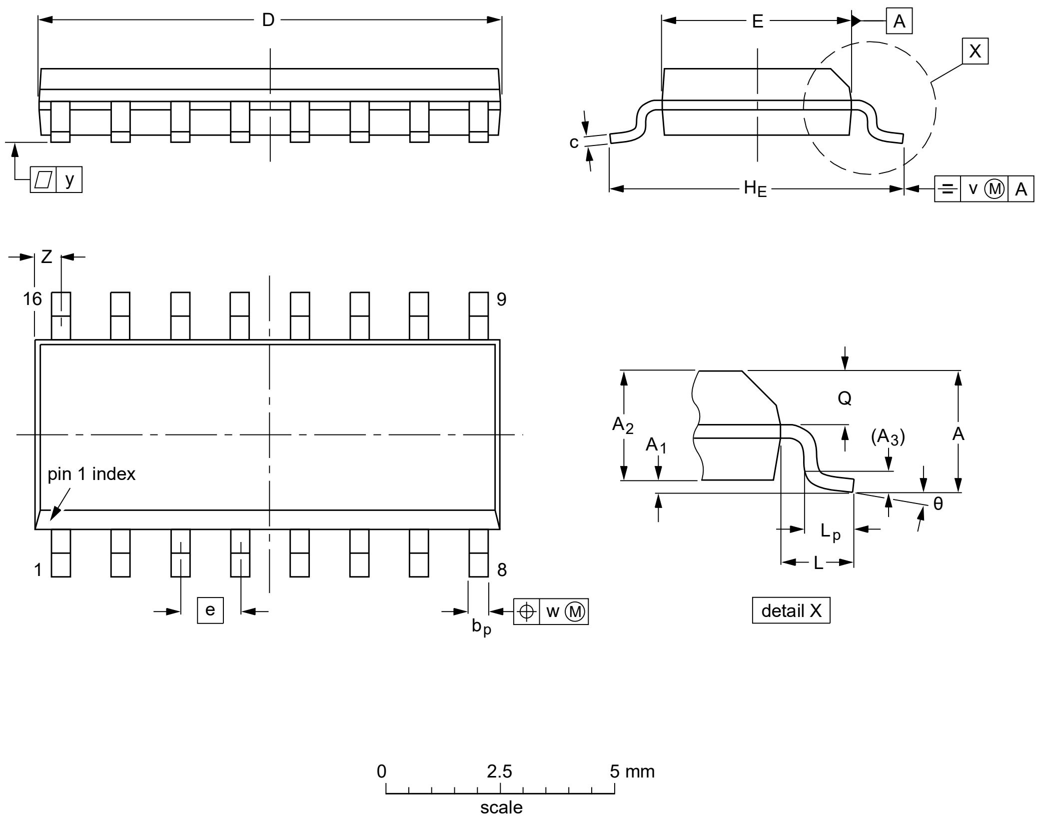
Table 11. Test data

Test	Input			Output		S1 position
	Control $\overline{E}$, Sn	Switch Yn (Z)	t_r, t_f	Switch Z (Yn)		
	V_I [1]	V_I		C_L	R_L	
t_{PHL}, t_{PLH}	V_{CC}	V_{CC}	6 ns	50 pF	-	open
t_{PHZ}, t_{PZH}	V_{CC}	V_{CC}	6 ns	50 pF	10 kΩ	GND
t_{PLZ}, t_{PZL}	V_{CC}	V_{CC}	6 ns	50 pF	10 kΩ	V_{CC}
C_{PD}	V_{CC}	V_{CC}	6 ns	0 pF	-	open

[1] For 74HCT4851: input voltage V_I = 3.0 V.

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

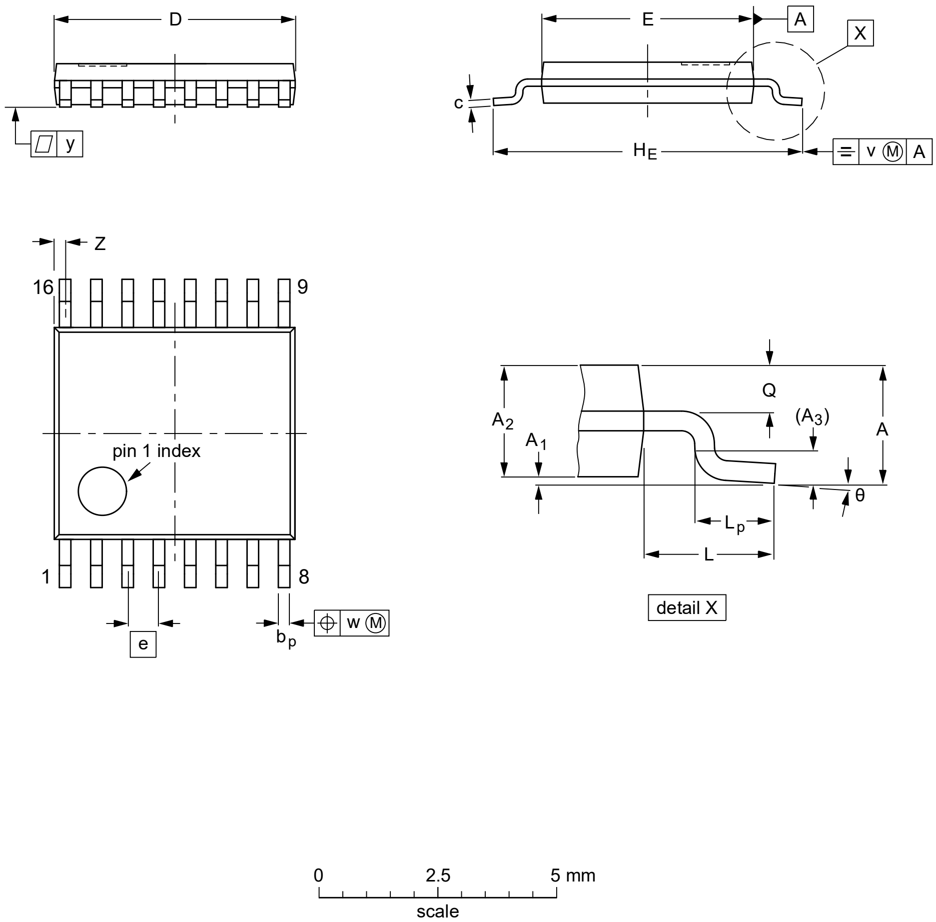
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

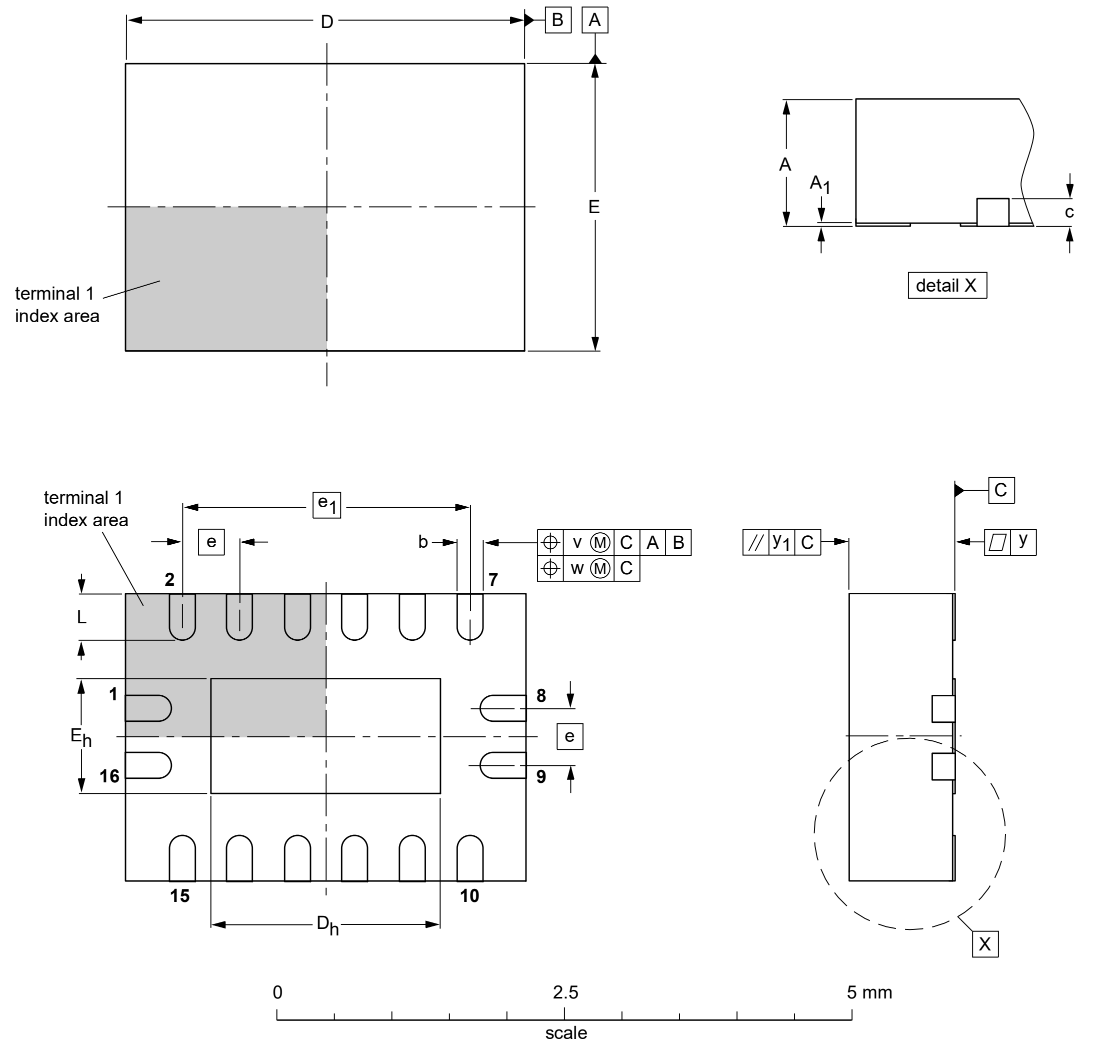
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 15. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4851 v.4	20230515	Product data sheet	-	74HC_HCT4851 v.3
Modifications:	• Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT4851 v.3	20180824	Product data sheet	-	74HC_HCT4851 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4851 v.2	20080902	Product data sheet	-	74HC4851 v.1
Modifications:	• 74HCT4851 device added.			
74HC4851 v.1	20070309	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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