11 A High Voltage Isolated Bipolar Gate Driver with Fault Detection, Miller Clamp

FEATURES

- 11 A short-circuit source current (0 Ω gate resistance)
- 9 A short-circuit sink current (0 Ω gate resistance)
- 4.61 A peak current (2 Ω gate resistance)
- Output power device resistance: <1 Ω
- Output voltage range up to 30 V
- Multiple UVLO options on V_{DD2}
  - Grade A: 14.5 V (typical) UVLO on V_{DD2} positive going threshold
  - Grade B and Grade C: 11.5 V (typical) UVLO on V_{DD2} positive going threshold
- V_{DD1} input voltage range from 2.5 V to 6 V
- Desaturation protection
  - Soft shutdown on desaturation fault
- Multiple desaturation detect comparator voltages
  - Grade B: 9.2 V (typical)
  - Grade A and Grade C: 3.5 V (typical)
- Miller clamp output with gate sense input
- Isolated fault and ready functions
- Low propagation delay: 75 ns (typical)
- Operating temperature range: −40°C to +125°C
- Creepage distance: 8.3 mm minimum
- CMTI: 100 kV/µs
- Safety and regulatory approvals (pending)
  - 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - DIN V VDE V 0884-11
  - V_{IORM} = 2150 V peak

APPLICATIONS

- SiC/MOSFET/IGBT gate drivers
- Photovoltaic (PV) inverters
- Motor drives
- Power supplies

GENERAL DESCRIPTION

The ADuM4146 is a single-channel gate driver specifically optimized for driving silicon carbide (SiC), metal-oxide semiconductor field effect transistors (MOSFETs). Analog Devices, Inc., *i*Coupler® technology provides isolation between the input signal and the output gate drive.

The ADuM4146 includes a Miller clamp to provide robust SiC turn off with a single-rail supply when the gate voltage drops to less than 2 V. Operation with unipolar or bipolar secondary supplies is possible with or without the Miller clamp operation.

The Analog Devices chip scale transformers also provide isolated communication of control information between the high voltage and low voltage domains of the chip. Information on the status of the chip can be read back from dedicated outputs. Control of resetting the device after a fault on the secondary side is performed on the primary side of the device.

Integrated onto the ADuM4146 is a desaturation detection circuit that provides protection against high voltage short-circuit SiC operation. The desaturation protection contains noise reducing features, such as a 300 ns masking time after a switching event to mask voltage spikes due to initial turn on (see Figure 17). An optional internal 500 µA current source allows low device count, and the internal blanking switch allows the addition of an external current source if more noise immunity is needed.

The secondary undervoltage lockout (UVLO) is set to 14.5 V (typical) for Grade A and is set to 11.5 V (typical) for Grade B and Grade C with common SiC and insulated gate bipolar transistor (IGBT) levels taken into consideration.

Rev. 0

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

4/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

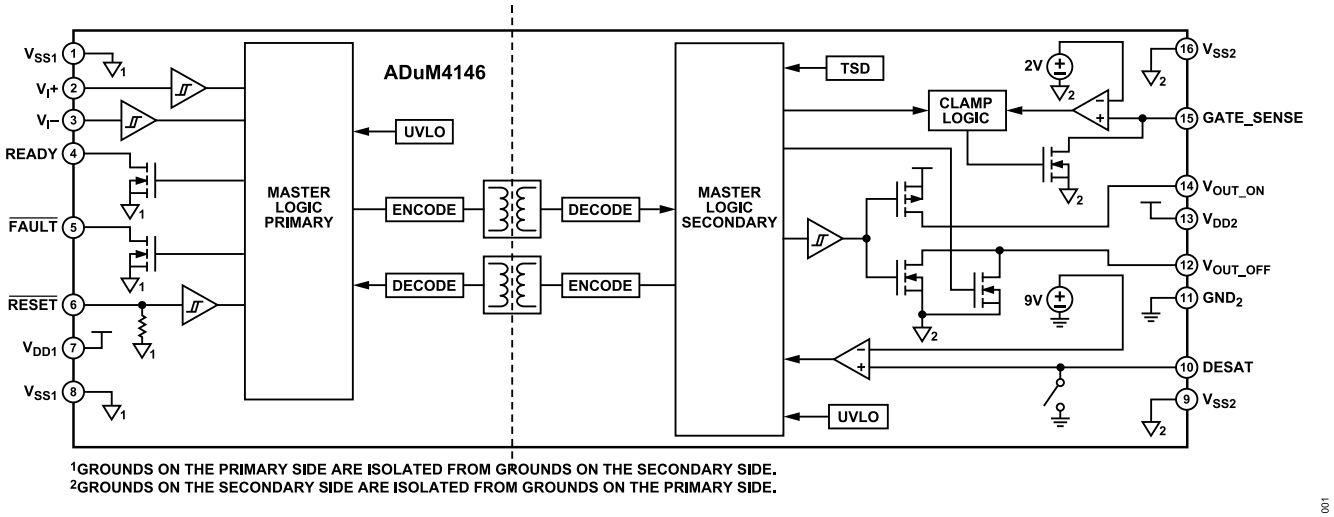

Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to V_{SS1}. High-side voltages referenced to GND_2, 2.5 V ≤ V_{DD1} ≤ 6 V, 12 V ≤ V_{DD2} ≤ 30 V, and T_J = −40°C to +125°C. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High-Side Power Supply						
Input Voltage						
V_{DD2}	V_{DD2}	12		30	V	$V_{DD2} - V_{SS2}$ ≤ 30 V
V_{SS2}	V_{SS2}	−15		0	V	
Input Current, Quiescent						Ready high
V_{DD2}	$I_{DD2\,(Q)}$		4.9	6.5	mA	
V_{SS2}	$I_{SS2\,(Q)}$		4.82	6.21	mA	
Logic Supply						
V_{DD1} Input Voltage	V_{DD1}	2.5		6	V	
Input Current	I_{DD1}					
Output Low			1.78	2.17	mA	Output signal low
Output High			10.45	14.5	mA	Output signal high
Logic Inputs (V_I+, V_I−, and $\overline{RESET}$)						
Input Current (V_I+ and V_I− Only)	I_I	−1	+0.01	+1	μA	
Logic High Input Voltage	V_{IH}	0.7 × V_{DD1}			V	2.5 V ≤ $V_{DD1} - V_{SS1}$ ≤ 5 V
		3.5			V	$V_{DD1} - V_{SS1}$ > 5 V
Logic Low Input Voltage	V_{IL}			0.3 × V_{DD1}	V	2.5 V ≤ $V_{DD1} - V_{SS1}$ ≤ 5 V
				1.5	V	$V_{DD1} - V_{SS1}$ > 5 V
$\overline{RESET}$ Internal Pull-Down	$R_{\overline{RESET}_PD}$		300		kΩ	
UVLO						
V_{DD1} Positive Going Threshold	$V_{VDD1UV+}$		2.43	2.5	V	
V_{DD1} Negative Going Threshold	$V_{VDD1UV-}$	2.2	2.34		V	
V_{DD1} Hysteresis	$V_{VDD1UVH}$		0.09		V	
V_{DD2} Positive Going Threshold	$V_{VDD2UV+}$		14.5	15.0	V	Grade A
			11.5	12.0	V	Grade B and Grade C
V_{DD2} Negative Going Threshold	$V_{VDD2UV-}$	13.35	14.1		V	Grade A
		10.4	11.1		V	Grade B and Grade C
V_{DD2} Hysteresis	$V_{VDD2UVH}$		0.4		V	
$\overline{FAULT}$ Pull-Down FET Resistance	$R_{\overline{FAULT}_PD_FET}$		11	50	Ω	Tested at 5 mA
$\overline{READY}$ Pull-Down FET Resistance	$R_{RDY_PD_FET}$		11	50	Ω	Tested at 5 mA
Desaturation (DESAT)						
Desaturation Detect Comparator Voltage	$V_{DESAT,\,TH}$	8.73	9.2	9.61	V	Grade B
		3.25	3.5	3.75	V	Grade A and Grade C
Internal Current Source	I_{DESAT_SRC}	470	527	593	μA	Grade B
			0		μA	Grade A and Grade C
Thermal Shutdown (TSD)						
TSD Positive Edge	T_{TSD_POS}		155		°C	
TSD Hysteresis	T_{TSD_HYST}		20		°C	
Miller Clamp Voltage Threshold	V_{CLP_TH}	1.75	2	2.25	V	Referenced to V_{SS2}
Pull-Down Negative Metal-Oxide Semiconductor (NMOS) On Resistance	R_{DSON_N}		470	807	mΩ	Tested at 250 mA

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
			470	807	mΩ	Tested at 1 A
Pull-Up Positive Metal-Oxide Semiconductor (PMOS) On Resistance	R_{DSON_P}		471	975	mΩ	Tested at 250 mA
			479	975	mΩ	Tested at 1 A
Soft Shutdown NMOS	R_{DSON_FAULT}		10.2	22	Ω	Grade B, tested at 25 mA
			5		Ω	Grade A and Grade C, tested at 25 mA
Internal Miller Clamp Resistance	R_{DSON_MILLER}		1.1	2.75	Ω	Tested at 100 mA
Short-Circuit Source Current	I_{SC_SOURCE}		11		A	V_{DD2} = 15 V, 0 Ω gate resistance
Short-Circuit Sink Current	I_{SC_SINK}		9		A	V_{DD2} = 15 V, 0 Ω gate resistance
Peak Current	I_{PK}		4.61		A	V_{DD2} = 12 V, 2 Ω gate resistance
SWITCHING SPECIFICATIONS						
Pulse Width[1]		50			ns	Load capacitance (C_L) = 2 nF, V_{DD2} = 15 V, external gate resistance in the on path (R_{GON})[2] = external gate resistance in the off path (R_{GOFF})[2] = 3.9 Ω
$\overline{\text{RESET}}$ Debounce	$t_{DEB_\overline{RESET}}$	500	615	700	ns	
Propagation Delay[3]	t_{DHL}, t_{DLH}	55	75	100	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[2]= R_{GOFF}[2] = 3.9 Ω
Propagation Delay Skew[4]	t_{PSK}			25	ns	C_L = 2 nF, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω, V_{DD1} = 5 V to 6 V
Output Rise and Fall Time (10% to 90%)	t_R/t_F	11	16	27	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω
Blanking Capacitor Discharge Switch Masking	t_{MASK}	260	300	340	ns	
Desaturation Comparator Delay	t_{DESAT_DELAY}	105	132	160	ns	Grade B
		90	115	145	ns	Grade A and Grade C
Time to Report Desaturation Fault to Pin	t_{REPORT}		1.2	2.2	µs	
Common-Mode Transient Immunity (CMTI)	|CMTI|					
Static CMTI[5]		100			kV/µs	Common-mode voltage (V_{CM}) = 1500 V
Dynamic CMTI[6]		100			kV/µs	V_{CM} = 1500 V

[1] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

[2] See the Power Dissipation section.

[3] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{OUTx} signal, where the V_{OUTx} signal is when V_{OUT_ON} and V_{OUT_OFF} are connected to each other. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{OUTx} signal. See Figure 16 for waveforms of propagation delay parameters.

[4] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 16 for the waveforms of the propagation delay parameters.

[5] Static CMTI is defined as the largest dv/dt between V_{SS1} and V_{SS2}, with inputs held either high or low, such that the output voltage remains either more than 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients more than the recommended levels can cause momentary data upsets.

[6] Dynamic CMTI is defined as the largest dv/dt between V_{SS1} and V_{SS2} with the switching edge coincident with the transient test pulse. Operation with transients more than the recommended levels can cause momentary data upsets.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
Junction to Ambient Thermal Resistance	θ_{JA}		59.35		°C/W	4-layer printed circuit board (PCB)
Junction to Top Thermal Characterization	Ψ_{JT}		12.74		°C/W	4-layer PCB

[1] The ADuM4146 is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

SPECIFICATIONS

REGULATORY INFORMATION

The ADuM4146 is pending approval by the organizations listed in Table 3.

Table 3.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to VDE0884-11[2]
Single Protection, 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2, 1532 V rms (2206 V peak) maximum working voltage	Reinforced insulation, 2150 V peak
	Reinforced Insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2, 766 V rms (1103 V peak) maximum working voltage	
File (Pending)	File (Pending)	File (Pending)

[1] In accordance with UL 1577, each ADuM4146 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).

[2] In accordance with DIN V VDE V 0884-11, each ADuM4146 is proof tested by applying an insulation test voltage ≥ 4031 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		51 min	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		I		Material Group

DIN V VDE V 0884-11 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics (Pending)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	2150	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	4031	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	3225	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	2580	V peak
Highest Allowable Overvoltage		V_{IOTM}	15,000	V peak

SPECIFICATIONS

Table 5. VDE Characteristics (Pending)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Surge Isolation Voltage	V peak = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	15,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	2.1	W
Insulation Resistance at T_S	Voltage between the input and output (V_{IO}) = 500 V	R_S	$>10^9$	Ω

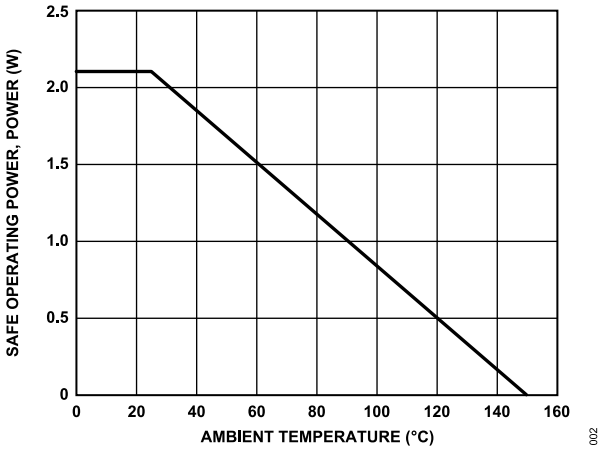

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Supply Voltages	
V_{DD1}[1]	2.5 V to 6 V
V_{DD2}[2]	12 V to 30 V
$V_{DD2} - V_{SS2}$[2]	12 V to 30 V
V_{SS2}[2]	−15 V to 0 V
Input Signal Rise and Fall Time	1 ms
Static CMTI[3]	−100 kV/µs to +100 kV/µs
Dynamic CMTI[4]	−100 kV/µs to +100 kV/µs
T_A Range	−40°C to +125°C

[1] Referenced to V_{SS1}.

[2] Referenced to GND_2. $V_{DD2} - V_{SS2}$ must not exceed 30 V.

[3] Static CMTI is defined as the largest dv/dt between V_{SS1} and V_{SS2}, with inputs held either high or low, such that the output voltage remains either more than 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients more than the recommended levels can cause momentary data upsets.

[4] Dynamic CMTI is defined as the largest dv/dt between V_{SS1} and V_{SS2} with the switching edge coincident with the transient test pulse. Operation with transients more than the recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltages	
V_{DD1}[1]	−0.3 V to +6.5 V
V_{DD2}[2]	−0.3 V to +35 V
V_{SS2}[2]	−20 V to +0.3 V
$V_{DD2} - V_{SS2}$	35 V
Input Voltages	
V_I+, V_I-[1]	−0.3 V to +6.5 V
DESAT Voltage (V_{DESAT})	−0.3 V to V_{DD2} + 0.3 V
GATE_SENSE Voltage (V_{GATE_SENSE})[3]	−0.3 V to V_{DD2} + 0.3 V
V_{OUT_ON}[3]	−0.3 V to V_{DD2} + 0.3 V
V_{OUT_OFF}[3]	−0.3 V to V_{DD2} + 0.3 V
Common-Mode Transients (|CM|)	−150 kV/µs to +150 kV/µs
Temperature	
Storage (T_{ST}) Range	−55°C to +150°C
T_A Range	−40°C to +125°C

[1] Referenced to V_{SS1}.

[2] Referenced to GND_2.

[3] Referenced to V_{SS2}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	1500 V rms	20 year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	1660 V peak	Limited by the creepage of the package, Pollution Degree 2, Material Group I[2, 3]

[1] See the Insulation Lifetime section for details.

[2] Other pollution degree and material group requirements yield a different limit.

[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

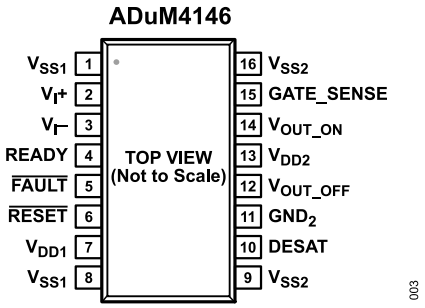

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	V_{SS1}	Ground Reference for Primary Side.
2	V_I+	Positive Logic Complementary Metal-Oxide Semiconductor (CMOS) Input Drive Signal.
3	V_I−	Negative Logic CMOS Input Drive Signal.
4	READY	Open-Drain Logic Output. Connect the READY pin to a pull-up resistor to read the signal. A high state on the READY pin indicates that the device is functional and ready to operate as a gate driver. The presence of READY low precludes the gate drive output from going high.
5	$\overline{\text{FAULT}}$	Open-Drain Logic Output. Connect the $\overline{\text{FAULT}}$ pin to a pull-up resistor to read the signal. A low state on the $\overline{\text{FAULT}}$ pin indicates when a desaturation fault occurs. The presence of a fault condition precludes the gate drive output from going high.
6	$\overline{\text{RESET}}$	CMOS Input. When a fault exists, bring the $\overline{\text{RESET}}$ pin low to clear the fault.
7	V_{DD1}	Input Supply Voltage on Primary Side, 2.5 V to 5.5 V. Referenced to V_{SS1}.
9, 16	V_{SS2}	Negative Supply for Secondary Side, −15 V to 0 V. Referenced to GND_2.
10	DESAT	Detection of Desaturation Condition. Connect the DESAT pin to an external current source or a pull-up resistor. A fault on the DESAT pin asserts a fault on the $\overline{\text{FAULT}}$ pin on the primary side. Until the fault is cleared on the primary side, the gate drive is suspended. During a fault condition, a smaller turn off FET slowly brings the gate voltage down.
11	GND_2	Ground Reference for Secondary Side. Connect the GND_2 pin to the source of the SiC MOSFET being driven.
12	V_{OUT_OFF}	Gate Drive Output Current Path for the Off Signal.
13	V_{DD2}	Secondary Side Input Supply Voltage, 12 V to 30 V. Referenced to V_{SS2}.
14	V_{OUT_ON}	Gate Drive Output Current Path for the On Signal.
15	GATE_SENSE	Gate Voltage Sense Input and Miller Clamp Output. Connect the GATE_SENSE pin to the gate of the power device being driven. The GATE_SENSE pin senses the gate voltage for the purpose of Miller clamping. When the Miller clamp is not used, tie GATE_SENSE to V_{SS2}.

Table 10. Truth Table (Positive Logic)

V_I+ Input	V_I− Input	$\overline{\text{RESET}}$ Pin	READY Pin	$\overline{\text{FAULT}}$ Pin	V_{DD1} State	V_{DD2} State	V_{GATE}[1]
Low	Low	High	High	High	Powered	Powered	Low
Low	High	High	High	High	Powered	Powered	Low
High	Low	High	High	High	Powered	Powered	High
High	High	High	High	High	Powered	Powered	Low
Don't Care	Don't care	High	Low	Unknown	Powered	Powered	Low
Don't Care	Don't care	High	Unknown	Low	Powered	Powered	Low
Low	Low	High	Low	Unknown	Unpowered	Powered	Low
Don't Care	Don't care	Low[2]	Unknown	H3	Powered	Powered	Low
Don't Care	Don't care	Don't care	Low	Unknown	Powered	Unpowered	Unknown

[1] V_{GATE} is the voltage of the gate being driven.

[2] Time dependent value. See the Absolute Maximum Ratings section for details on timing.

TYPICAL PERFORMANCE CHARACTERISTICS

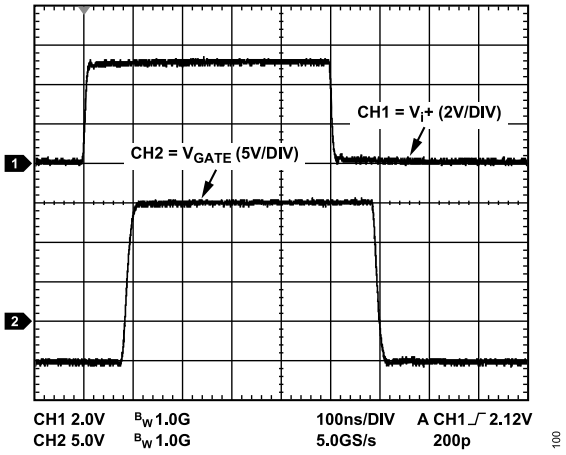

Figure 4. Typical Input to Output Waveform, 2 nF Load, 3.6 Ω Series Gate Resistor, V_{DD1} = 5 V, V_{DD2} = 15 V, V_{SS2} = −5 V

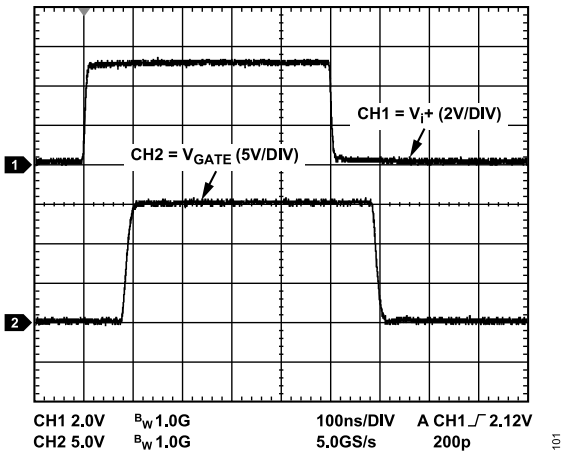

Figure 5. Typical Input to Output Waveform, 2 nF Load, 3.6 Ω Series Gate Resistor, V_{DD1} = 5 V, V_{DD2} = 15 V, V_{SS2} = 0 V

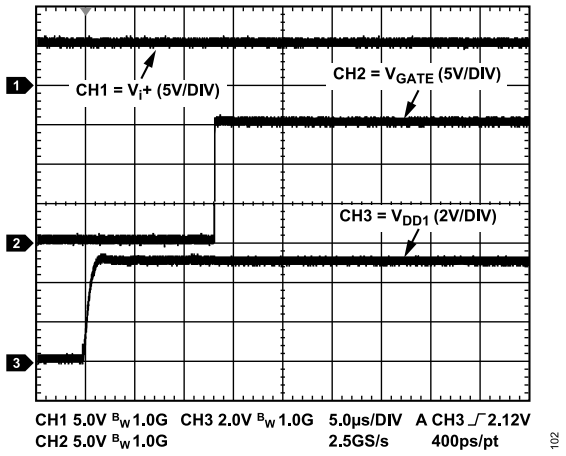

Figure 6. Typical V_{DD1} Startup to Output Valid

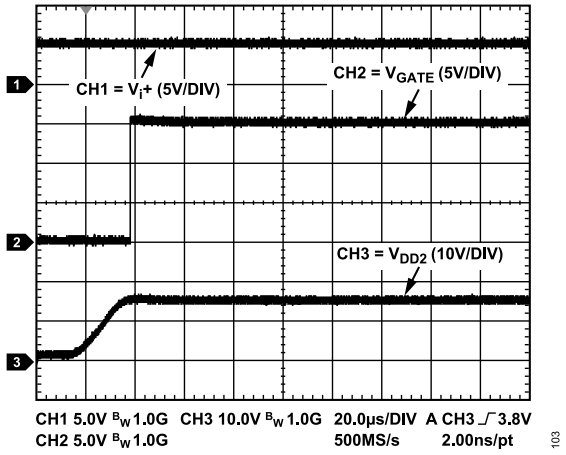

Figure 7. Typical V_{DD2} Startup to Output Valid

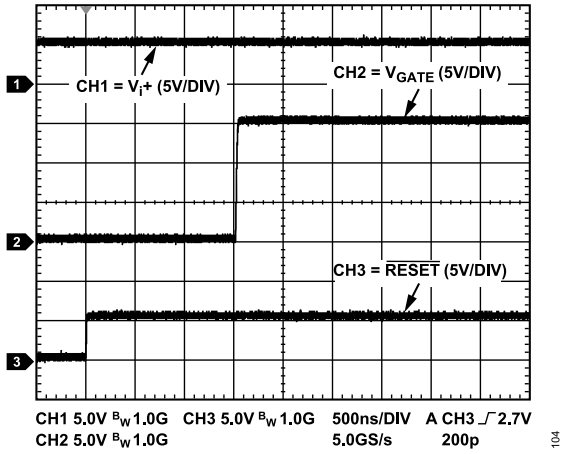

Figure 8. Typical $\overline{RESET}$ to Output Valid

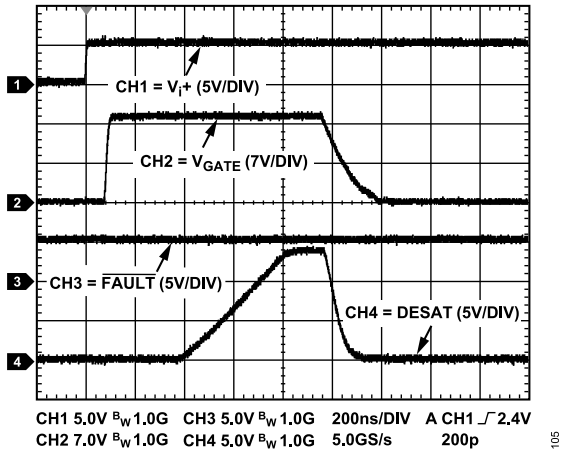

Figure 9. Example Desaturation Event and Reporting, B Grade

TYPICAL PERFORMANCE CHARACTERISTICS

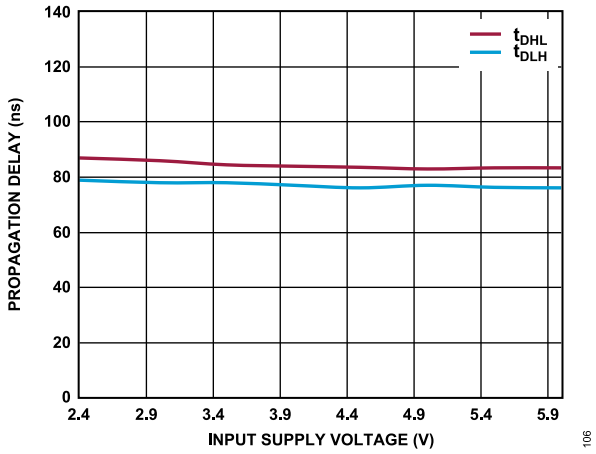

Figure 10. Propagation Delay vs. Input Supply Voltage (V_{DD1}), $V_{DD2} - V_{SS2}$ = 15 V

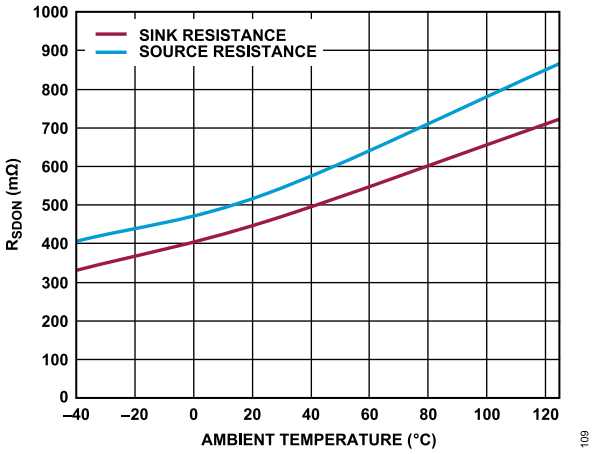

Figure 13. Output Resistance (R_{DSON}) vs. Ambient Temperature, V_{DD2} = 15 V, 250 mA Test

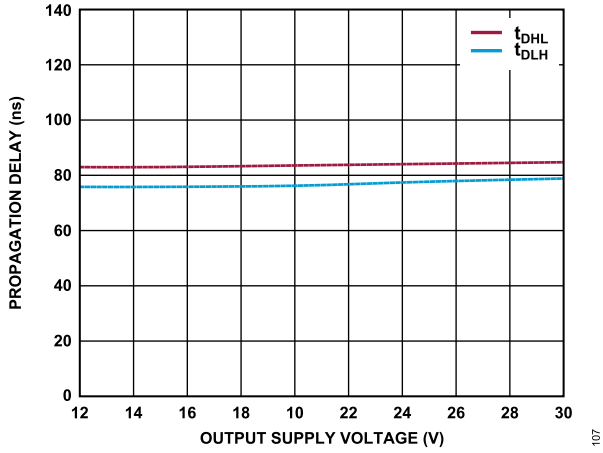

Figure 11. Propagation Delay vs. Output Supply Voltage (V_{DD2}), V_{DD1} = 5 V

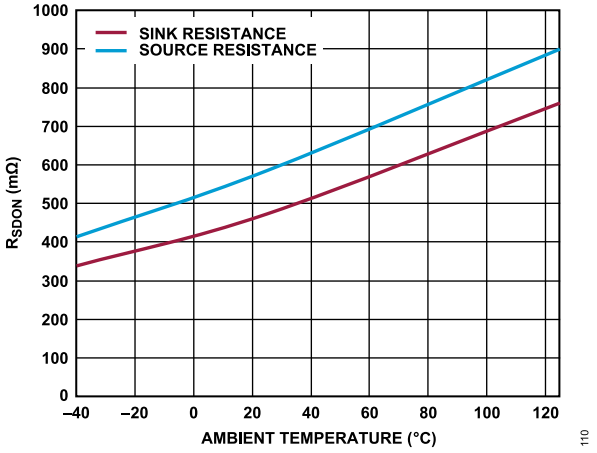

Figure 14. R_{DSON} vs. Ambient Temperature, V_{DD2} = 15 V, 1 A Test

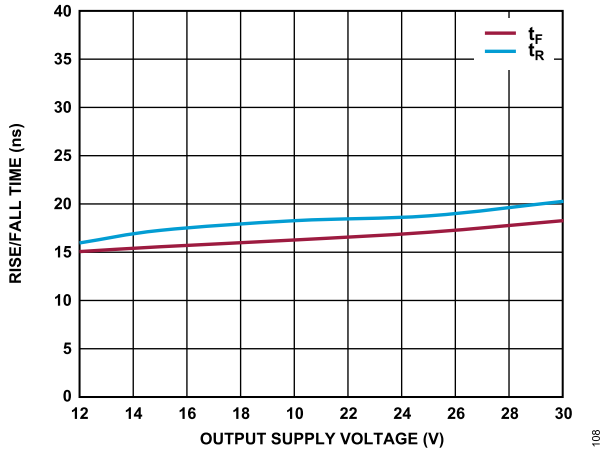

Figure 12. Rise and Fall Time vs. Output Supply Voltage (V_{DD2}), V_{DD1} = 5 V, 2 nF Load, R_G = 3.6 Ω

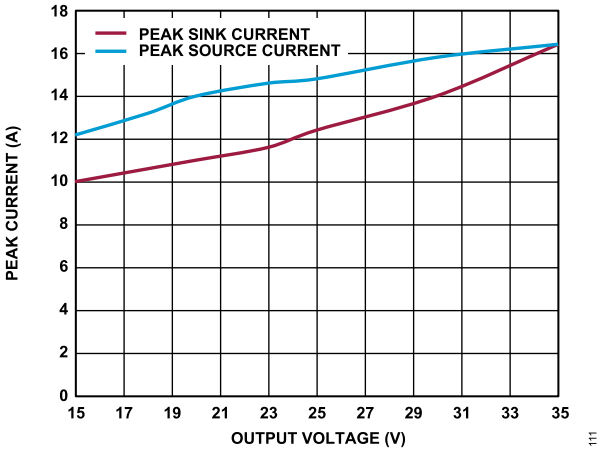

Figure 15. Peak Current vs. Output Voltage, 0 Ω Series Gate Resistor

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4146 SiC gate driver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide an optimal high frequency bypass. On the output power supply pin, V_{DD2}, it is recommended to add 10 µF capacitors from V_{DD2} to GND_2 and from GND_2 to V_{SS2} to provide the charge required to drive the gate capacitance at the ADuM4146 outputs. Adding another 10 µF capacitor from V_{DD2} to V_{SS2} can improve decoupling further. On the output supply pin, avoid the use of vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 5 mm.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay describes the time that it takes a logic signal to propagate through a component. The propagation delay to a low output can differ from the propagation delay to a high output. The ADuM4146 specifies t_{DLH} as the time between the rising input high logic threshold (V_{IH}) to the output rising 10% threshold (see Figure 16). Likewise, the falling propagation delay (t_{DHL}) is defined as the time between the input falling logic low threshold (V_{IL}) and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

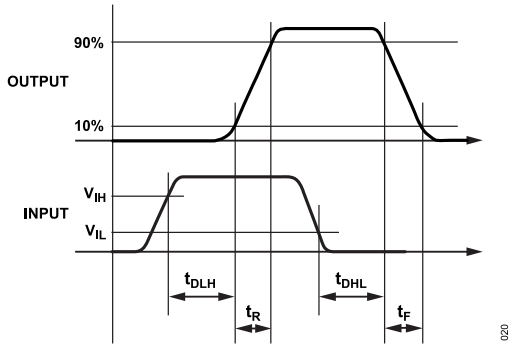

Figure 16. Propagation Delay Parameters

The propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4146 components operating under the same temperature, input voltage, and load conditions.

PROTECTION FEATURES

Fault Reporting

The ADuM4146 provides protection for faults that may occur during the operation of a SiC MOSFET. The primary fault condition is desaturation. If saturation is detected, the ADuM4146 shuts down the gate drive and asserts $\overline{FAULT}$ low. The output remains disabled until $\overline{RESET}$ is brought low for more than 500 ns and then brought high. $\overline{FAULT}$ resets to high on the falling edge of $\overline{RESET}$.

While $\overline{RESET}$ remains held low, the output remains disabled. The $\overline{RESET}$ pin has an internal, 300 kΩ pull-down resistor.

Desaturation Detection

Occasionally, component failures or faults occur with the circuitry connected to the SiC MOSFET connected to the ADuM4146. Examples include shorts in the inductor and motor windings or shorts to power and ground buses. The resulting excess in current flow causes the SiC MOSFET to have excess voltage from drain to source. To detect this condition and reduce the likelihood of damage to the MOSFET, a threshold circuit is used on the ADuM4146. If the DESAT pin exceeds the desaturation threshold ($V_{DESAT, TH}$) of 9.2 V for Grade B or 3.5 V for Grade A and Grade C while the high-side driver is on, the ADuM4146 enters the failure state and turns the SiC MOSFET off. At this time, the $\overline{FAULT}$ pin is brought low. An internal current source of 500 µA is provided, as well as the option to boost the charging current using external current sources or pull-up resistors. The ADuM4146 has a built-in blanking time to prevent false triggering when the SiC MOSFET first turns on. The time between desaturation detection and reporting a desaturation fault to the $\overline{FAULT}$ pin is less than 2 µs (t_{REPORT}). Bring $\overline{RESET}$ low to clear the fault. The $\overline{RESET}$ pin has a 500 ns debounce (t_{DEB_RESET}). The time, t_{MASK}, shown in Figure 17, provides a 300 ns masking time that keeps the internal switch that grounds the blanking capacitor tied low for the initial portion of the SiC MOSFET on time.

APPLICATIONS INFORMATION

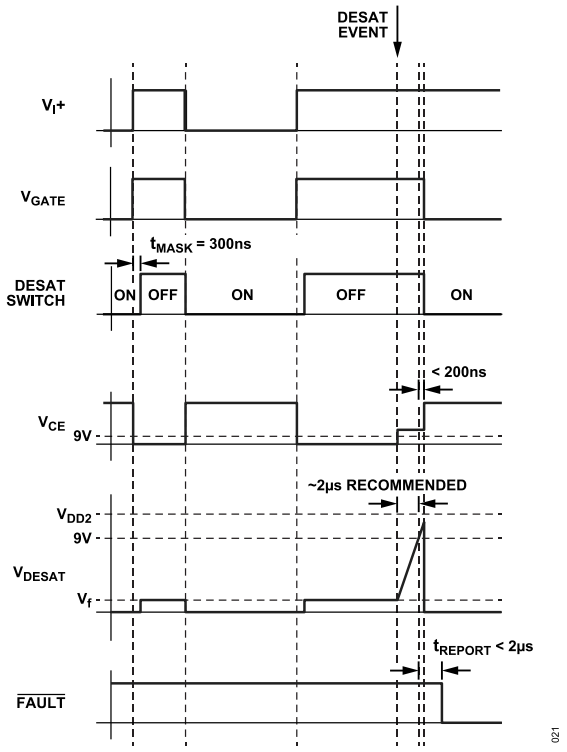

Figure 17. Desaturation Detection Timing Diagram

For the following design example, see the schematic shown in Figure 22 along with the waveforms in Figure 17. Under normal operation, during SiC MOSFET off times, the voltage across the SiC MOSFET, V_{CE}, rises to the rail voltage supplied to the system. In this case, the blocking diode shuts off, protecting the ADuM4146 from high voltages. During the off time, the internal desaturation switch is on and accepting the current going through the blanking resistor, R_{BLANK}, which allows the blanking capacitor, C_{BLANK}, to remain at a low voltage. For the first 300 ns of the SiC MOSFET on time, the DESAT switch remains on, clamping the DESAT pin voltage low. After the 300 ns delay time, the DESAT pin is released, and the DESAT pin is allowed to rise towards V_{DD2} either by the internal current source on the DESAT pin, or additionally with an optional external pull-up, R_{BLANK}, to increase the current drive if it is not clamped by the collector or drain of the switch being driven. The desaturation resistor (R_{DESAT}) is chosen to dampen the current at this time, which is typically selected around 100 Ω to 2 kΩ. Select the blocking diode to block more than the high rail voltage on the collector of the SiC MOSFET and to be a fast recovery diode.

In the case of a desaturation event, V_{CE} rises above the 9 V threshold in the desaturation detection circuit. If no R_{BLANK} resistor is used to increase the blanking current, the voltage on C_{BLANK} rises at a rate of 500 µA (typical) divided by the C_{BLANK} capacitance. Depending on the SiC MOSFET specifications, a blanking time of approximately 2 µs is a typical design choice. When the DESAT pin rises more than the 9 V threshold, a fault registers, and within 200 ns the gate output drives low. The output is brought low using the N channel FET (NFET) fault MOSFET, which is approximately 35 times more resistive than the internal gate driver NFET, to perform a soft shutdown to reduce the chance of an overvoltage spike on the SiC MOSFET during an abrupt turn off event. Within 2 µs, the fault is communicated back to the primary side $\overline{\text{FAULT}}$ pin. To clear the fault, a reset is required.

Miller Clamp

The ADuM4146 has an integrated Miller clamp to reduce voltage spikes on the SiC MOSFET gate caused by the Miller capacitance during the turn off of the SiC MOSFET. When the input gate signal calls for the SiC MOSFET to turn off (driven low), the Miller clamp MOSFET is initially off. When the voltage on the GATE_SENSE pin (V_{GATE_SENSE}) crosses the 2 V internal voltage reference, as referenced to V_{SS2}, the internal Miller clamp latches on for the remainder of the off time of the SiC MOSFET, creating a second low impedance current path for the gate current to follow. The Miller clamp switch remains on until the input drive signal changes from low to high. An example waveform of the timing is shown in Figure 18.

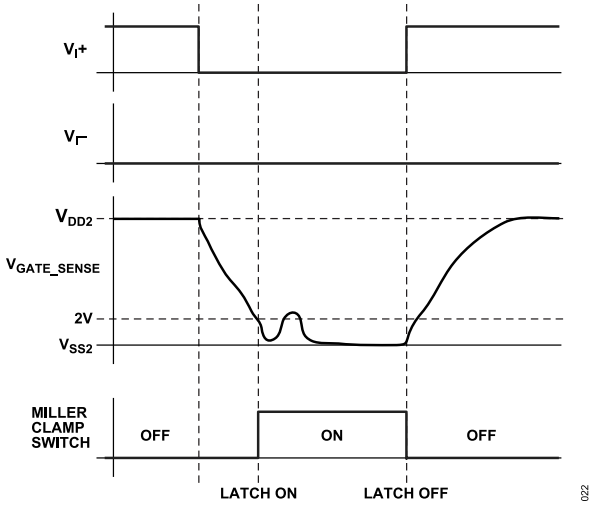

Figure 18. Miller Clamp Example

Thermal Shutdown (TSD)

If the internal temperature of the ADuM4146 exceeds 155°C (typical), the device enters TSD. During the TSD time, the READY pin is brought low on the primary side, and the gate drive is disabled. When TSD occurs, the device does not leave TSD until the internal temperature drops below 125°C (typical), at which time, the READY pin returns to high, and the device exits shutdown.

Undervoltage Lockout (UVLO) Faults

UVLO faults occur when the supply voltages are less than the specified UVLO threshold values. During a UVLO event on either the primary side or secondary side, the READY pin goes low, and the gate drive is disabled. When the UVLO condition is removed, the device resumes operation, and the READY pin goes high.

APPLICATIONS INFORMATION

READY Pin

The open-drain READY pin is an output that confirms that communication between the primary to secondary sides is active. The READY pin remains high when there are no UVLO or TSD events present. When the READY pin is low, the SiC MOSFET gate is driven low.

Table 11. READY Pin Logic Table

UVLO	TSD	READY Pin Output
No	No	High
Yes	No	Low
No	Yes	Low
Yes	Yes	Low

$\overline{\text{FAULT}}$ and $\overline{\text{RESET}}$ Pins

The open-drain $\overline{\text{FAULT}}$ output pin communicates when a desaturation fault occurs. When the $\overline{\text{FAULT}}$ pin is low, the SiC MOSFET gate is driven low. If a desaturation event occurs, the $\overline{\text{RESET}}$ pin must be driven low for at least 500 ns, then high to return operation to the SiC MOSFET gate drive.

The $\overline{\text{RESET}}$ pin has an internal 300 kΩ (typical) pull-down resistor. The $\overline{\text{RESET}}$ pin accepts CMOS level logic. When the $\overline{\text{RESET}}$ pin is held low after a 500 ns debounce time, any faults on the $\overline{\text{RESET}}$ pin are cleared. While the $\overline{\text{RESET}}$ pin is held low, the switch on V_{OUT_OFF} is closed, bringing the gate voltage of the SiC MOSFET low. When $\overline{\text{RESET}}$ is brought high and no fault exists, the device resumes operation (see Figure 19).

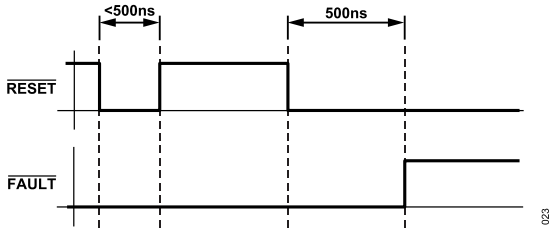

Figure 19. Timing

V_I+ and V_I− Operation

The ADuM4146 has two drive inputs, V_I+ and V_I−, to control the SiC MOSFET gate drive signals, V_{OUT_ON} and V_{OUT_OFF} (see Figure 20). Both the V_I+ and V_I− inputs use CMOS logic level inputs. The input logic of the V_I+ and V_I− pins can be controlled by either asserting the V_I+ pin high or the V_I− pin low. With the V_I− pin low, the V_I+ pin accepts positive logic. If V_I+ is held high, the V_I− pin accepts negative logic. If a fault is asserted, transmission is blocked until the fault is cleared by the $\overline{\text{RESET}}$ pin.

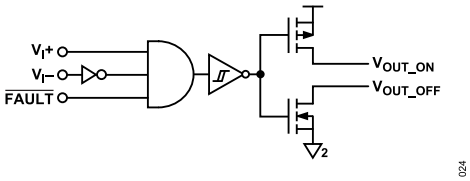

Figure 20. V_I+ and V_I− Block Diagram

The minimum pulse width is the minimum period in which the timing specifications are guaranteed.

Gate Resistance Selection

The ADuM4146 provides two output nodes for the driving of a SiC MOSFET. The benefit of this approach is that the user can select two different series resistances for the turn on and turn off of the SiC MOSFET. It is generally desired to have the turn off occur faster than the turn on. To select the series resistance, decide what the maximum allowed peak current, I_{PEAK}, is for the SiC MOSFET. Knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external resistor can be chosen.

$$I_{PEAK} = (V_{DD2} - V_{SS2})/(R_{DSON_N} + R_{GOFF})$$

For example, if the turn off peak current is 4 A, with a (V_{DD2} − V_{SS2}) of 18 V,

$$R_{GOFF} = ((V_{DD2} - V_{SS2}) - I_{PEAK} \times R_{DSON_N})/I_{PEAK}$$

$$R_{GOFF} = (18\ V - 4\ A \times 0.6\ \Omega)/4\ A = 3.9\ \Omega$$

After R_{GOFF} is selected, a slightly larger R_{GON} can be selected to arrive at a slower turn on time.

POWER DISSIPATION

During the driving of a SiC MOSFET gate, the gate driver must dissipate power. This power is not insignificant and can lead to TSD if considerations are not made. The gate of a SiC MOSFET can be roughly simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance (C_{ISS}) of a given SiC MOSFET and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation (P_{DISS}) in the system due to switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - V_{SS2})^2 \times f_S$$

where:
$C_{EST} = C_{ISS} \times 5$.
f_S is the switching frequency of the SiC MOSFET.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4146 chip.

APPLICATIONS INFORMATION

$P_{DISS_ADuM4146} = P_{DISS} \times 0.5(R_{DSON_P}/(R_{GON} + R_{DSON_P}) + R_{DSON_N}/(R_{GOFF} + R_{DSON_N}))$

where:
$P_{DISS_ADuM4146}$ is the power dissipation of the ADuM4146.

Taking the power dissipation found inside the chip and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4146 experiences.

$T_{ADuM4146} = \theta_{JA} \times P_{DISS_ADuM4146} + T_{AMB}$

where:
$T_{ADuM4146}$ is the junction temperature of the ADuM4146.
T_{AMB} is the ambient temperature.

For the ADuM4146 to remain within specification, $T_{ADuM4146}$ must not exceed 125°C. If
$T_{ADuM4146}$ exceeds 155°C (typical), the device enters thermal shutdown.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation, as well as on the materials and material interfaces.

Two types of insulation degradation are of primary interest: breakdown along surfaces exposed to air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM4146 isolator are presented in Table 8.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress because this stress reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{{V_{AC\ RMS}}^2 + {V_{DC}}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

APPLICATIONS INFORMATION

Calculation and Use of Parameters Example

The following is an example that frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms, and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage clearance and lifetime of a device, see Figure 21 and the following equations.

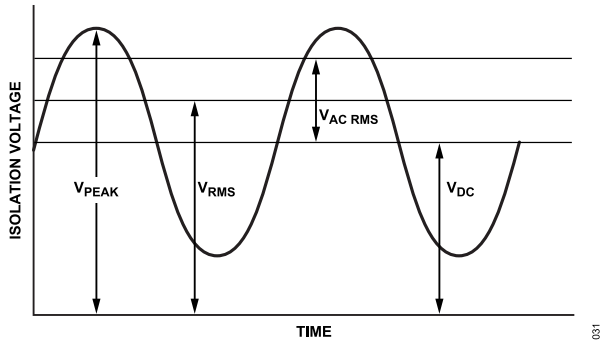

Figure 21. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V rms

This working voltage of 466 V rms is used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. The ac rms voltage can be obtained from Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\ RMS}$ = 240 V rms

In this case, $V_{AC\ RMS}$ is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value of the ac waveform is compared to the limits for working voltage in Table 8 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 20 year service lifetime.

Note that the dc working voltage limit in Table 8 is set by the creepage of the package as specified in IEC 60664-1. This value may differ for specific system level standards.

TYPICAL APPLICATION

The typical application schematic in Figure 22 shows a bipolar setup with an additional R_{BLANK} resistor to increase the charging current of the blanking capacitor (C_{BLANK}) for desaturation detection. The R_{BLANK} resistor is optional. If unipolar operation is desired, the V_{SS2} supply can be removed and must be tied to GND_2.

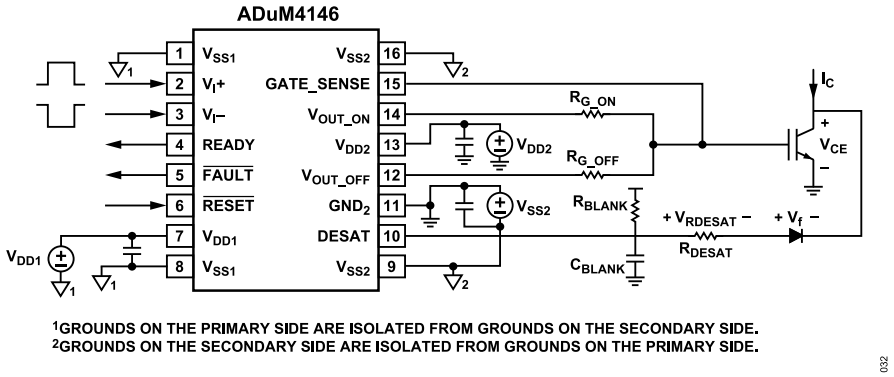

Figure 22. Typical Application Schematic

OUTLINE DIMENSIONS

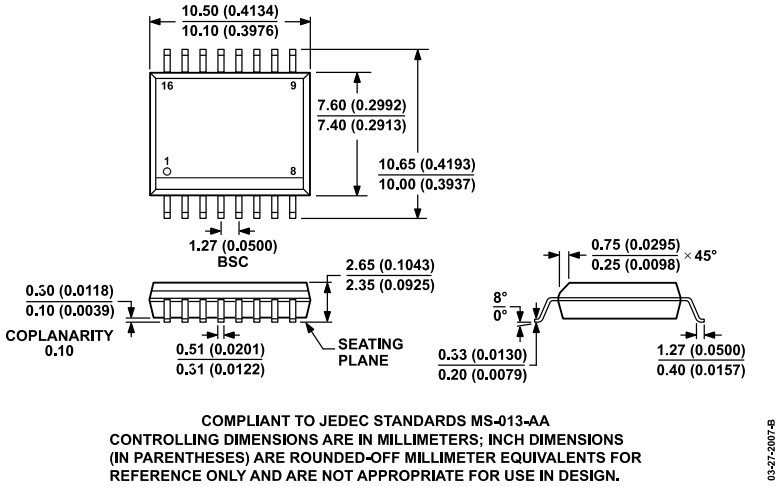

Figure 23. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

Updated: March 24, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM4146ARWZ	-40°C to +125°C	16-Lead SOIC Wide	Tube, 47	RW-16
ADUM4146ARWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM4146BRWZ	-40°C to +125°C	16-Lead SOIC Wide	Tube, 47	RW-16
ADUM4146BRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16
ADUM4146CRWZ	-40°C to +125°C	16-Lead SOIC Wide	Tube, 47	RW-16
ADUM4146CRWZ-RL	-40°C to +125°C	16-Lead SOIC Wide	Reel, 1000	RW-16

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuM4146EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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