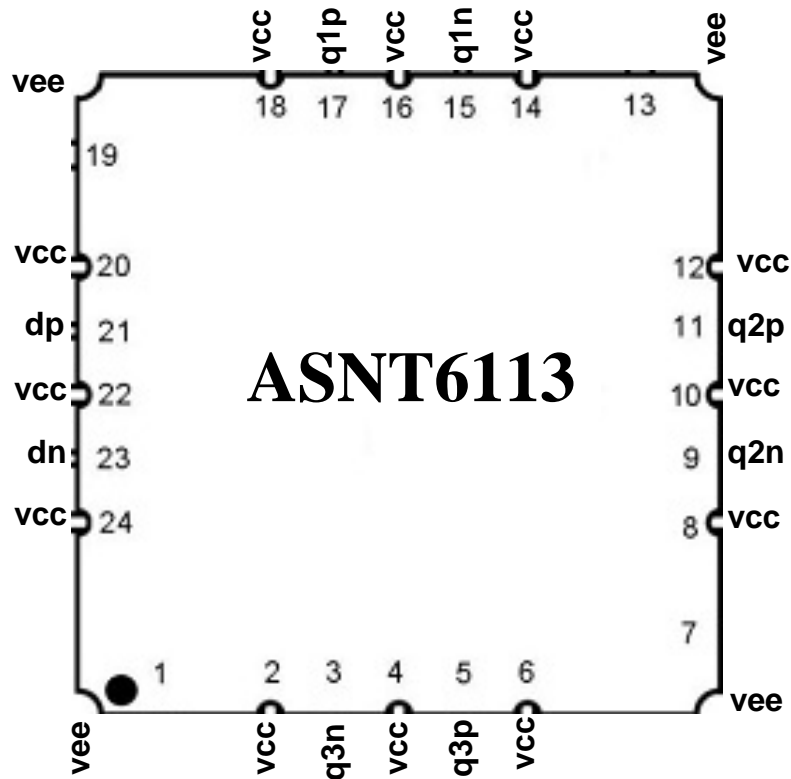




ASNT6113-KHC DC-25GHz 1-to-3 Analog Signal Splitter

- DC to 25GHz broadband linear signal splitter
- One differential CML-type input port and three phase-matched differential CML-type output ports
- Differential input linearity range up to 1000mV p-p
- Differential gain of approximately 0dB
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.3V or -3.3V power supply
- Power consumption: 1.0W
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package





DESCRIPTION

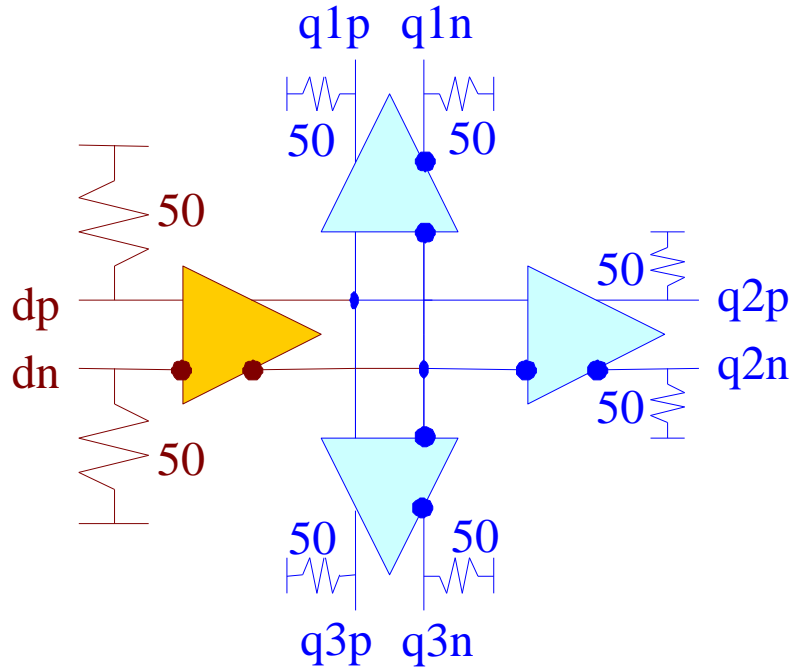


Fig. 1. Functional Block Diagram

The temperature stable ASNT6113-KHC 1-to-3 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. The IC shown in Fig. 1 can receive a broad-band analog signal at its differential input dp/dn and effectively distribute it to three separate phase matched differential outputs $q1p/q1n$, $q2p/q2n$, $q3p/q3n$ with a nominal gain of $0dB$.

The part's I/O's support the CML logic interface with on chip 50Ω termination to VCC and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50Ω DC termination to VCC .

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply ($VCC = 0.0V = \text{ground}$ and $VEE = -3.3V$), or positive supply ($VCC = +3.3V$ and $VEE = 0.0V = \text{ground}$). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $VCC = 0.0V$ and $VEE = -3.3V$.



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		1.1	W
RF Input Voltage Swing (SE)		1.4	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTION

TERMINAL			DESCRIPTION
Name	No.	Type	
dp	21	CML input	Differential high speed data inputs with internal SE 500hm termination to vcc
dn	23		
q1p	17	CML output	Differential high speed data outputs with internal SE 500hm termination to vcc. Require external SE 500hm termination to vcc
q1n	15		
q2p	11	CML output	
q2n	9		
q3p	5	CML output	
q3n	3		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19



ELECTRICAL CHARACTERISTICS

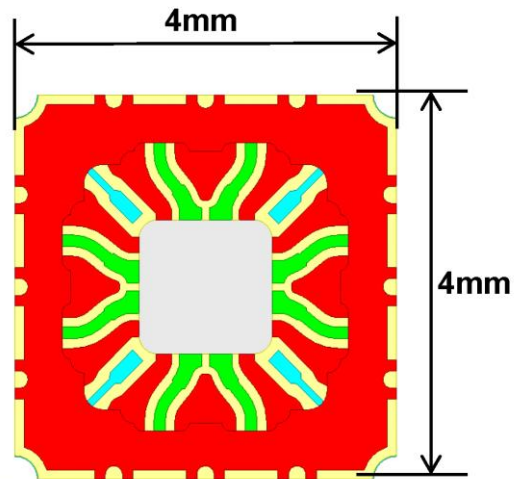
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}		300		mA	
Power consumption		1000		mW	
Junction temperature	-25	50	125	°C	
Input Analog (dp/dn)					
Bandwidth	DC		25	GHz	-3dB
Common mode level	vcc-0.6	vcc-0.5	vcc-0.4	mV	
Input Noise Density		1.5		nV/sqrt(Hz)	
S ₁₁		-10		dB	DC to 30GHz
Output Analog (q1p/q1n, q2p/q2n, q3p/q3n)					
Common mode level		vcc-0.55		V	With external 50Ohm DC termination
S ₂₂		-8		dB	DC to 30GHz
Small Signal Differential Gain		0		dB	at 10GHz
Output referred 1dB Compression Point		2.7		dBm	Single-Ended, 20GHz
THD		0.2		%	

PACKAGE INFORMATION

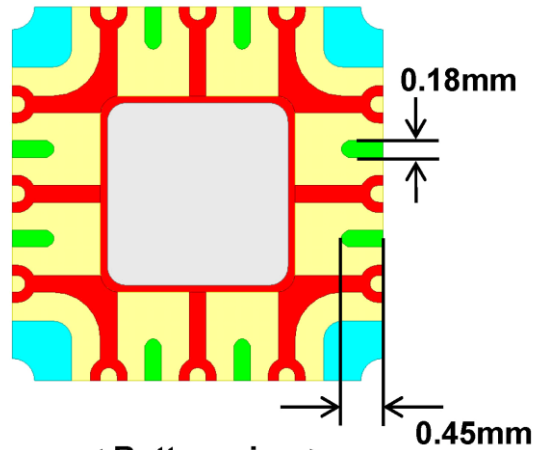
The chip die is housed in a custom 24-pin CQFN package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6113-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.



< Top view >



< Bottom view >

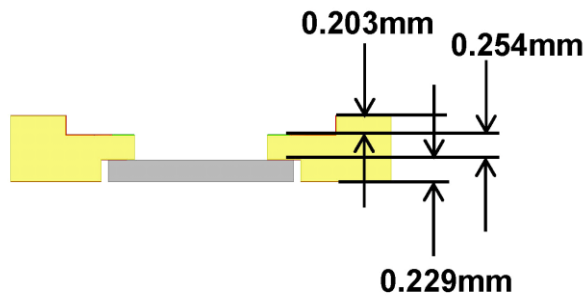


Fig. 2. CQFN24-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
1.1.2	08-2021	Updated RoHS Statement
1.0.2	04-2020	Updated Package information section
1.0.1	04-2020	First release