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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E13RG62424LWAM450-N

Overview:

- 1.3-inch TFT: 240x240 (35.9x39.7)
- 16/18- bit RGB
- 8/9/16/18-bit MCU
- 3/4SPI Interface
- White LED back-light
- Transmissive
- No Touch Panel
- 450 NITS
- Controller: ST7789V
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses l·y amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit amd back-light unit. The resolution of a 1.3" TFT-LCD contains 240X240 pixels and can display up to 65K/262K colors.

Features

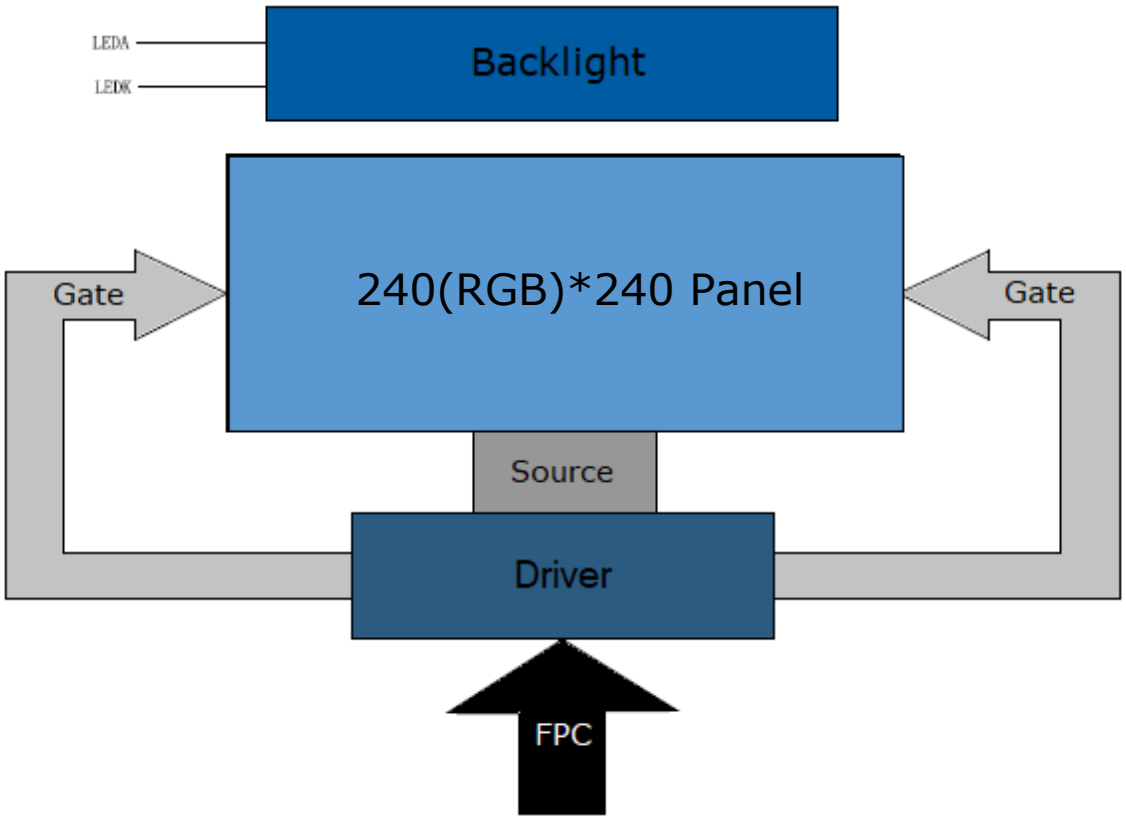
Low Input Voltage: 3.3V (TYP)
Display Colors of TFT LCD: 65K/262K colors
TFT Interface: 8/9/16/18Bit MCU;
3/4SPI+16/18Bit RGB
3-line/4-line Serial Interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area (AA)	32.40(H) *32.40(V) (1.3inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*240	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.135 (H) x 0.135 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

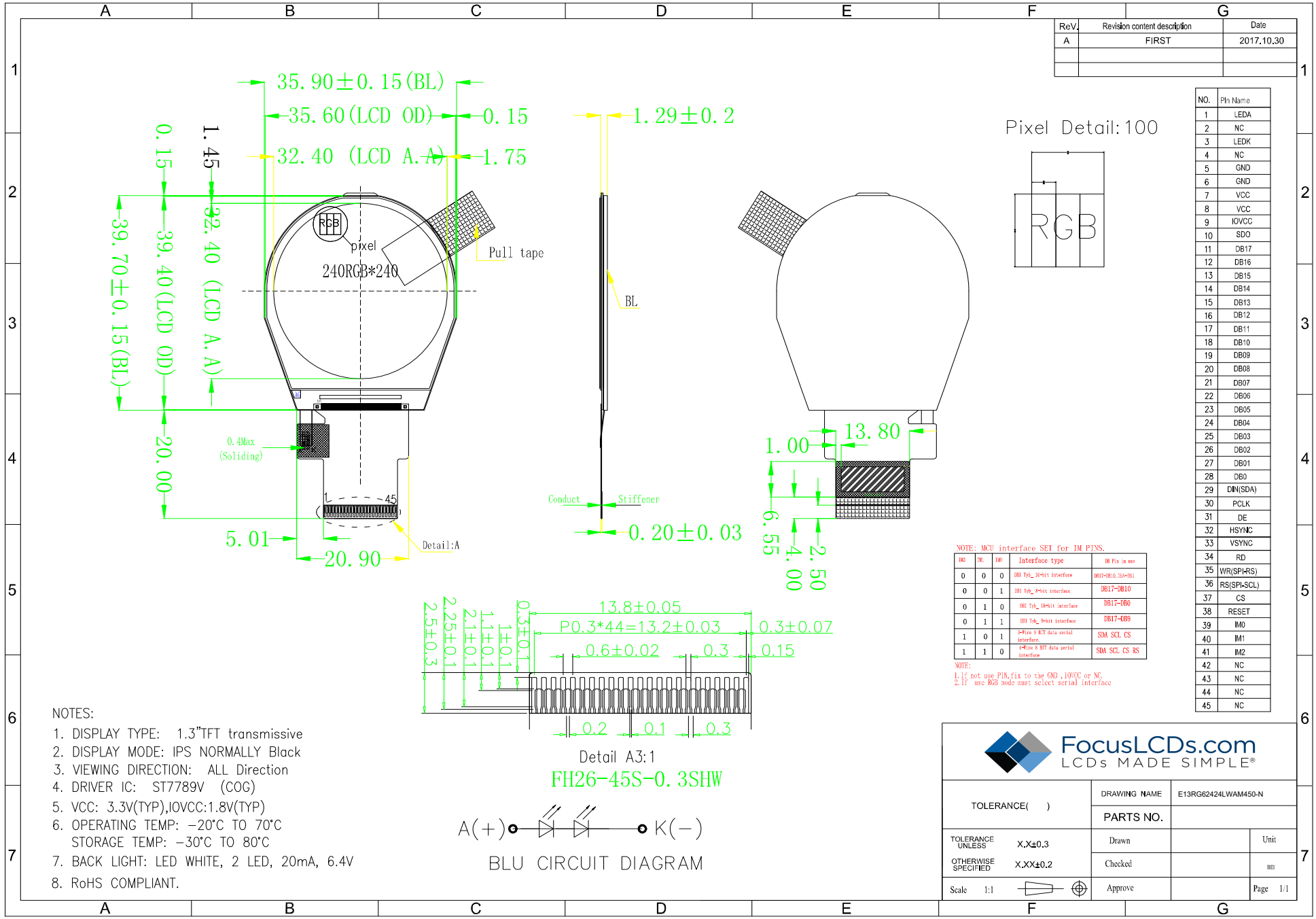
Mechanical Information

Item		Min	Typ	Max	Unit	Note
Module size	Horizontal(H)		35.90		mm	-
	Vertical(V)		39.70		mm	-
	Depth(D)		1.29		mm	-
Weight			4.0		g	-

1. Block Diagram



2. Outline Dimensions



ReV.	Revision content description	Date
A	FIRST	2017.10.30

NO.	Pin Name
1	LEDA
2	NC
3	LEDK
4	NC
5	GND
6	GND
7	VCC
8	VCC
9	IOVCC
10	SDO
11	DB17
12	DB16
13	DB15
14	DB14
15	DB13
16	DB12
17	DB11
18	DB10
19	DB09
20	DB08
21	DB07
22	DB06
23	DB05
24	DB04
25	DB03
26	DB02
27	DB01
28	DB0
29	DIN(SDA)
30	PCLK
31	DE
32	HSYNC
33	VSYNC
34	RD
35	WR(SPI-RS)
36	RS(SPI-SCL)
37	CS
38	RESET
39	IM0
40	IM1
41	IM2
42	NC
43	NC
44	NC
45	NC

NOTE: MCU interface SET for IM PINS.

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	8bit Typ. 16-bit interface	DB17-DB10, DB8-DB1
0	0	1	8bit Typ. 8-bit interface	DB17-DB10
0	1	0	9bit Typ. 18-bit interface	DB17-DB0
0	1	1	8bit Typ. 9-bit interface	DB17-DB9
1	0	1	3-Wire 9 BIT data serial interface	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.
2. If use RGB mode must select serial interface

NOTES:
1. DISPLAY TYPE: 1.3"TFT transmissive
2. DISPLAY MODE: IPS NORMALLY Black
3. VIEWING DIRECTION: ALL Direction
4. DRIVER IC: ST7789V (COG)
5. VCC: 3.3V(TYP),IOVCC:1.8V(TYP)
6. OPERATING TEMP: −20°C TO 70°C
   STORAGE TEMP: −30°C TO 80°C
7. BACK LIGHT: LED WHITE, 2 LED, 20mA, 6.4V
8. RoHS COMPLIANT.

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TOLERANCE( )	DRAWING NAME	E13RG62424LWAM450-N	
	PARTS NO.		
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn		Unit
	Checked		mm
Scale 1:1	Approve		Page 1/1

3. Input Terminal Pin Assignment

Recommended Connector: FH26-45S-0.3SHW(05)

NO.	Symbol	Description	I/O
1	LEDA	Anode pin of backlight	P
2	NC	--	--
3	LEDK	Cathode pin of backlight	P
4	NC	--	--
5	GND	Ground	P
6	GND		
7	VCC/VCI	Supply voltage (3.3V).	P
8	VCC/VCI		
9	IOVCC	Supply voltage (1.65-3.3V).	P
10	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. If not used, let this pin open.	O
11-28	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode. Fix to GND level when not in use	I/O
29	DIN(SDA)	When IM3: Low, SPI interface input/output pin. When IM3: High, SPI interface input pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at IOVCC or DGND level	I/O
30	PCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.	I
31	DE	Data enable signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
32	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
33	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at IOVCC or GND when not in use.	I
34	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use.	I
35	WR(SPI-RS)	Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface. Second data lane in 2 data lane serial interface. Fix to IOVCC or GND if not used.	I
36	RS(SPI-SCL)	Display data/command selection pin in parallel interface. This pin is used as serial interface clock. RS='1': Display data. RS='0': Command data. Fix to IOVCC or DGND when not used.	I
37	CS	Chip select input pin ("low" enable). Fix to IOVCC or GND when not used.	I
38	RESET	Reset signal of device. Must be applied to properly initialize the chip.	I
39	IM0	MPU parallel interface bus and serial interface select. If RGB interface, must select serial interface. Fix to IOVCC or GND if not used.	I
40	IM1		I
41	IM2		I
42	NC	--	--
43	NC	--	--
44	NC	--	--
45	NC	--	--

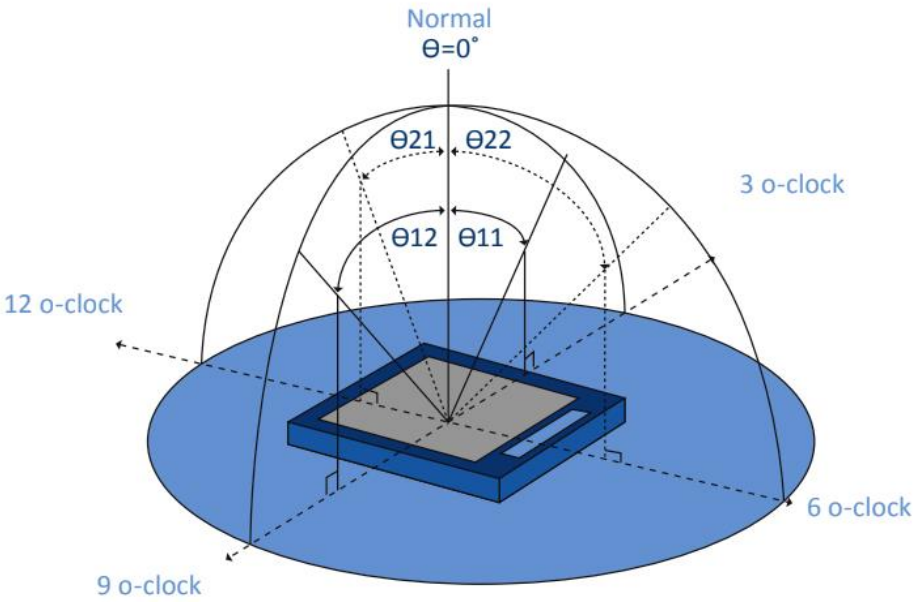
4. LCD Optical Characteristics

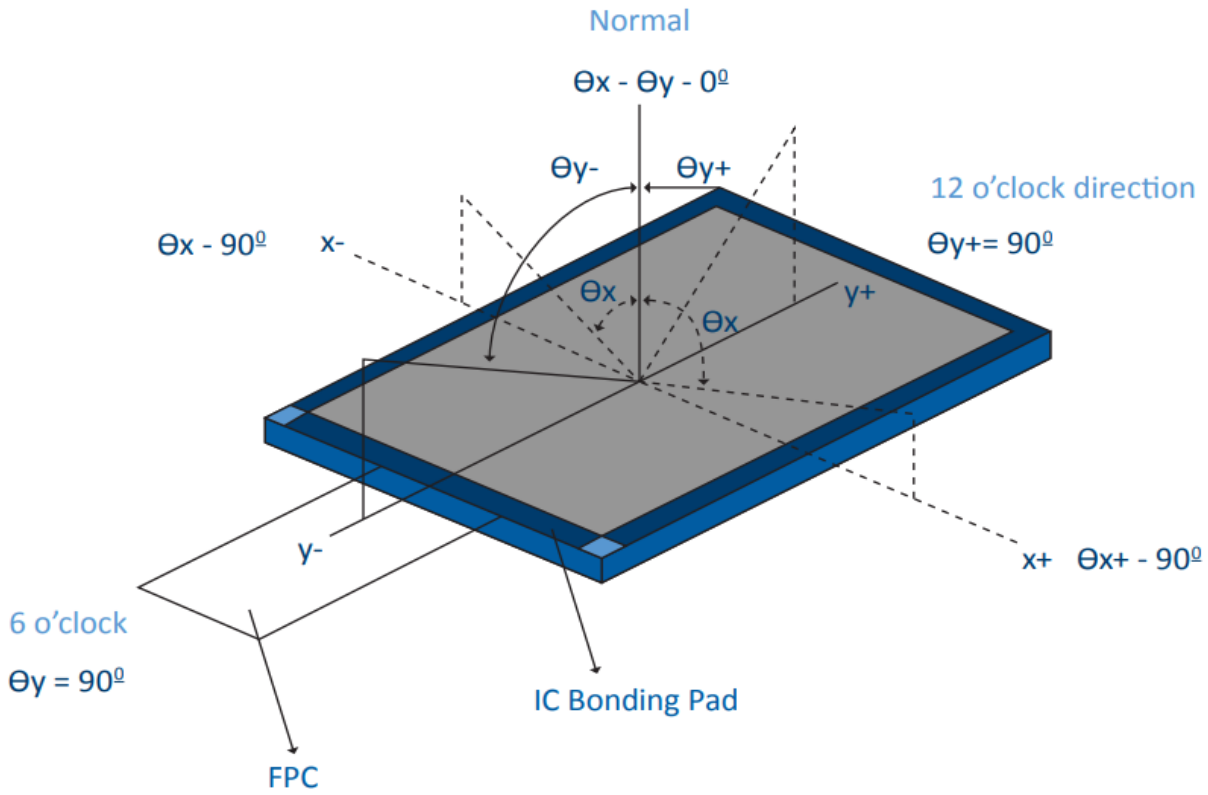
4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	400	600	--		(2)
Response time	Rising+ Falling	T_{R+T_F}		--	35	50	msec	(4)
Color gamut		S (%)		--	60	--	%	(5)
Color Filter Chromaticity	White	W_X		0.2510	0.2910	0.3310		(5)
		W_Y		0.2738	0.3138	0.3538		
	Red	R_X		0.5918	0.6118	0.6318		
		R_Y		0.3202	0.3402	0.3602		
	Green	G_X		0.3094	0.3294	0.3494		
		G_Y		0.5926	0.6126	0.6326		
	Blue	B_X		0.1327	0.1527	0.1727		
		B_Y		0.0467	0.0667	0.0867		
Viewing angle	Hor.	ΘL	CR>10	60	80	--		(1)(6)
		ΘR		60	80	--		
	Ver.	ΘU		60	80	--		
		ΘD		60	80	--		
Option View Direction		ALL						(6)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

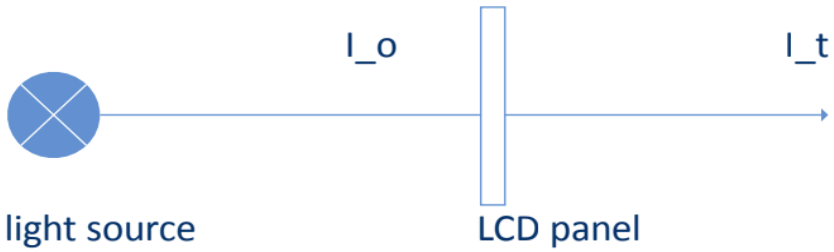




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

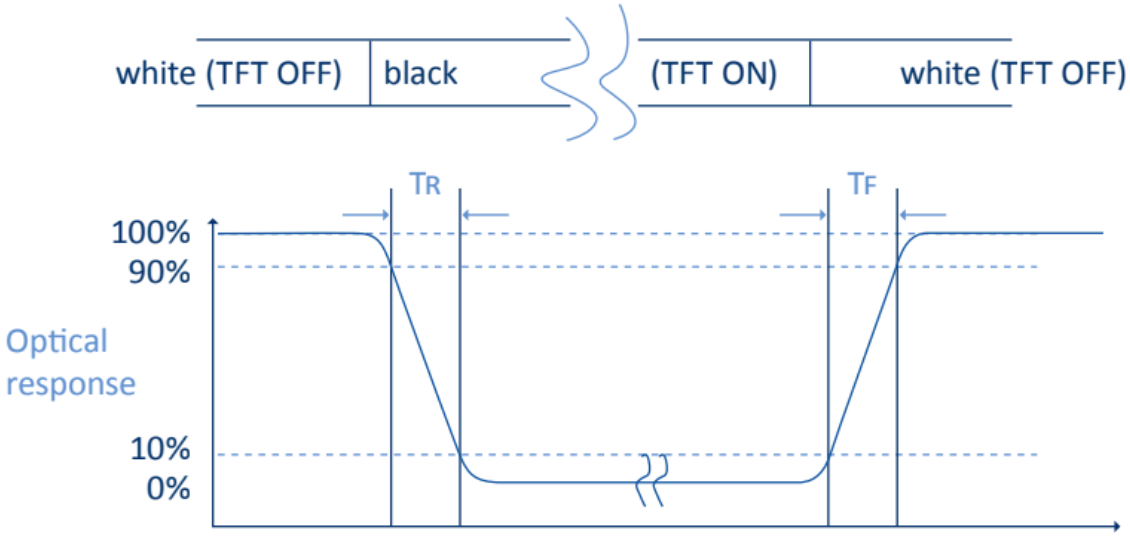


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

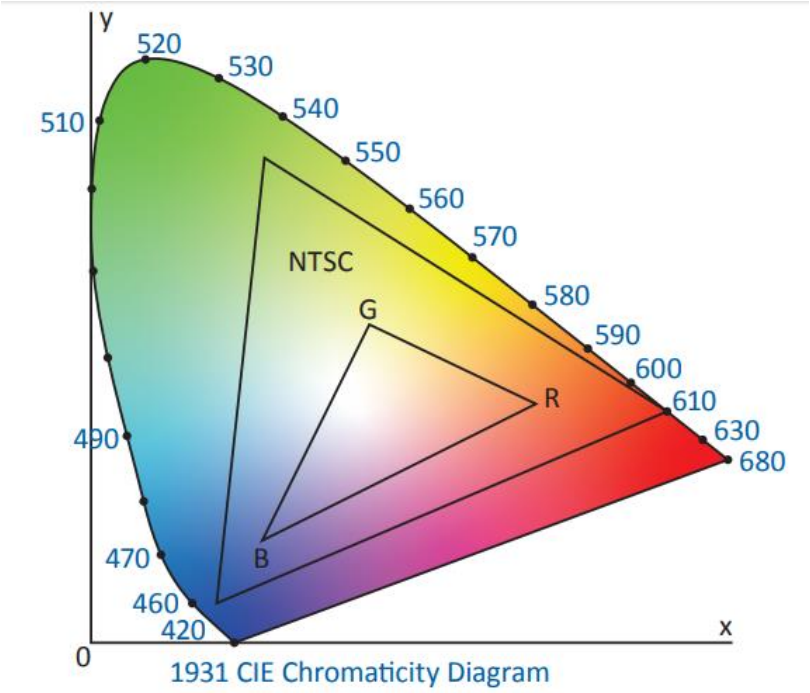
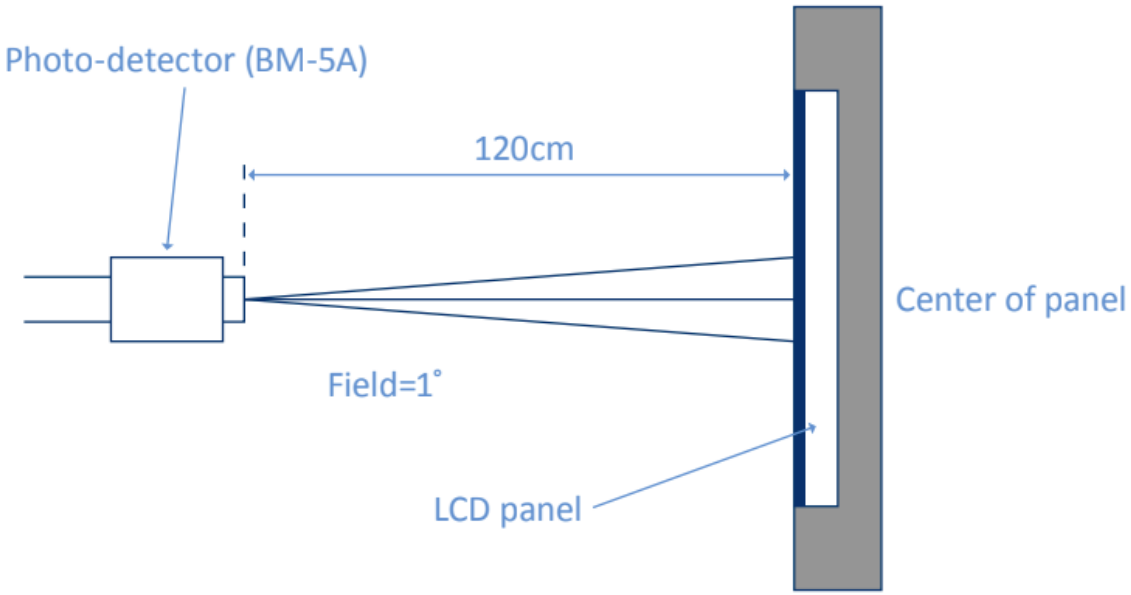


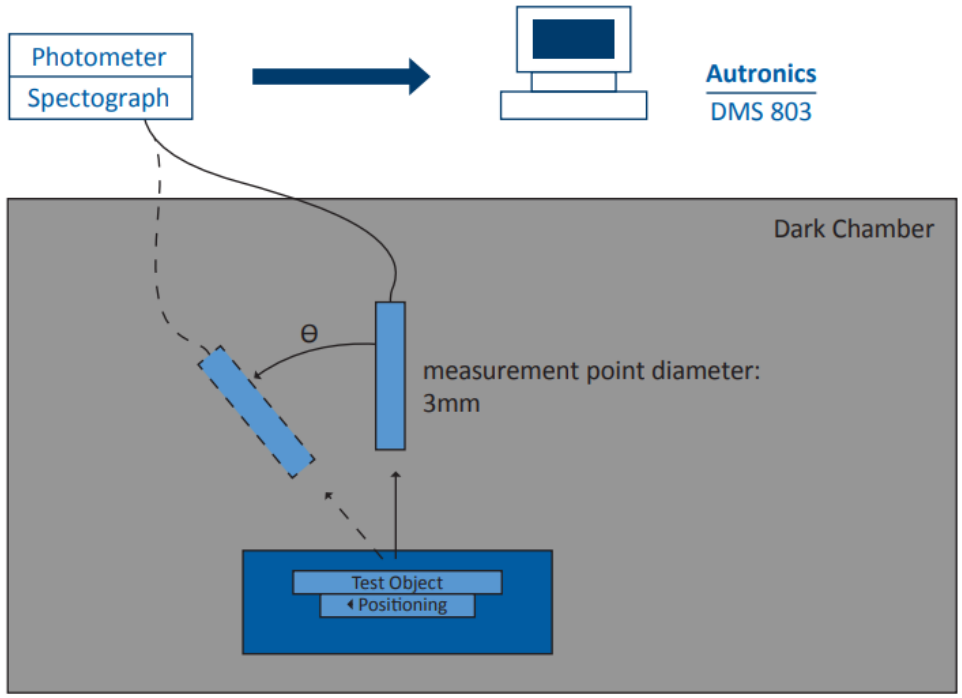
Fig. 1931 CIE chromacity diagram

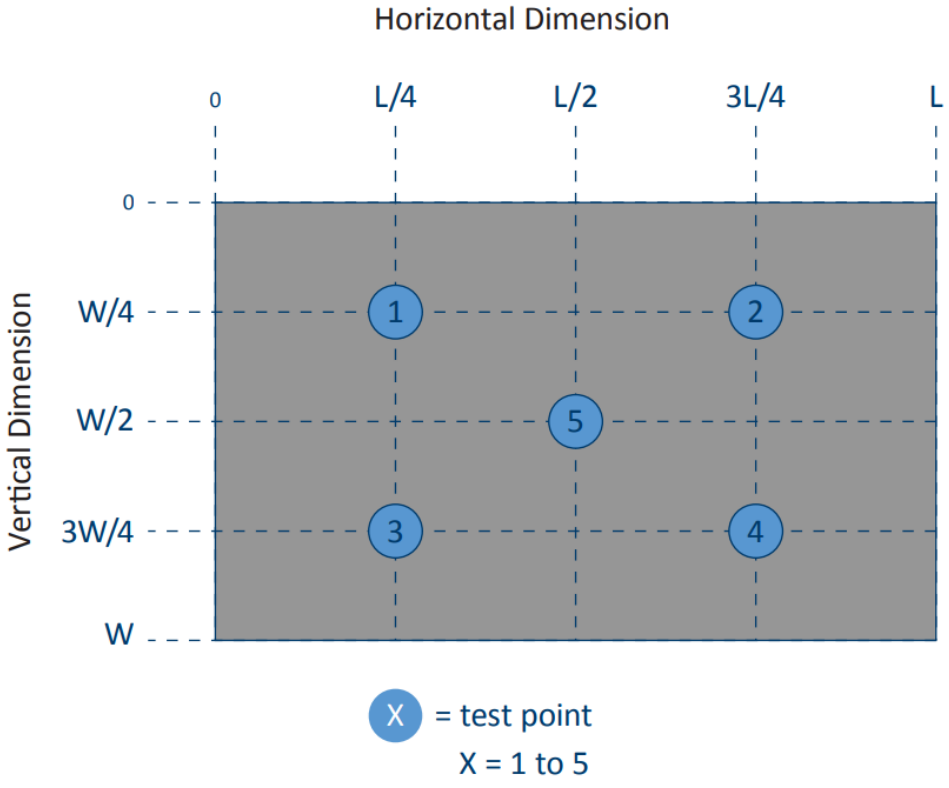
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Interface Operation Voltage	IOVCC	-0.3	4.6	V
Operating temperature	T_{OP}	-20	+70	℃
Storage temperature	T_{ST}	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.4	3.3	3.6	V	
Interface Operation Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current Consumption	IDD	--	8.5	--	mA	
Level input voltage	V_{IH}	0.7 Iovcc		Iovcc	V	
	V_{IL}	GND		0.3 Iovcc	V	
Level output voltage	V_{OH}	0.8 Iovcc		Iovcc	V	
	V_{OL}	GND		0.2 Iovcc	V	

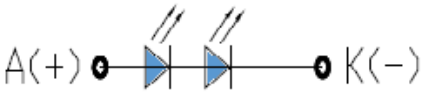
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 2 chips White LED

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	15	20	--	mA	
Forward Voltage	VF	--	6.4	--	V	
LCM Luminance	LV	--	450	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

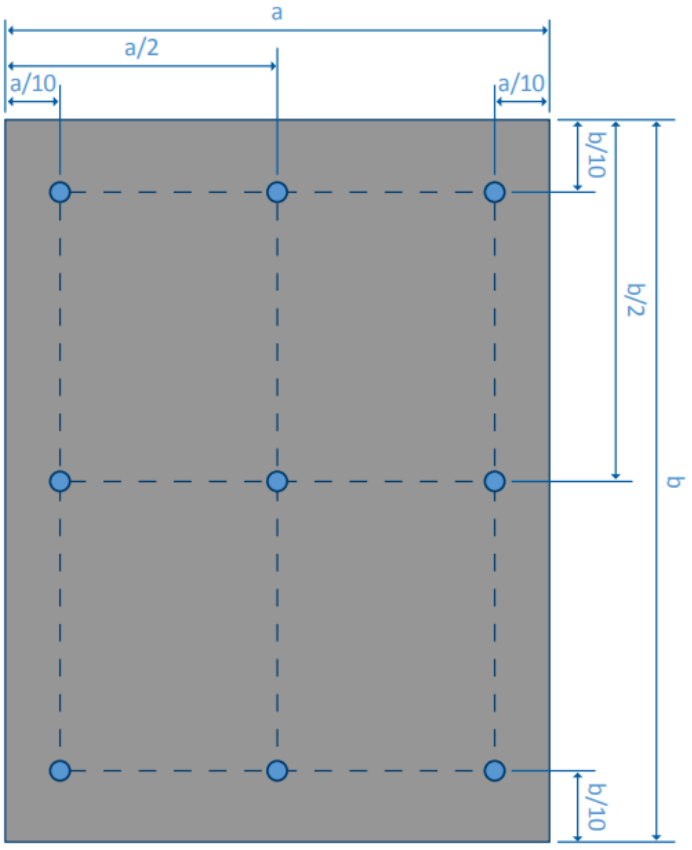
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

6. AC Characteristic

6.1 RGB Interface Characteristics

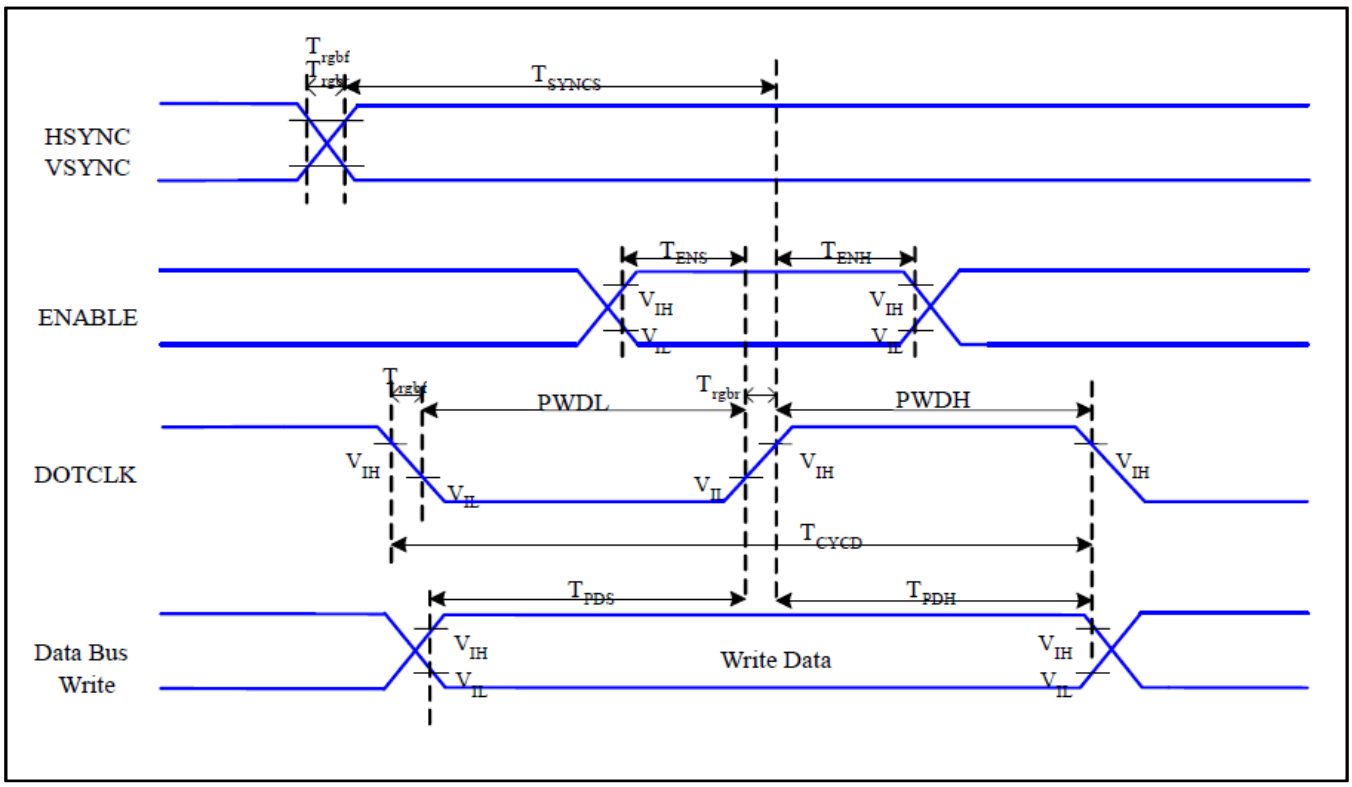


Figure 6.1: RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	20	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK Rise/Fall Time	-	-	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 6.1: 18/16-bit RGB Interface Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	25	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	25	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	55	-	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK Rise/Fall Time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	25	-	ns	
	T_{PDH}	PD Data Hold Time	25	-	ns	

Table 6.2: 8/9-bit RGB Interface Timing Characteristics

6.2 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

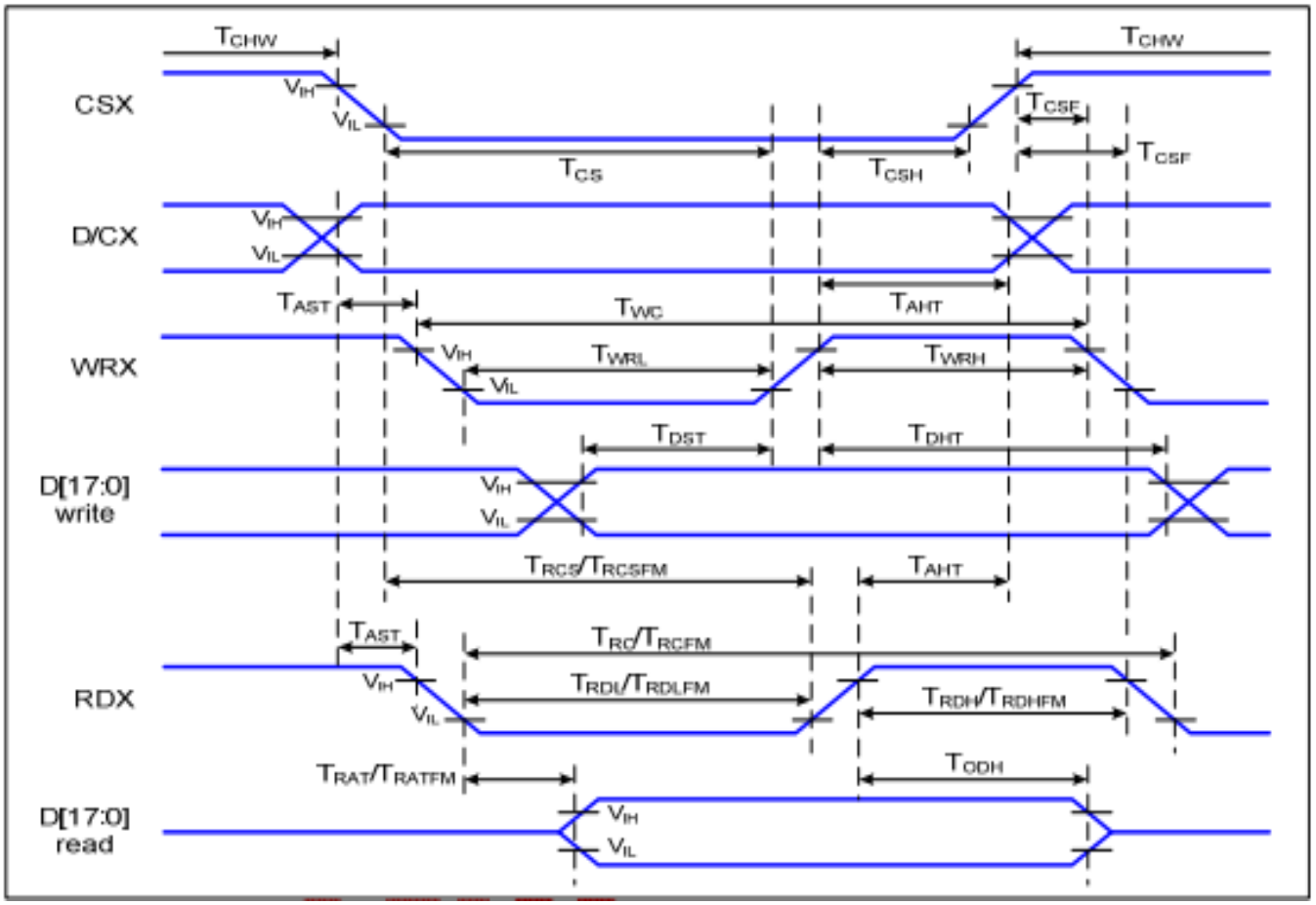
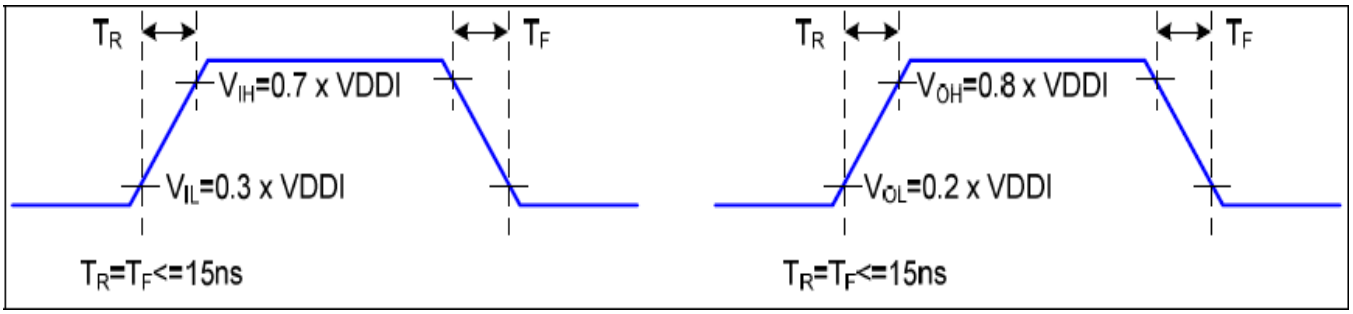


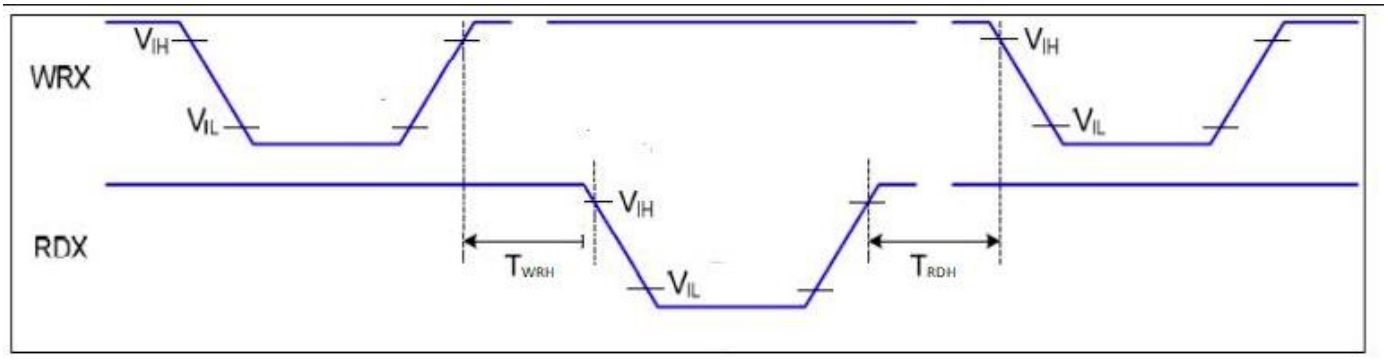
Figure 6.2: Parallel Interface Timing Characteristics (8080-Series MCU Interface)



Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0], D[15:0], D[8:0], D[7:0]	T_{DST}	Data setup time	10		ns	For max CL=30pF For min CL=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 6.3: 8080 Series MCU Parallel Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



6.3 Serial Interface Characteristics (3-line serial)

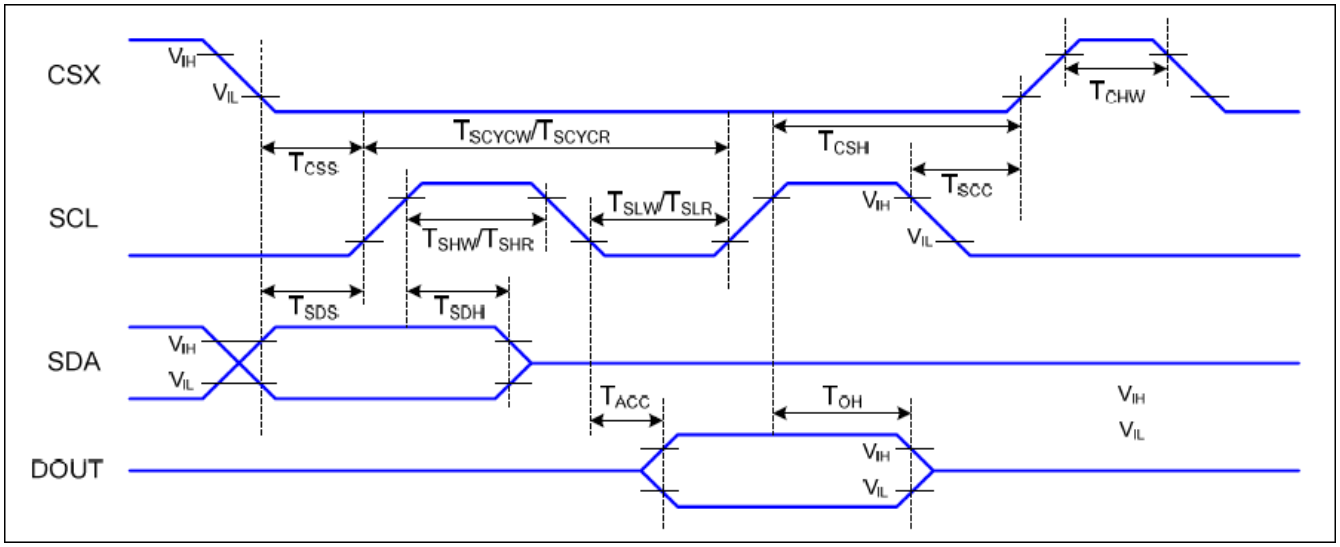


***Figure 6.3: Serial Interface* 3-SPI Timing Diagram**

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C°

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10			
DOUT	T_{ACC}	Access time	10			For max CL=30pF For min CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 6.4: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.4 Serial Interface Characteristics (4-line serial)

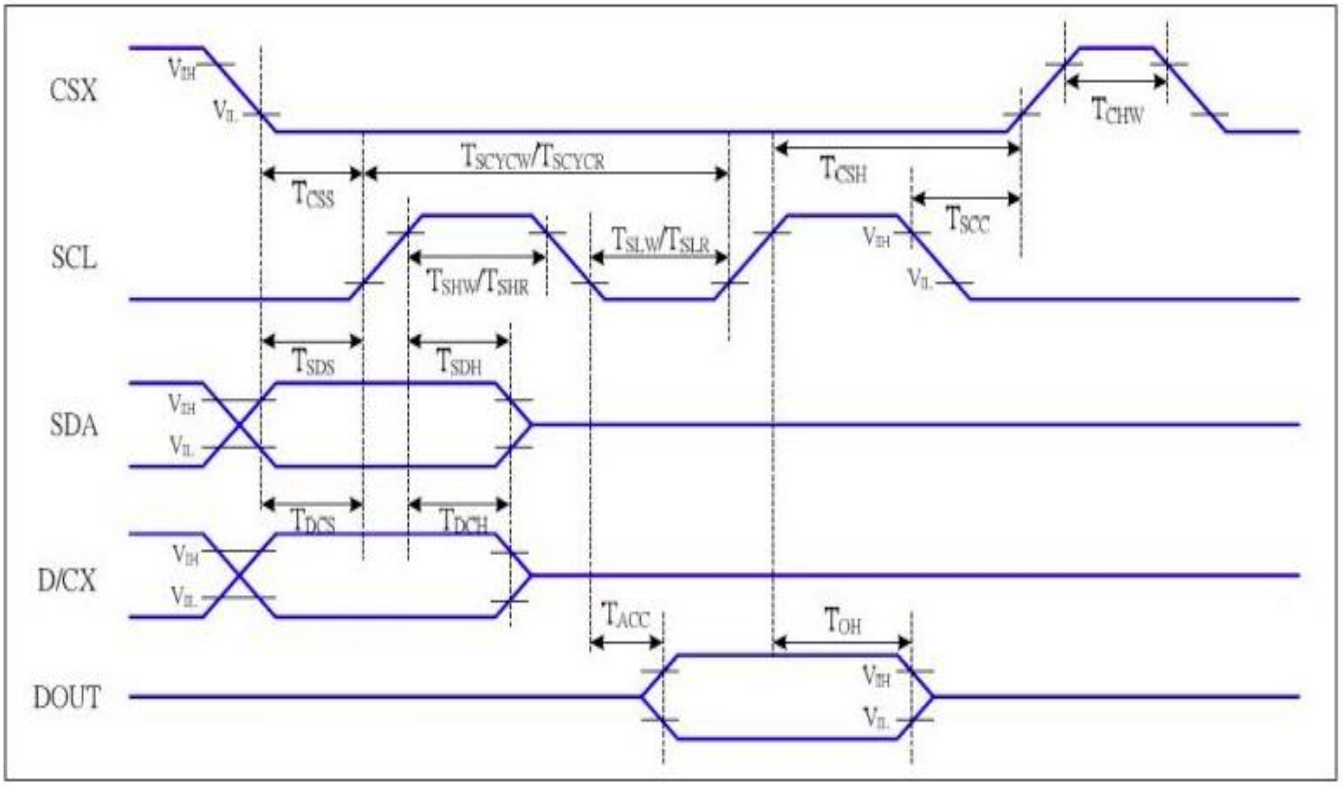


***Figure 6.4: Serial Interface* 4-SPI Timing Diagram**

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	write command & data ram
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	read command & data ram
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For max CL=30pF
	T_{OH}	Output disable time	15	50	ns	For min CL=8pF

Table 6.5: 4-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6.5 Reset Timing

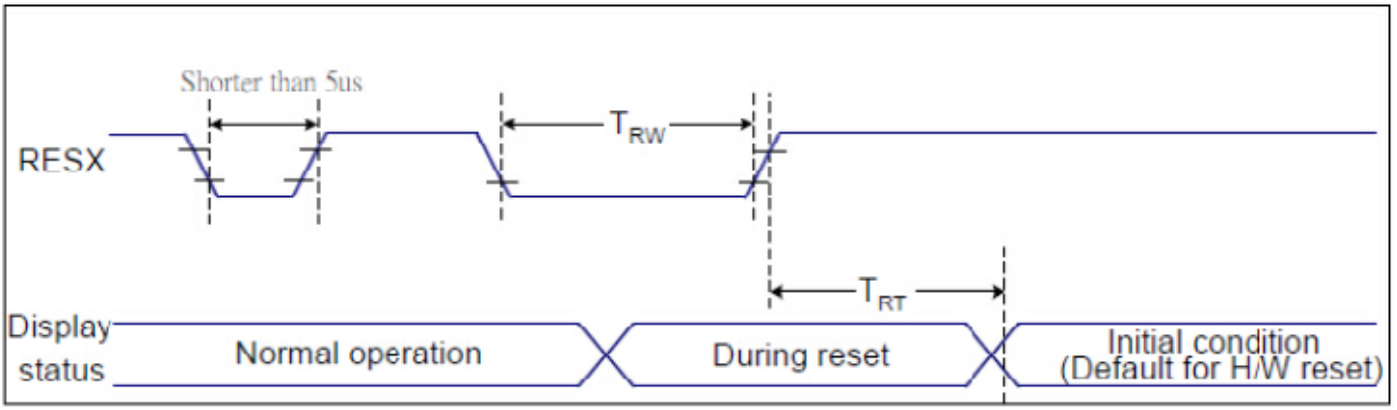


Figure 6.5: Reset Timing

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

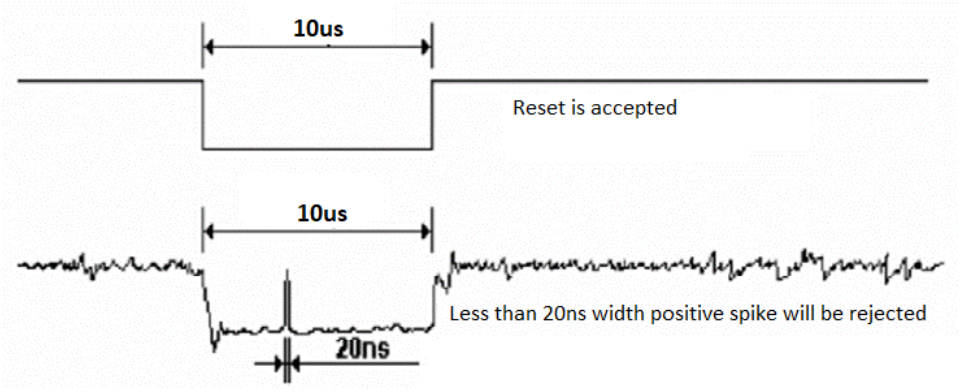
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.