Data Sheet | February 2, 2005 | FN8156.0

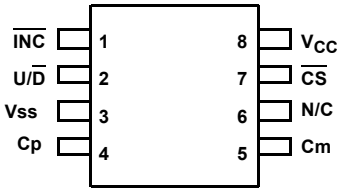
NV Electronically Programmable Capacitor

The Intersil X90100 is a non-volatile electronically programmable capacitor. The device is programmed through a simple digital interface. After programming, the chosen setting for the device is retained by internal EEPROM storage whether or not DC power is maintained. There are 32 programmable capacitance values selectable, ranging from 7.5pF to 14.5pF in 0.23pF increments, in single-ended mode. The dielectric is highly stable, and the capacitance exhibits a very low voltage coefficient. It has virtually no dielectric absorbtion and has a very low temperature drift coefficient in differential mode (<50ppm/°C).

The X90100 is programmed through three digital interface pins, which have Schmitt triggers and pullup resistors to secure code retention. The three pins, $\overline{INC}$, U/$\overline{D}$, and $\overline{CS}$, are identical in operation to other Intersil chips with up/down interface, such as the X9315 5-bit Digitally Controlled Potentiometer (DCP).

Pinout

X90100
(8 LD MSOP)
TOP VIEW



Features

- Non-volatile EEPROM storage of programmed trim codes
- Power On Recall of capacitance setting
- High-Performance Electronically Trimmable Capacitance
- Excellent linearity: <0.5 LSB error
- Very Simple Digital Interface
- Fast adjustments: 5µs max incremental change
- Eliminates the need for mechanical tuning
- Capacitance trimmable from 7.5pF to 14.5pF (single-ended mode)
- Packages:
  - MSOP (1.1mm x 3.0mm x 3.0mm)

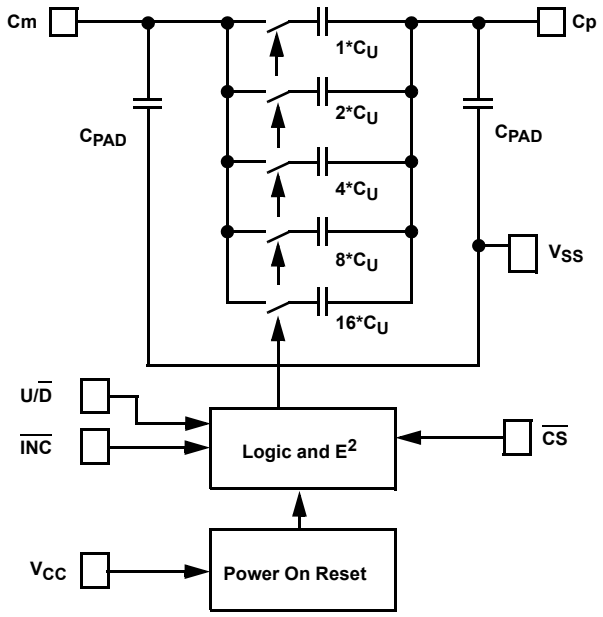
Applications

- Post-trim of low-cost regenerative receivers
- Tunable RF stages
- Low-cost, Low temperature drift oscillators
- Garage door openers
- Keyless entry
- Industrial wireless control
- Capacitive sensor trimming
- RFID tags

Ordering Information

ORDERING NUMBER	C_{TOTAL}	PACKAGE	TEMP RANGE (°C)
X90100M8I	7.5pF to 14.5pF, Single Ended	8 Ld MSOP	-40 to +85
X90100M8IT1	7.5pF to 14.5pF, Single Ended	8 Ld MSOP Tape and Reel	-40 to +85

Block Diagram



Pin Descriptions

MSOP	SYMBOL	BRIEF DESCRIPTION
1	$\overline{INC}$	**Increment ($\overline{INC}$)**. The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the capacitance value and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.
2	U/$\overline{D}$	**Up/Down (U/$\overline{D}$)**. The U/$\overline{D}$ input controls the direction of the trimmed capacitor value and whether the counter is incremented or decremented.
3	V_{SS}	**Ground**.
4	Cp	**Cp**. The high (Cp) and low (Cm) terminals of the X90100 are equivalent to the fixed terminals of a mechanical trimmable capacitor. The minimum dc voltage is V_{SS} and the maximum is V_{CC}. The value of capacitance across the terminals is determined by digital inputs $\overline{INC}$, U/$\overline{D}$, and $\overline{CS}$.
5	Cm	**Cm**. The high (Cp) and low (Cm) terminals of the X90100 are equivalent to the fixed terminals of a mechanical trimmable capacitor. The minimum dc voltage is V_{SS} and the maximum is V_{CC}. The value of capacitance across the terminals is determined by digital inputs $\overline{INC}$, U/$\overline{D}$, and $\overline{CS}$.
6	N/C	**Not Connected**. Must be floating.
7	$\overline{CS}$	**Chip Select ($\overline{CS}$)**. The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X90100 will be placed in the low power standby mode until the device is selected once again.
8	V_{CC}	**Positive Supply Voltage**.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, C_P, and
C_M with respect to V_{SS} . . . . . -1V to +7V

$\Delta V = |V_{CP}-V_{CM}|$ 5V
Lead temperature (soldering 10 seconds) . . . . . 300°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitor Specifications

V_{CC} = +5V, T_A = 25°C, single ended mode, C_M = 0V, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	TYP (4)	MAX	UNIT
	Absolute accuracy			±15		%
V_{Cp}	C_p terminal voltage		0		V_{CC}	V
V_{Cm}	C_m terminal voltage		0		V_{CC}	V
ΔC	Capacitance increments			0.23		pF
ΔC	Capacitance range			7		pF
C_{TOTAL}	Capacitance at Code=0			7.5		pF
C_{TOTAL}	Capacitance at Code=31			14.5		pF
Q	Quality factor(5)	f = 315MHz		7		
	Resolution			5		bits
INL	Absolute linearity error(1)			±0.15		lsb
DNL	Relative linearity error(2)			±0.15		lsb
TC_1	C_{TOTAL} Temperature Coefficient(5)	Differential Mode		±50		ppm/°C
V_{CC}	Supply Voltage		2.7		5.5	V

Notes: (1) Absolute linearity is used to determine actual capacitance versus expected capacitance = $C_{(n)}$(actual) - $C_{(n)}$ (expected) = ±0.15 Ml.
(2) Relative linearity is a measure of the error in step size between settings = $C_{(n+1)}$-[$C_{(n)}$ + Ml] = ±0.15 Ml.
(3) lsb = least significant bit = C_{TOT}/31.
(4) Typical values are for T_A = 25°C and nominal supply voltage.
(5) This parameter is not 100% tested.

DC Electrical Specifications

V_{CC} = 5V, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (4)	MAX	UNIT
I_{CC1}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V @ max. t_{CYC}		50	100	µA
I_{CC2}	V_{CC} active current (Store) (EEPROM Store)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max. t_{WR}		250	500	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V		0.5	2	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS}		-15		µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		-0.5		V_{CC} x 0.1	V
C_{IN}(5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz			10	pF

Endurance and Data Retention V_{CC} = 5V, T_A = 25°C unless otherwise specified

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

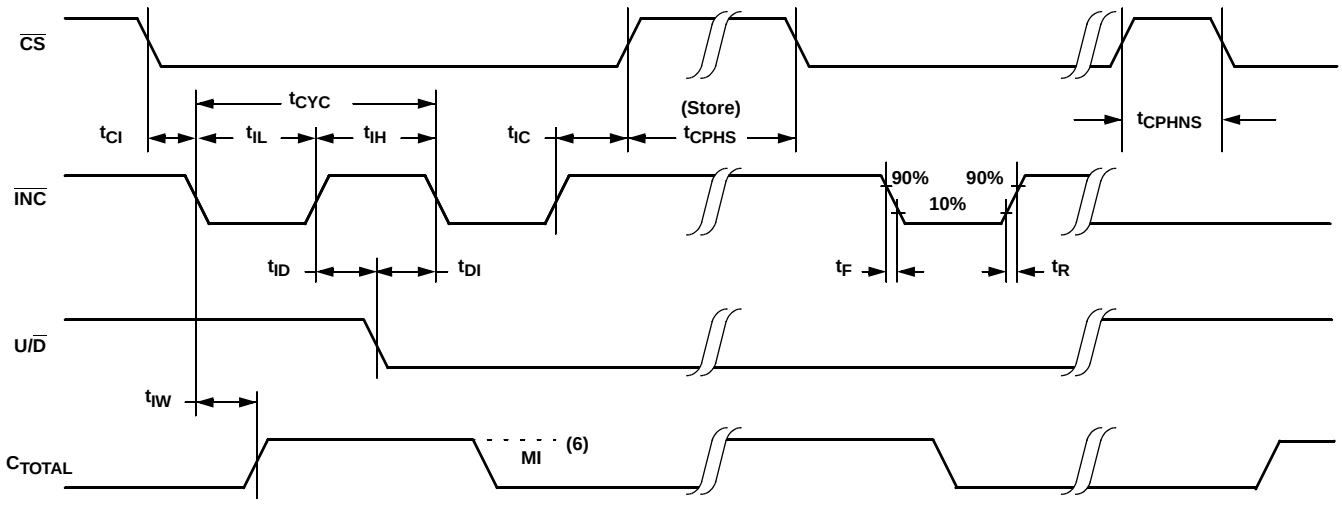
AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

AC Electrical Specifications V_{CC} = 5V, T_A = 25°C unless otherwise specified.

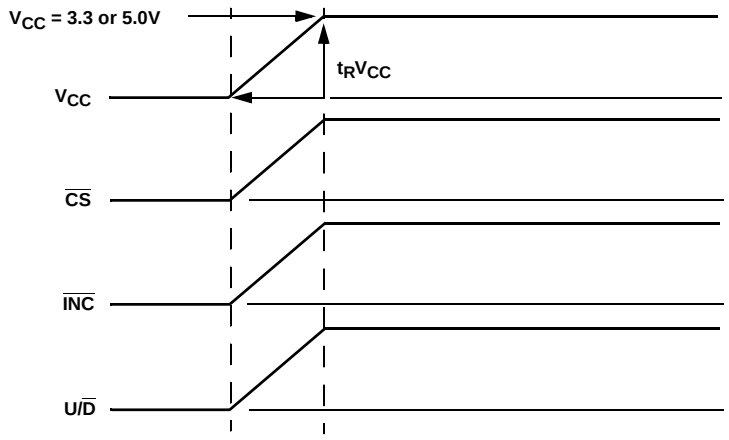
SYMBOL	PARAMETER	MIN	TYP (4)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	100			ns
t_{IL}(7)	$\overline{INC}$ LOW period	1			µs
t_{IH}(7)	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ inactive	1			µs
t_{CPHNS}(5)	$\overline{CS}$ Deselect time (NO STORE)	1			µs
t_{CPHS}(5)	$\overline{CS}$ Deselect time (STORE)	10			ms
t_{IW}	$\overline{INC}$ to C_{TOTAL} change		1	5	µs
t_{CYC}	$\overline{INC}$ cycle time	4			µs
t_R, t_F(5)	$\overline{INC}$ input rise and fall time			500	µs
t_{PU}(5)	Power up to capacitance stable			5	µs
t_R V_{CC}(5)	V_{CC} power-up rate	0.2		50	V/ms
t_{WR}(5)	Store cycle		5	10	ms

AC Timing



Notes: (6) MI in the A.C. timing diagram refers to the minimum incremental change in the C_{TOTAL} output due to a change in the counter value.
(7) $t_{IH} + t_{IL} \geq 4\mu s$

Power Up Timing (Digital Inputs Floating, Internal Pullup Action Shown)



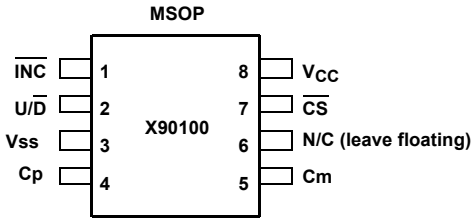
Power Up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the Cp, Cm pins provided that V_{CC} is always more positive than or equal to V_{Cp}, V_{Cm}, i.e., $V_{CC} \geq V_{Cp}$, V_{Cm}. The V_{CC} ramp rate spec is always in effect.

Powerup Requirements

In order to prevent unwanted tap position changes or an inadvertant store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin. The logic inputs have internal active pullups to provide reliable powerup operation. See powerup timing diagram.

Pin Configuration



Detailed Pin Descriptions

Cp and Cm

The high (Cp) and low (Cm) terminals of the X90100 are equivalent to the fixed terminals of a mechanical trimmable capacitor. The minimum dc voltage is V_{SS} and the maximum is V_{CC}. The value of capacitance across the terminals is determined by digital inputs $\overline{INC}$, U/$\overline{D}$, and $\overline{CS}$.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the trimmed capacitor value and whether the counter is incremented or decremented. This pin has an active current source pullup.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the capacitance value and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input. This pin has an active current source pullup.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X90100 will be placed in the low power standby mode until the device is selected once again. This pin has active circuit source pullup.

N/C - This pin should be left floating.

Pin Names

SYMBOL	DEFAULT	DESCRIPTION
Cp	output	Positive capacitor terminal
Cm	output	Negative capacitor terminal
V_{SS}	supply	Ground
V_{CC}	supply	Positive supply voltage
U/$\overline{D}$	pull up	Up/Down control input
$\overline{INC}$	pull up	Increment control input
$\overline{CS}$	pull up	Chip Select control input

Principles of Operation

There are three sections of the X90100: the input control, counter and decode section; the nonvolatile memory; and the capacitor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on electronic switches connecting internal units to the sum capacitor. Under the proper conditions the contents of the counter can be stored in nonvolatile memory

and retained for future use. The capacitor array is comprised of 31 individual capacitors connected in parallel. At one end of each element is an electronic switch that connects it to the sum.

The capacitor, when at either end of the range, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the counter changes positions. If the counter is moved several positions, multiple units are connected to the total for t_{IW} (INC to C_{TOTAL} change). The C_{TOTAL} value for the device can temporarily be increased by a significant amount if the counter is moved several positions.

When the device is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the capacitor is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the capacitor total value. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty two capacitor combinations for the capacitor array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X90100, move the capacitor value and deselect the device without having to store the latest count total in nonvolatile memory. After the count movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new C_{TOTAL} value will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments can be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the counter up and down until the proper trim is attained.

Mode Selection

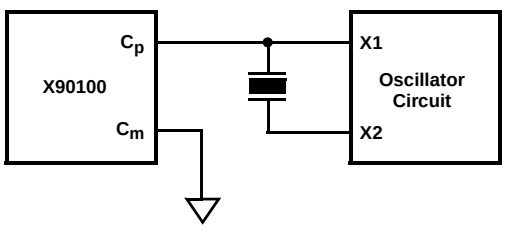
$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Cap Value Up
L	↘	L	Cap Value Down
↗	H	X	Store Cap Position
H	X	X	Standby Current
↗	L	X	No Store, Return To Standby
↘	L	H	Cap Value Up (not recommended)
↘	L	L	Cap Value Down (not recommended)

Table of Values

Single-Ended Mode

$$C_{OUT} = \frac{Code}{31} \bullet 7.0 + 7.5\ (pF)$$

$$0 \le Code \le 31$$

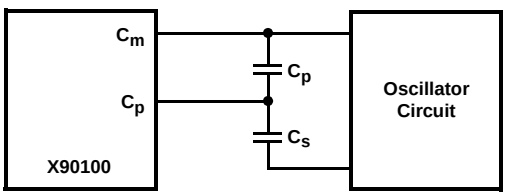


Example of a single-ended circuit

Differential Mode

$$C_{OUT} = Code \bullet 0.35 + 1.00\ (pF)$$

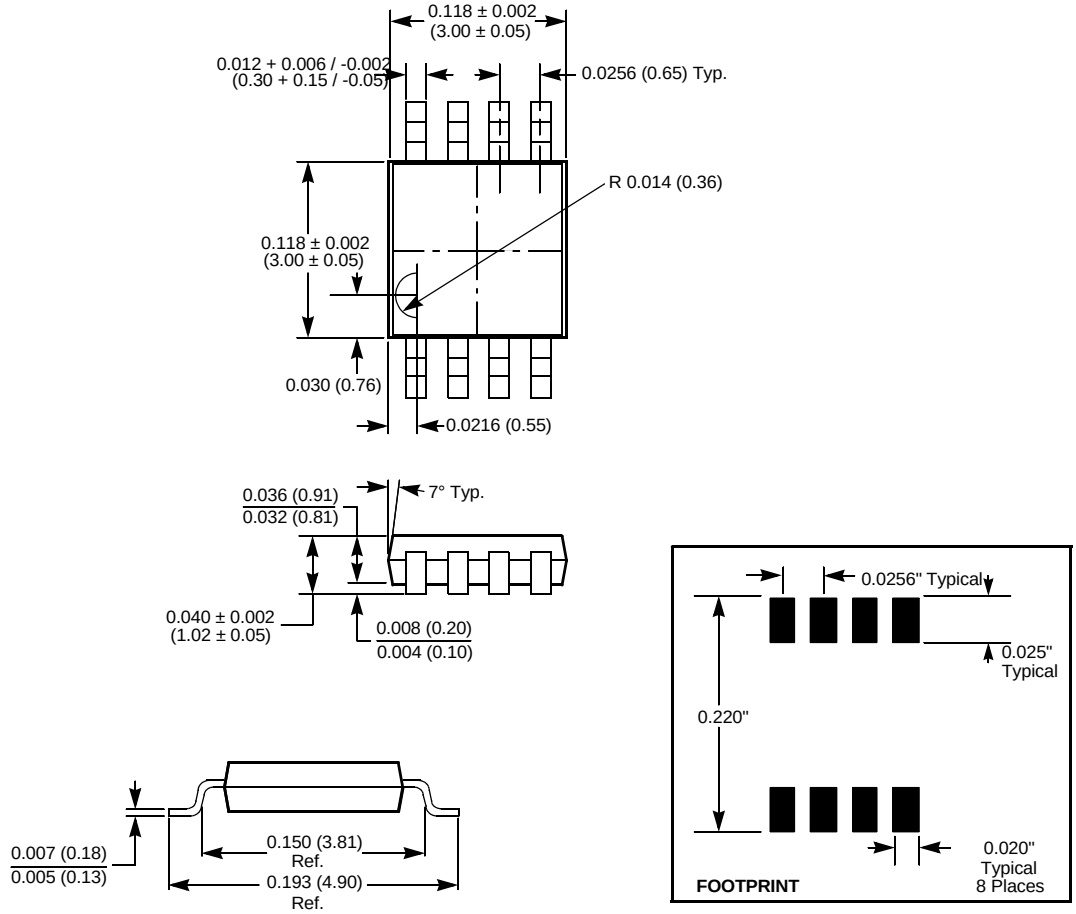
$$0 \le Code \le 31$$



Example of a differential mode circuit

Packaging Information

8-Lead Miniature Small Outline Gull Wing Package Type M



NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)