Product/Process Change Notice - PCN 18_0199 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD9542 Data Sheet Specification Changes

Publication Date: 13-Dec-2018

Effectivity Date: 13-Dec-2018 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release

Description Of Change:

Revision of the AD9542 Product Data Sheet from Rev0 to RevA.

The following summarizes the data sheet specification changes...

1) System Clock Inputs, XOA and XOB table:
1a) The Slew Rate for Sinusoidal Input expands to two line items below:
1b) Functional, >6 V/us TYP.
1c) Operational, >31 V/us TYP (formerly 50 V/us MIN).

2) Reference Inputs table:
2a) Differential Mode Slew Rate limit change; from 20 V/us MIN to >4.1 V/us TYP.
2b) Addition of DC-Coupled, LVDS-Compatible Mode Slew Rate line item; >1.2 V/us TYP.
2c) Addition of Single-Ended Mode Slew Rate, 1.2V CMOS line item; >8 V/us TYP.
2d) Addition of Single-Ended Mode Slew Rate, 1.8V CMOS line item; >8 V/us TYP.
2e) Addition of Single-Ended Mode Slew Rate, AC-Coupled line item; >8 V/us TYP.

3) Distribution Clock Outputs table:
3a) Differential Mode; addition of Rise/Fall Time line items.
3b) Differential Mode; addition of Duty Cycle line items.
3c) Single-Ended Mode; addition of Rise/Fall Time line items.
3d) Single-Ended Mode; addition of Duty Cycle line items.

4) Time Duration of Digital Functions table:
4a) Addition of "Time from Release of Power Down to Completion of System Clock PLL Calibration" line item.
4b) Addition of "Time from Release of Power Down to System Clock PLL Locked and Calibrated" line item.

5) Digital PLL (DPLL0, DPLL1) Specifications table:
5a) Digital Phase Detector (DPD) Input Frequency Range limit change; from 1 Hz MIN to 2 kHz MIN.

6) Holdover Specifications table:
6a) Relative Frequency Accuracy, Cascaded DPLL Operation limit change; from 0 ppb TYP to 0 ppb MAX.
6b) Addition of Relative Frequency Accuracy, Non-Cascaded DPLL Operation line item; <1 ppb TYP.

7) Logic Output Specifications (M0 to M6) table:
7a) Addition of Rise/Fall Time line items.

8) Temperature Sensor Specifications table:
8a) Accuracy, Absolute line item changes to Accuracy, Absolute Die Temperature
8b) Accuracy, Relative line item changes to Accuracy, Relative Die Temperature.

9) Addition of new tables:
9a) Operating Temperature
9b) Reference-to-Reference Coupling
9c) Reference-to-Mx Pin Input Timing Skew
9d) Output-to-Output Timing Skew
9f) DPLL Propagation Delay
9g) DPLL Propagation Delay Variation
9h) Mx-to-Mx Pin Output Timing Skew

10) Absolute Maximum Ratings
10a) Addition of Output Drivers line item.
10b) Removal of Operating Temperature Range line item (moved to the new Operating Temperature table in the Specifications section).

11) Removal of Configuration 3 line items from the Jitter Generation (Random Jitter) table.

12) Removal of Configuration 3 line items from the Phase Noise table.

13) Removal of two TPCs each containing "fREF = 1 Hz" as part of the figure label.

14) Addition of new Typical Performance Characteristics plots:
14a) Mx Pin Waveforms for Various Load Conditions
14b) DPLL Delay Compensation Versus Temperature, Differential AC-Coupled Input Reference Mode
14c) DPLL Delay Compensation Versus Temperature, 1.8V CMOS Input Reference Mode
14d) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 50 ppb
14e) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 4.6 ppm
14f) Reference Monitor Reference Valid Probability Versus Reference Input Frequency Offset, Tolerance = 100 ppm

Reason For Change:

1) The data sheet is in the process of revision to more thoroughly and accurately specify device performance/functionality.

2) Several Specification Tables and Typical Performance Characteristics (TPC) indicate device performance with 1Hz input reference frequency, which the AD9542 does not support. These specifications were accidentally included in the original data sheet and will not appear in the revised data sheet.

Impact of the change (positive or negative) on fit, form, function & reliability:

The changes described above have no impact on fit, form or reliability of the device.

Product Identification *(this section will describe how to identify the changed material)*

N/A, no physical change to device.

Summary of Supporting Information:

No physical change to die; no qualification is required.

Comments

No physical change to the device; no change to production test program; strictly a documentation change.

Supporting Documents None

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (2)				
AD9542 / AD9542BCPZ	AD9542 / AD9542BCPZ-REEL7			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	13-Dec-2018	13-Dec-2018	Initial Release