



CL1018

pHEMT Active Bias Gain Block
10MHz to 10 GHz, Low Noise Amplifier

Criteria Labs CL1018 is a high-performance E-pHEMT MMIC, low noise wideband amplifier that operates from 10 MHz to 10 GHz. The CL1018 is designed in a hermetic package for use in space, military and other high-reliability industrial applications. The CL1018 provides a typical gain of 18.5 dB, a 1.1 dB typical noise figure, and a typical output IP3 of 31.4 dBm, and requiring only 65 mA from a 5 V supply voltage. The saturated output power (Psat) of 22.4 dBm enables this low noise amplifier (LNA) to function as a local oscillator (LO) driver for balance I/Q or image rejection mixers. This amplifier has input/outputs that are internally matched to 50 ohms.



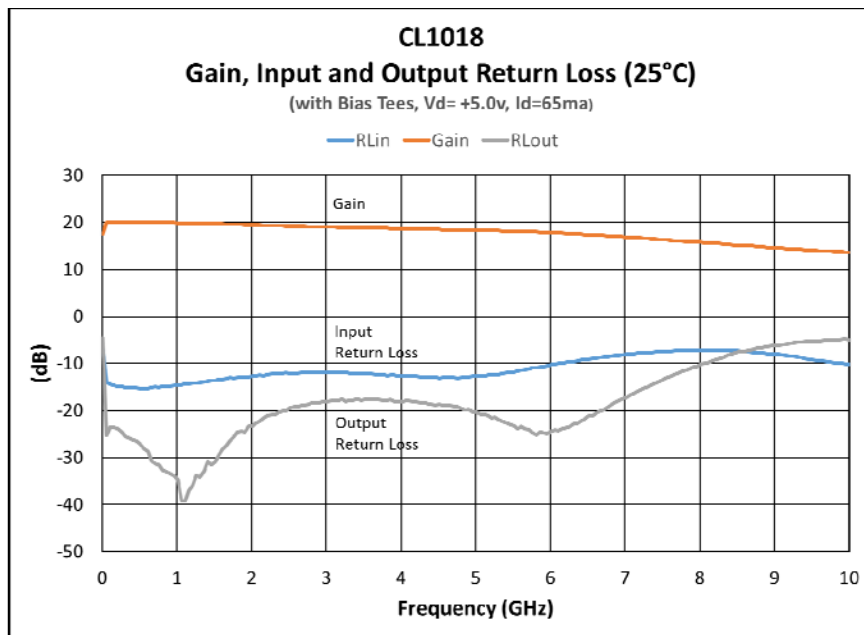
Package: Hermetic, 2-pin, 5.8mm x 2.8mm

Product Features

- Hermetic Package for High Reliability Applications
- High gain: 18.5 dB @ 4 GHz
- Low noise: 1.42 dB @ 4 GHz
- OIP3: 31.4 dBm @ 4 GHz
- P1db: 20.4 dBm @ 4 GHz
- Psat: 22.4 dBm @ 4 GHz

Applications:

- Military and Space Communications
- LO Driver and Balanced , I/Q or image rejection mixers



Criteria Labs 706 Brentwood St., Austin, TX 78752
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Absolute Maximum Ratings		
Parameter	Rating	Units
Device Current (Id)	100	mA
Device Voltage	7	V
RF Input Power	19	dBm
Channel Temperature (Tch)	+175	°C
Operating Temperature Range	-55 to +85	°C
Storage Temperature Range	-65 to +150	°C
Moisture Sensitivity Level	Hermetic	
ESD Rating - Human body Model (HBM)	Class 1B	500V+



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

0.01 GHz to 3 GHz Frequency Range					
Nominal Operating Parameters					
	CL1018 Specifications			Units	Conditions
	Min	typ	Max		
General Performance					Test conditions: Vd = 5.0Vdc, Id = 65mA, OIP3 tone spacing 1 MHz, Pout per tone = 5 dBm Ta=25C, 50 ohm system. Bias Tee tested.
Frequency Range	0.01		3	GHz	
Small Signal Gain	17.4	19.5		dB	
Gain Variation Over Temperature		0.01		dB/°C	
Output					
P1dB	19	21		dBm	
Psat		22.5			
OIP3		33		dBm	
Input Return Loss		15		dB	
Output Return Loss		24		dB	
Reverse Isolation		23		dB	
Noise Figure		1.15	1.65	dB	0.3GHz to 3 GHz
Operating Voltage		5		V	
Operating Current		65	80	mA	Adjust Vgg to achieve Id=65 ma
Thermal Resistance		76		°C/W	Channel to Case



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3 GHz to 8 GHz Frequency Range					
Nominal Operating Parameters					
	CL1018 Specifications			Units	Conditions
	Min	typ	Max		
General Performance					Test conditions: Vd = 5.0Vdc, Id = 65mA, OIP3 tone spacing 1 MHz, Pout per tone = 5 dBm Ta=25C, 50 ohm system. Bias Tee tested.
Frequency Range	3		8	GHz	
Small Signal Gain	15	18		dB	
Gain Variation Over Temperature		0.01		dB/°C	
Output					
P1dB	17.4	20.4		dBm	
P _{sat}		22.4			
OIP3		31.4		dBm	
Input Return Loss		12		dB	
Output Return Loss		12		dB	
Reverse Isolation		24		dB	
Noise Figure		1.42	1.92	dB	0.3GHz to 3 GHz
Operating Voltage		5		V	
Operating Current		65	80	mA	Adjust V _{gg} to achieve Id=65 mA
Thermal Resistance		76		°C/W	Channel to Case

8 GHz to 10 GHz Frequency Range					
Nominal Operating Parameters					
	CL1018 Specifications			Units	Conditions
	Min	typ	Max		
General Performance					Test conditions: Vd = 5.0Vdc, Id = 65mA, OIP3 tone spacing 1 MHz, Pout per tone = 5 dBm Ta=25C, 50 ohm system. Bias Tee tested.
Frequency Range	8		10	GHz	
Small Signal Gain	12.9	15.9		dB	
Gain Variation Over Temperature		0.01		dB/°C	
Output					
P1dB	17.4	19.4		dBm	
P _{sat}		21.4			
OIP3		31.9		dBm	
Input Return Loss		6		dB	
Output Return Loss		10		dB	
Reverse Isolation		30		dB	
Noise Figure		1.72	2.23	dB	0.3GHz to 3 GHz
Operating Voltage		5		V	
Operating Current		65	80	mA	Adjust V _{gg} to achieve Id=65 mA
Thermal Resistance		76		°C/W	Channel to Case

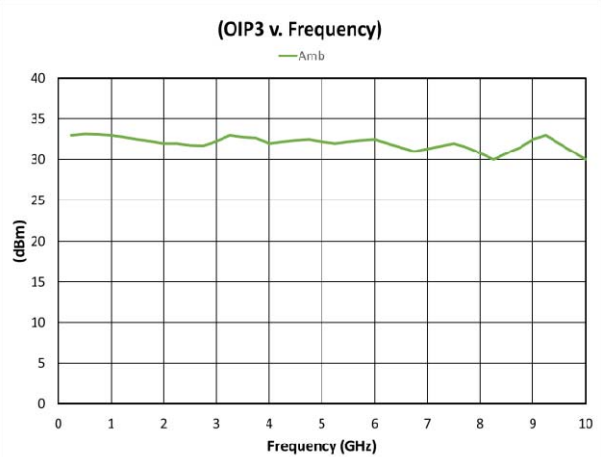
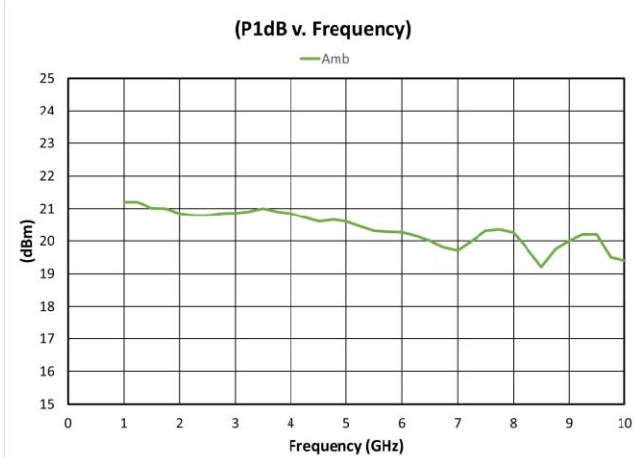
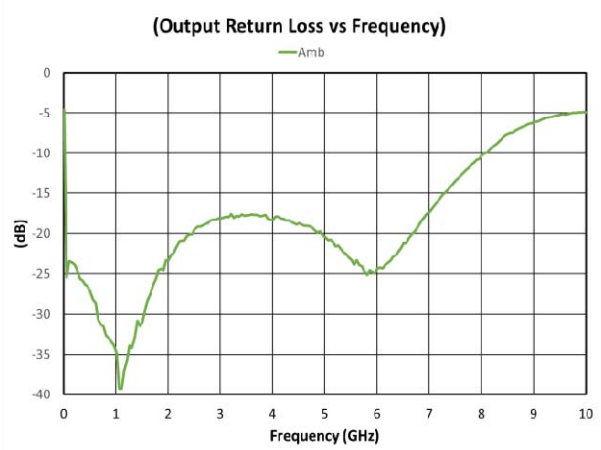
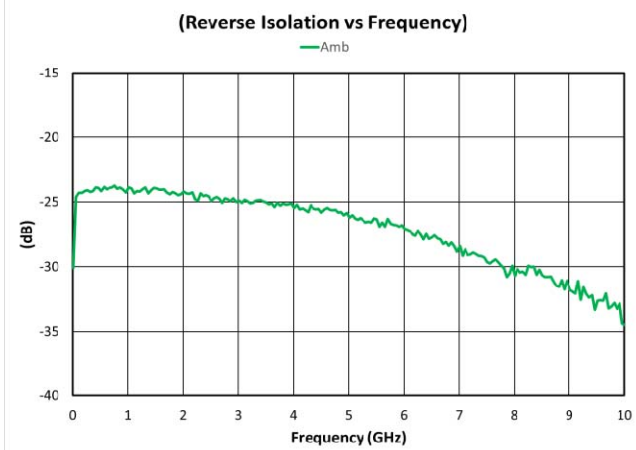
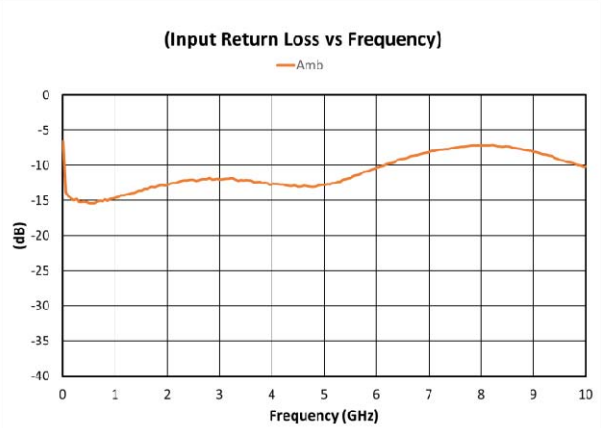
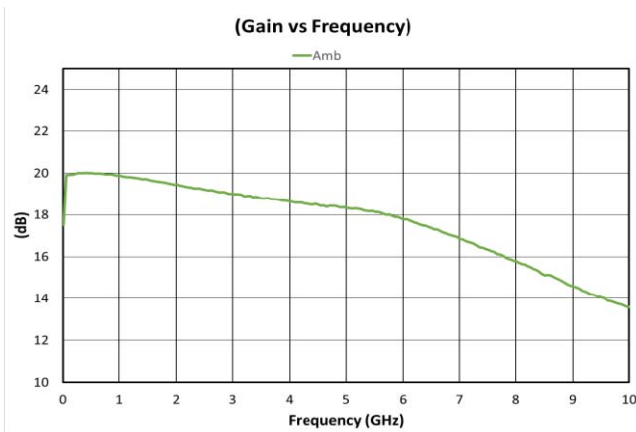


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Typical Performance (Vd= +5.0 V)

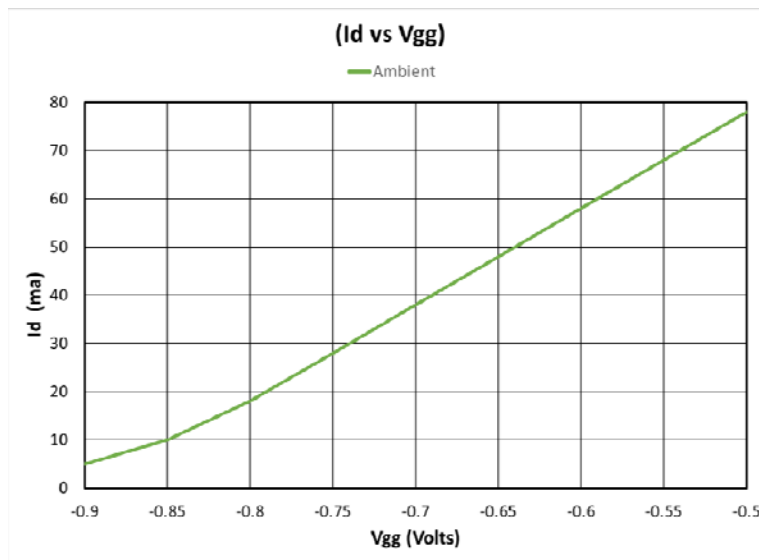
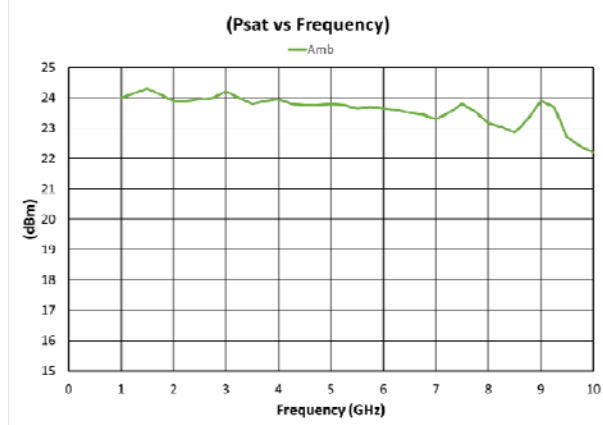
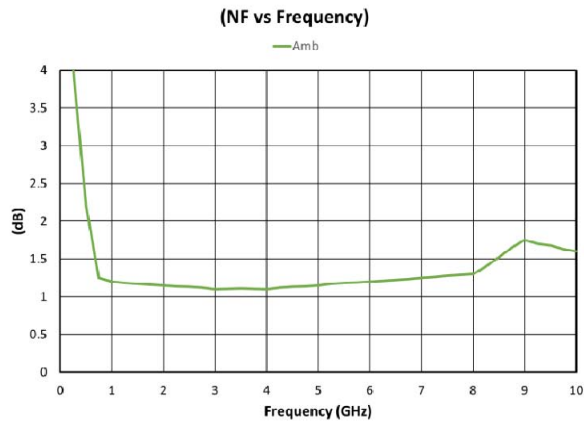


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Typical Performance (Vd= +5.0 V)



Application Information

The CL1018 has single ended input and outputs where the impedances are nominally equal to 50 ohms over the 10 MHz to 10 GHz frequency range. The CL1018 can be used directly into a 50 ohm system with no required impedance matching circuitry.

The input and output impedances are stable over a wide temperature and supply voltage range without matching compensation.

See typical application schematic for operation of the CL1018. Wideband bias tees on the input and outputs provide ac coupling and the necessary supply voltages to the RFIN/Vgg and RFOUT/Vd pins. A 5.0 V dc drain bias is supplied to the amplifier through the inductor connected to the RFOUT/Vd pin, and the -2V gate bias voltage is supplied to the RFIN/Vgg pin through the inductor. When using this circuit in wide bandwidth applications, self resonances with RF inductor can introduce design trade offs.

Recommended Bias Sequencing

The recommended bias sequence during power up is as follows:

1. Set RFIN/Vgg to -2.0 V
2. Set RFOUT/Vd to 5.0 V
3. Increase RFIN/Vgg to achieve a typical supply current $I_d=65\text{mA}$.
4. Apply the RF signal

The recommended bias sequence during power down is as follows:

1. Turn off the RF signal
2. Decrease RFIN/Vgg to -2.0 V. $I_d=0.0\text{ mA}$
3. Decrease RFOUT/Vd to 0.0 V.
4. Set RFIN/Vgg = 0.0 V.

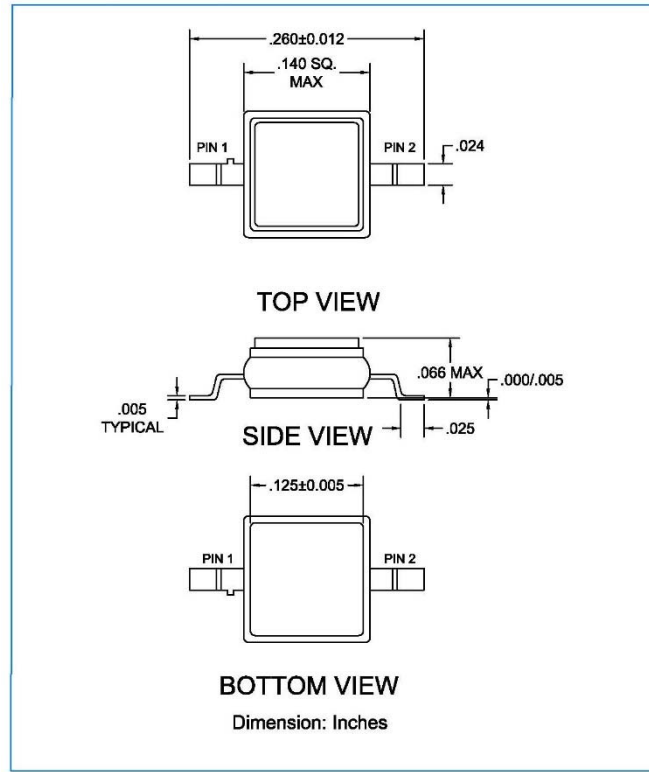
Wide Range Of Operating Conditions

The CL1018 can be used with a wide range of operating conditions. Biasing the CL1018 with $V_d= 5.0\text{ V}$ and $I_d=65\text{ mA}$ provides optimal performance. The supply voltage V_d can be adjusted from 3.0V to 7.0V and adjusting RFIN/Vgg bias conditions I_d can be adjusted from 5mA to 75mA.

Consult with Criteria Labs for additional operating performance under different bias conditions.



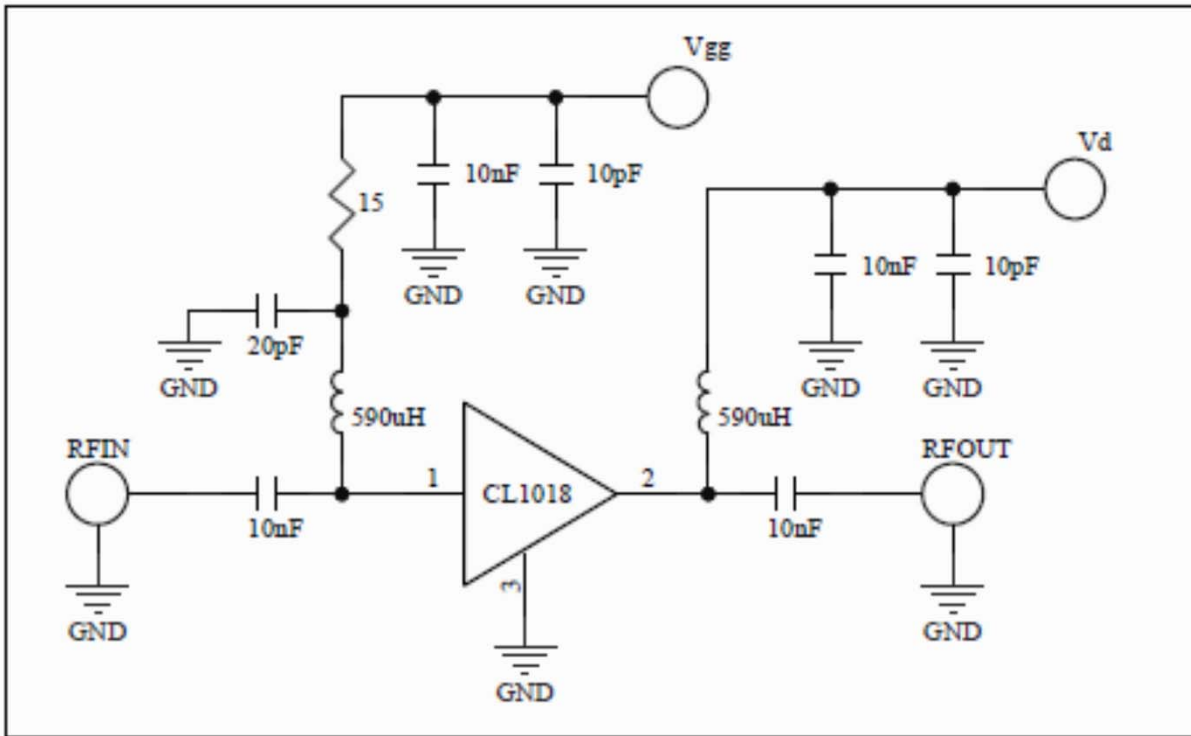
Package Drawing



Pin Names and Descriptions		
Pin	Name	Description
1	RFIN/Vgg	RF Input (RFIN/Vgg). This pin is dc-coupled and matched to 50 ohms. See the typical application schematic for Gate Bias interface to the Amplifier (Vgg). This pin requires the use of an external blocking capacitor and inductor chosen for the frequency of operation.
2	RFOUT/DC Bias	RF Output (RFOUT). This pin is dc-coupled and matched to 50 ohms. See the typical application schematic for the Drain Bias interface to the Amplifier (Vd). This pin requires the use of an external blocking capacitor and inductor chosen for the frequency of operation.
Package Paddle	GND	Ground. The package bottom must be connected to RF/dc ground.

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Typical Application Schematic



Order Information:

CL1018-X-Y-Z

- | | | |
|--|---|---|
| <p>Screening Level</p> <ul style="list-style-type: none"> - Blank Mil-STD-883 screen flow - 3 temperature electrical - S Space Flow | <p>Lead Finish</p> <ul style="list-style-type: none"> - Blank (Au finish) - D (63/37 solder dip leads only) | <p>Packaging</p> <ul style="list-style-type: none"> - Blank (Foam ESD shipping box) - T (tape and reel) |
|--|---|---|



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