TPD4S1394 Firewire ESD Clamp With Live-Insertion Detection Circuit

1 Features

- IEEE 1394 Live Insertion Detection
- ESD Protection Exceeds IEC61000-4-2 (Level 4)
  - ±15-kV Human-Body Model (HBM)
  - ±6-kV IEC 61000-4-2 Contact Discharge
- 4-Channel Matching ESD Clamps for High-Speed Differential Lines
- Flow-Through, Single-in-Line Pin Mapping Simplifies Board Layout
- Available in an 8-Pin X2SON (DQL) package

2 Applications

Firewire Interface

3 Description

The TPD4S1394 provides robust system level ESD solution for the IEEE 1394 port, along with a live insertion detection mechanism for high-speed lines interfacing a low-voltage, ESD sensitive core chipset. This device protects and monitors up to two differential input pairs. The optimized line capacitance protects the data lines with data rates in excess of 1.6 GHz without degrading signal integrity.

The TPD4S1394 incorporates a live insertion detection circuit whose output state changes when improper voltage levels are present on the input data lines. The FWPWR_EN signal controls an external FireWire port power switch. During the live insertion event if there is a floating GND or a high level signal at the D+ or D– pins, the internal comparator detects the changes and pull the FWPWR_EN signal to a low state. When FWPWR_EN is driven low, there is an internal delay mechanism preventing it from being driven to the high state regardless of the inputs to the comparator.

Additionally, the TPD4S1394 performs ESD protection on the four inputs pins: D1+, D1–, D2+, and D2–. The TPD4S1394 conforms to the IEC61000-4-2 (Level 4) ESD protection and ±15-kV HBM ESD protection. The TPD4S1394 is characterized for operation over ambient air temperature of –40°C to 85°C.

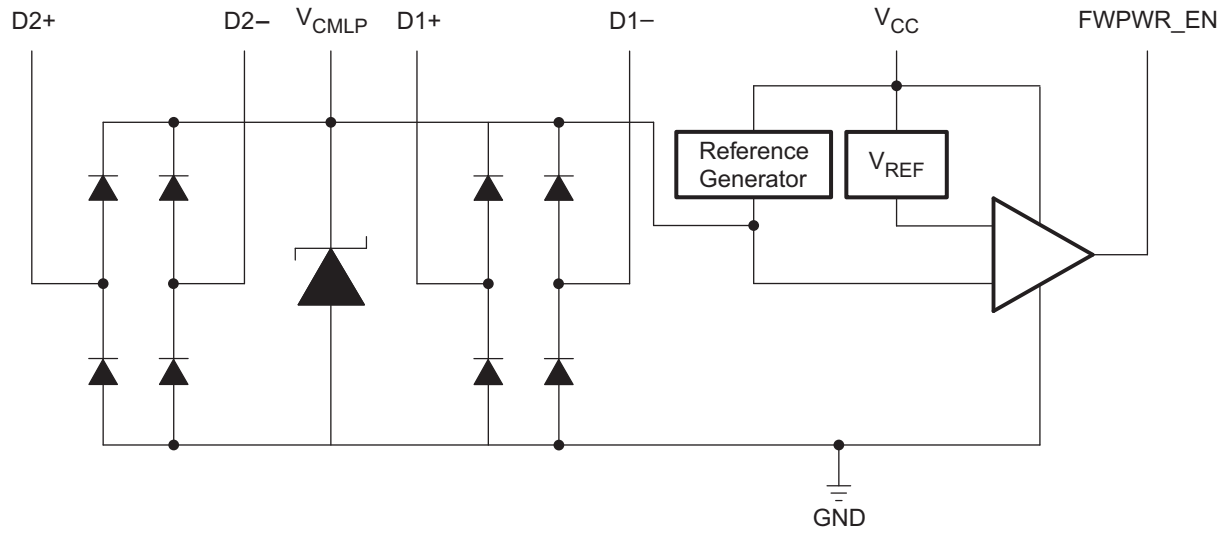
A 0.1-µF decoupling capacitor is required at VCC.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4S1394	X2SON (8)	2.00 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B **Page**

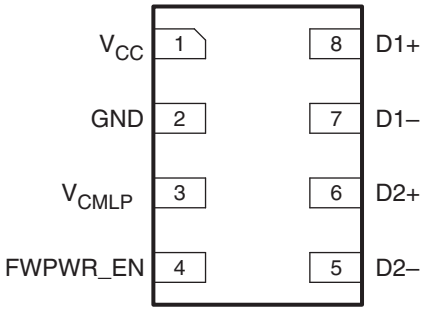
- Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Switching Characteristics* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 4

Changes from Original (November 2009) to Revision A **Page**

- Removed hard coded ordering information table. Information contained in Package Orderable Addendum. ... 1

5 Pin Configuration and Functions

DQL Package
8-Pin X2SON
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D1+	8	Input	High-speed ESD clamp input
D1–	7	Input	High-speed ESD clamp input
D2+	6	Input	High-speed ESD clamp input
D2–	5	Input	High-speed ESD clamp input
FWPWR_EN	4	Output	Control output
GND	2	Ground	Ground
VCC	1	Power	Power supply
VCLMP	3	Output	Comparator trip reference

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	4.6	V
V_{IO}	IO voltage at D+, D–, V_{CLMP}	0	4	V
FWPWR_EN	Switch output	–0.5	4.6	V
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 5, 6, 7, and 8	±2500	V
			Pins 5, 6, 7, and 8	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins except 5, 6, 7, and 8	±1000	
			Pins 5, 6, 7, and 8	±1000	
		IEC 61000-4-2 contact discharge	Pins 5, 6, 7, and 8 (interface side)	±6000	
		IEC 61000-4-2 air-gap discharge	Pins 5, 6, 7, and 8 (interface side)	±6000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V

6.4 Thermal Information

THERMAL METRIC(1)		TPD4S1394 DQL (X2SON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	167.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DX}	FWPWR_EN trip voltage (D+ and D– pins)	High-to-low		2.9	3.4	4	V
		Low-to-high		2.7	3.2	3.8	
V_{CLMP}	Value on pin		No connection		2.45		V
V_{BR}	Breakdown voltage at V_{CLAMP}		I_I = 1 mA		4.2		V
V_D	Diode forward voltage for lower clamp		I_D = 8 mA lower clamp diode	–0.6	–0.8	–0.95	V
FWPWR_EN	Switch output				V_{CC}		V
R_{DYN}	Dynamic resistance (in and out clamp) of D+, D–		I = 1 A		1		Ω
C_{IO}	I/O capacitance of D+, D–		V_{IO} = 2.5 V		1.5	2	pF
I_{CC}	Current consumption		V_{CC} = 3.3 V, FWPWR_EN = high		130	200	µA

(1) A 0.1-µF decoupling capacitor is required at VCC.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TRIP}	Delay time for FWPWR_EN to go low	Loading on FWPWR_EN = 50 pF	0.5	2	5	µs
t_{RESET}	Delay time for FWPWR_EN to go high after trip	FWPWR_EN = V_{CC}	300	450	600	ms

6.7 Typical Characteristics

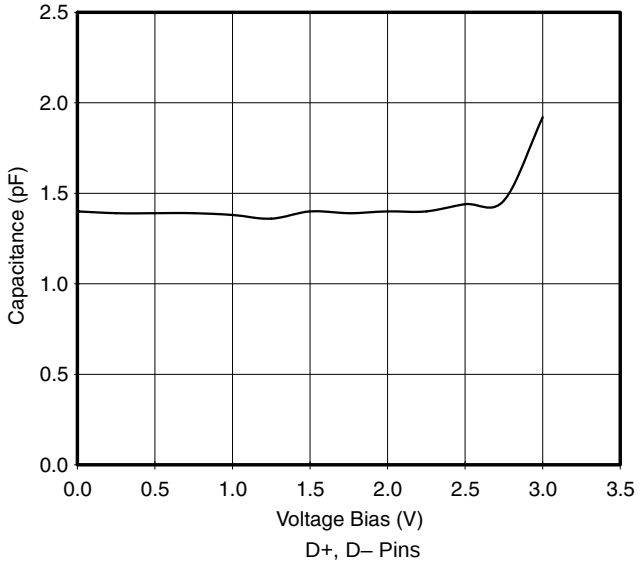


Figure 1. I/O Capacitance vs I/O Voltage

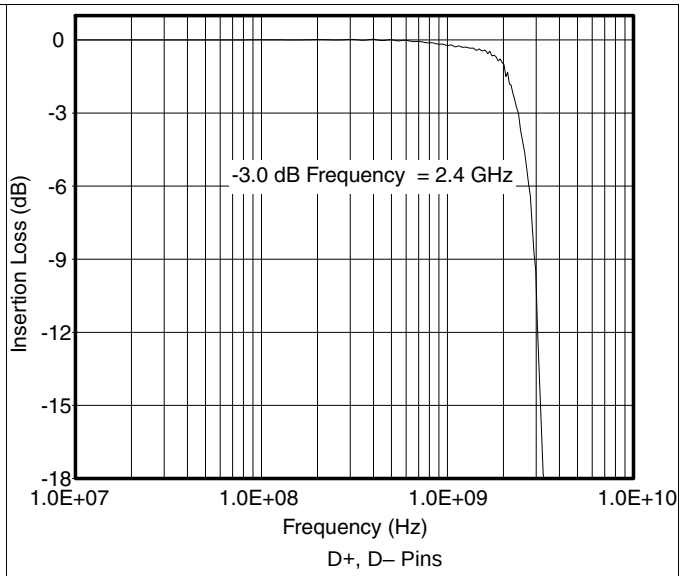


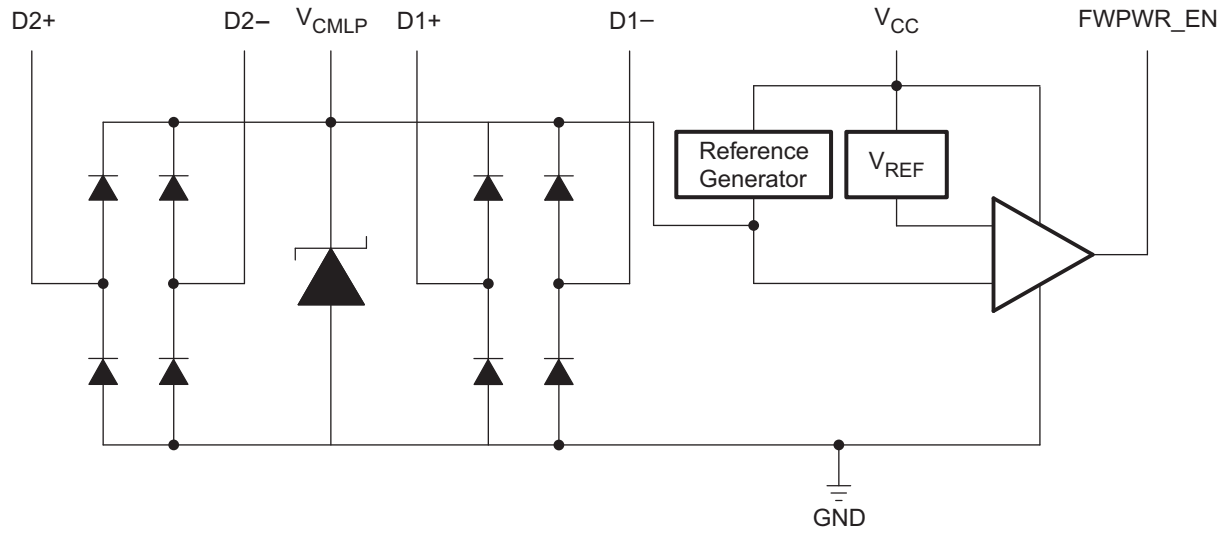
Figure 2. Insertion Loss (S21)

7 Detailed Description

7.1 Overview

TPD4S1394 is a FireWire interface part that complies to the IEEE 1394 standard. The device has ESD protection for four high-speed data lines that pass 6-kV IEC61000-4-2 standard. Each dataline's I/O capacitance associated with the ESD cell is minimal and supports high data rate. There is a live insertion detection circuit integrated in TPD4S1394. During the live insertion event if there is a floating GND or a high-level signal at D+ or D–, the FWPWR_EN is driven low, disabling the external FireWire power switch.

7.2 Functional Block Diagram



7.3 Feature Description

TPD4S1394's high-speed ESD cells on the data lines protect the pins from up to ±6-kV IEC 61000-4-2 contact discharge. The live insertion protection circuit detects improper voltages on the data lines and turn off the FireWire port power switch during an abnormal condition.

7.4 Device Functional Modes

The TPD4S1394's D1+, D1–, D2+, and D2– pins are a passive-integrated circuit that activates when voltages exceed the forward voltage plus V_{CLMP} or fall below the lower diodes forward voltage (–0.6 V). V_{CC} must be within recommended voltage range for live insertion detection circuit to work correctly.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD4S1394 has both high-speed ESD cells to protect the D1+, D1–, D2+, and D2– lines and live insertion detection circuit to identify improper status during insertion and to control the external power switch.

8.2 Typical Application

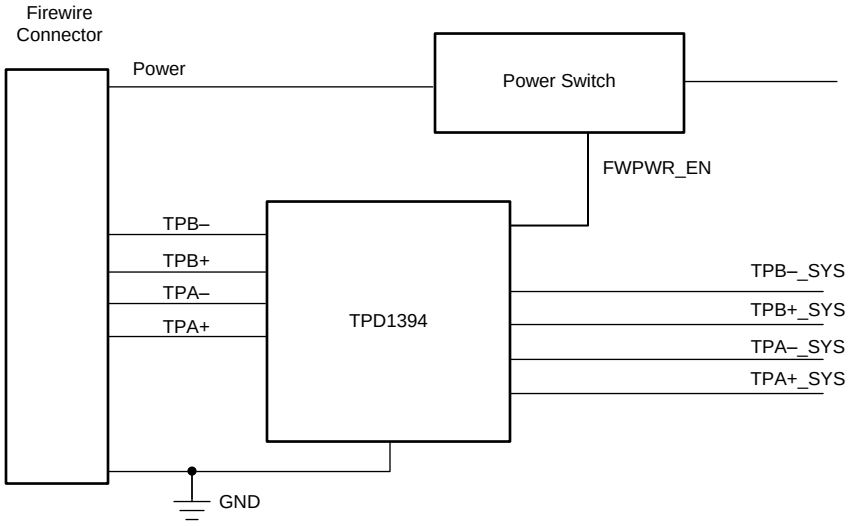


Figure 3. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a TPD4S1394 is used to protect the FireWire connector and detect live insertion.

Table 1 shows the design parameters:

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Power supply, V_{CC}	3.3 V
Data line operating frequency	400 MHz (800 Mbps)

8.2.2 Detailed Design Procedure

The data transfer rate of 800 Mbps is well below the bandwidth of the data pins of TPD4S1394. So the parasitics associated with the ESD cells on these lines do not degrade the signal integrity. 3.3-V power supplies are commonly available from the board and can be used to power the live insertion detection circuit.

8.2.3 Application Curves

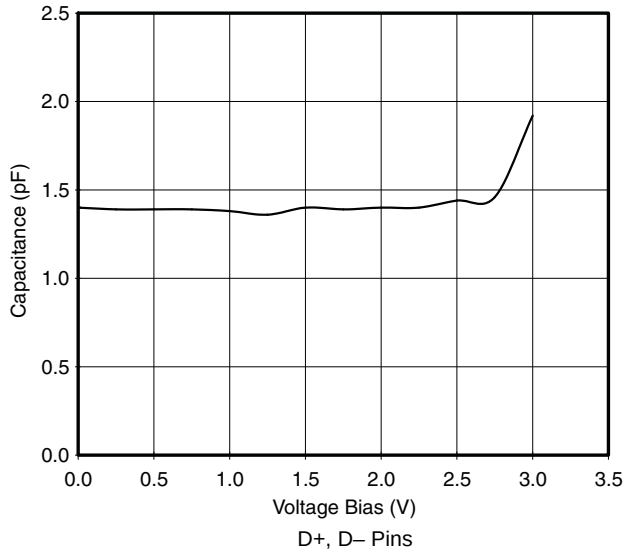


Figure 4. I/O Capacitance vs I/O Voltage

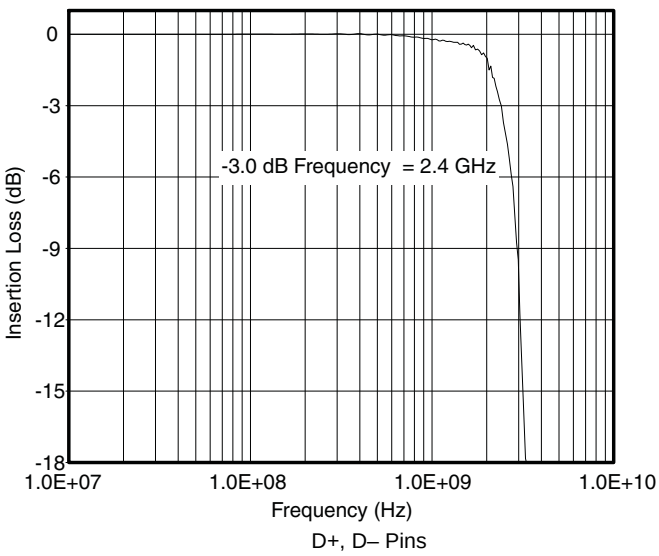


Figure 5. Insertion Loss (S21)

9 Power Supply Recommendations

TI recommends a power supply for V_{CC} is from 3 V to 3.6 V.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

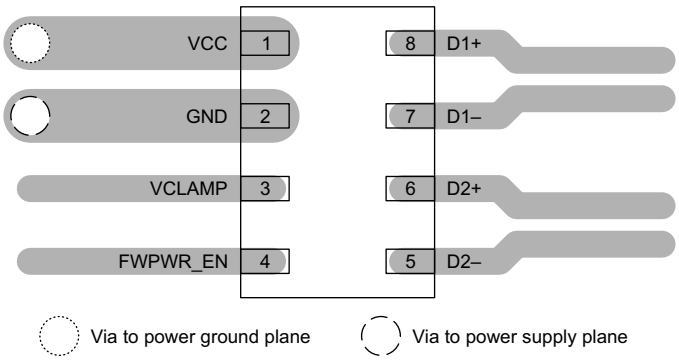


Figure 6. TPD4S1394 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4S1394DQLR	ACTIVE	X2SON	DQL	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(5J7, 5JR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

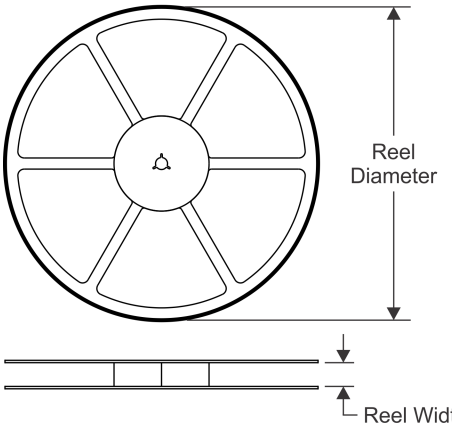
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

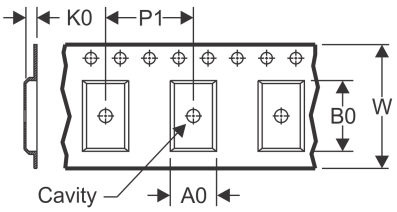
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

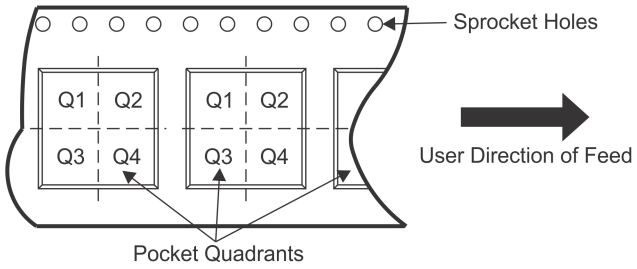


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

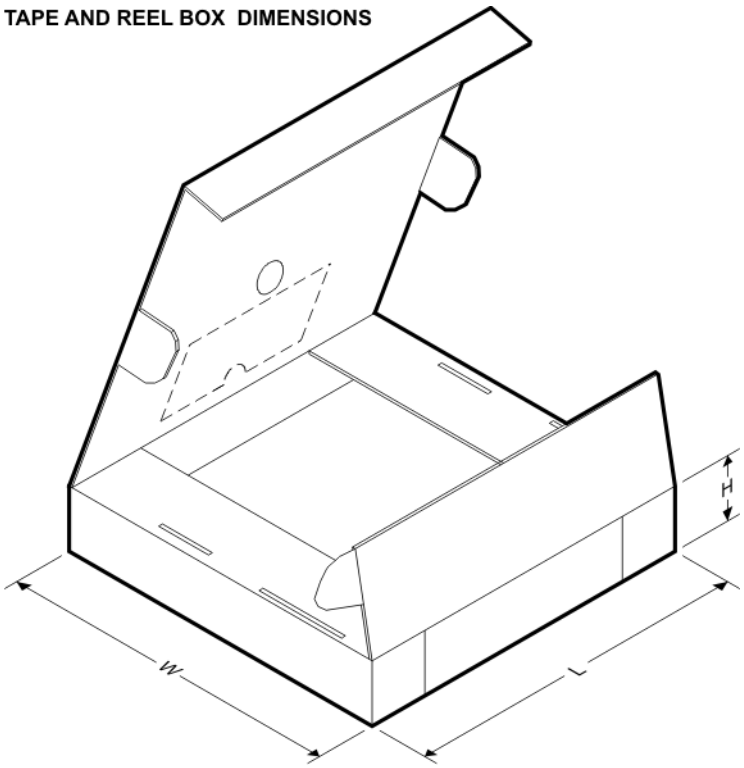
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S1394DQLR	X2SON	DQL	8	3000	180.0	9.5	1.6	2.3	0.5	4.0	8.0	Q1

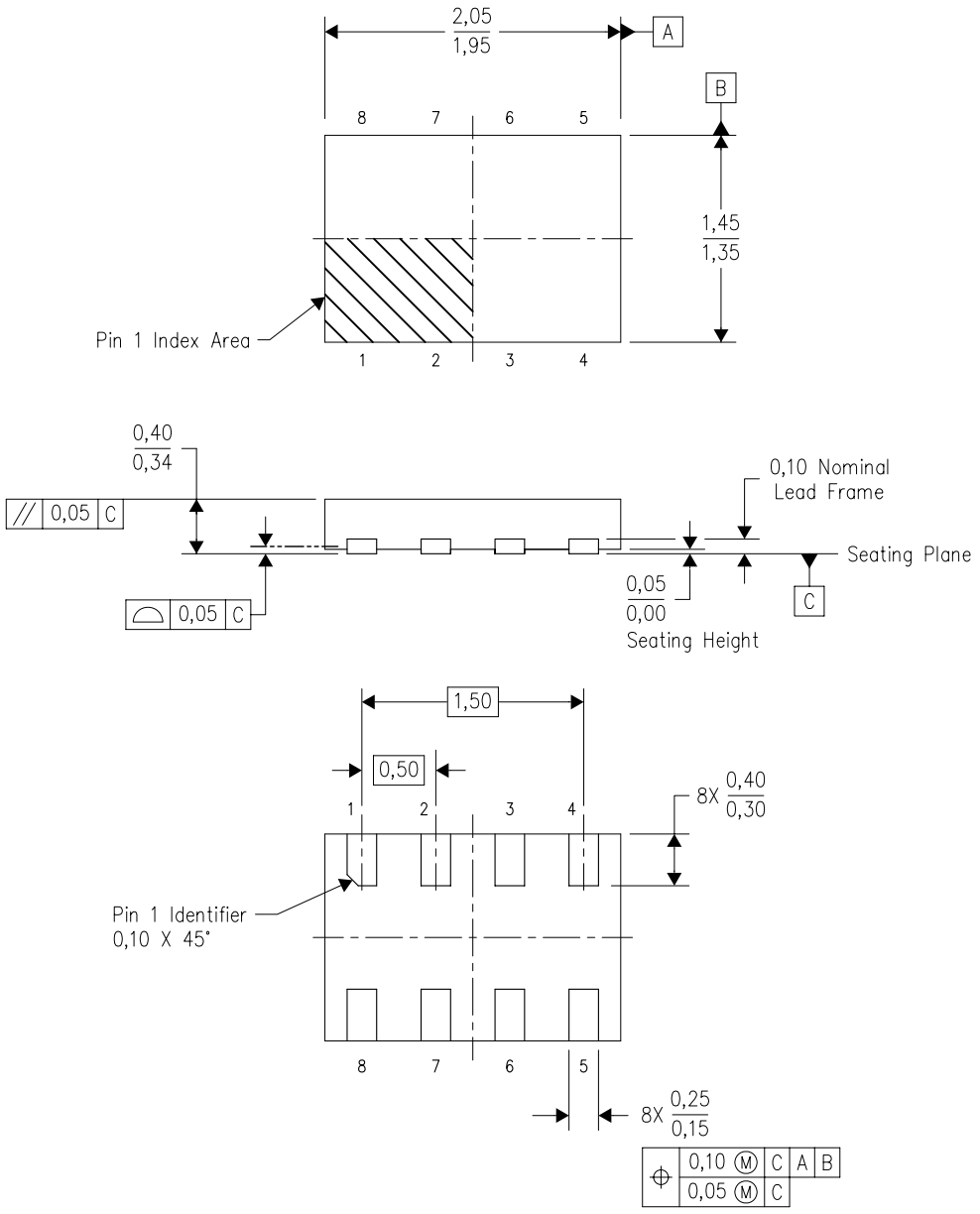
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S1394DQLR	X2SON	DQL	8	3000	184.0	184.0	19.0

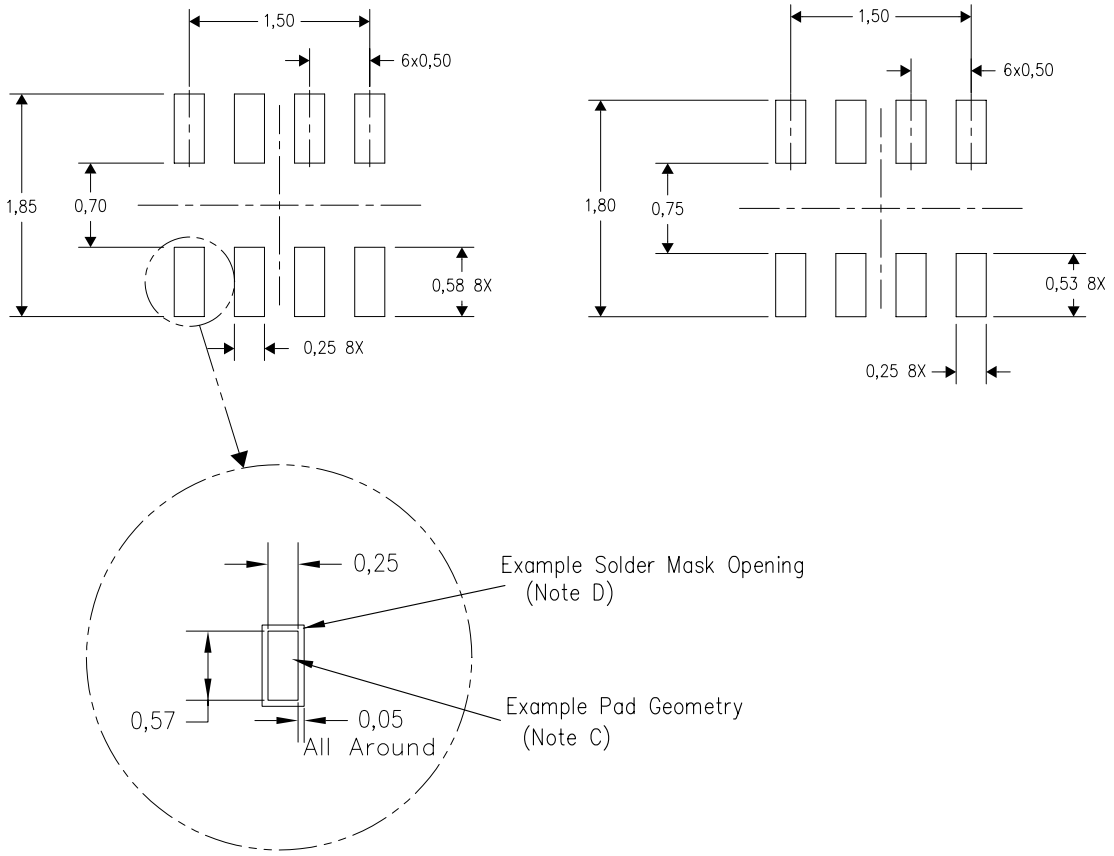
DQL (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4210271/A 06/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQL (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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