

## **Product Change Notification**

(Notification - P1608041-DIGI) (CST-R2-AJ094) August 19, 2016

To: Our Valued Digi-Key, Inc. Customer

Overview:

The purpose of this notification is to communicate product change of select Renesas Electronics America, Inc. (REA) devices. These devices have suggested replacements.

Select SRAM products in TSOP packages are undergoing a Speed and Temperature grade unification. Grades "-5SR", "-7SI", "-7SR" are being unified to single grade "-5SI".

There are no changes to reliability and quality levels. The replacement device is has superior electrical specifications, and also have the following changes (see Appendix for detailed changes)...

- Assembly and Final Test Site change from Renesas Semiconductor Beijing to Amkor Technology Malaysia (Assembly) & Powertech Technology Inc. (Final Test).
- Lead Frame Material change from 42-Alloy to Cu.
- Moisture Sensitivity Level change from MSL2 to MSL3.
- Lead Plating Material change from Sn-Cu to Sn.
- 5. Change to Halogen Free molding compound.
- Standardization of JEDEC trays and embossed tape.

Affected Products: A review of our records to your company indicate the attached list of products is affected by this notification.

Booking Part Number	Suggested Replacement Part Number
R1LP0408DSB-7SI#B0	R1LP0408DSB-5SI#B1
R1LP0408DSB-7SR#B0	R1LP0408DSB-5SI#B1
R1LP5256ESA-7SI#B0	R1LP5256ESA-5SI#B1
R1LP5256ESA-7SR#B0	R1LP5256ESA-5SI#B1
R1LV0108ESA-7SR#B0	R1LV0108ESA-5SI#B1
R1LV0108ESF-5SR#B0	R1LV0108ESF-5SI#B1
R1LV0216BSB-7SI#B0	R1LV0216BSB-5SI#B1
R1LV5256ESA-7SR#B0	R1LV5256ESA-5SI#B1

Part numbers given in this list are for active part numbers in REA database at the time of this notification.

### **Key Dates:**

Samples of replacement device available.	Nov. 1 <sup>st</sup> , 2016
Final last time buy <b>(LTB)</b> orders of original part number placed to REA or to a franchised REA distributor.	Jun. 15 <sup>th</sup> , 2017
Planned date for last time shipment (LTS) of original part number from REA.	Dec 15 <sup>th</sup> , 2017

### Response:

Please place last time buy (LTB) orders in a timely manner prior to the key dates listed to avoid product availability issues. If you anticipate volumes beyond your regular rate, please contact your REA sales representative with a forecast of your requirements. Shipments between the LTB and LTS dates are Non-Cancelable and Non-Returnable (NCNR).

You are encouraged to sample the suggested replacement device and begin qualification as soon as possible. Please contact you REA sales representative to obtain samples.

Please contact your REA sales representative for any questions or comments.

Thank you for your attention.

Sincerely,

Renesas Electronics America, Inc.



# Appendix A: Change Details

(1) 28pin-TSOP(I) 256Kb(5V) Part name: R1LP5256ESA

Item		Pre Change	Post Change
0.1		R1LP5256ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP5256ESA-5SI#B1 (Tray packing)
Orderable part name		R1LP5256ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP5256ESA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of	f origin display	CHINA	MALAYSIA
JEITA Pack	kage Code	P-TSOP(1)28-8x11.8-0.55	P-TSOP(1)28-8x11.8-0.55
Package m specificatio	on	R1LP5256ESA CHINA -5SI XXXXXXXXX  R1LP5256ESA CHINA -5SR XXXXXXXXX  R1LP5256ESA CHINA -7SI XXXXXXXXX  R1LP5256ESA CHINA -7SI XXXXXXXXX  CHINA -7SR  CHINA -7SR	R1LP5256ESA  MALAYSIA -5SI  Electrical characteristics  XXXXXXXXX  Date code  Country of origin (Back-End Line: Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test I	ine	Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
Tray	Storage number	234pcs/tray	234pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's comer is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(2) 28pin-TSOP(I) 256Kb(3V) Part name: R1LV5256ESA

Item		Pre Change	Post Change
Orderable part name		R1LV5256ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LV5256ESA-5SI#B1 (Tray packing)
		R1LV5256ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV5256ESA-5SI#S1 (Tape & Reel packing)
Assembly I		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
	forigin display	CHINA	MALAYSIA
JEITA Pack	rage Code	P-TSOP(1)28-8x11.8-0.55	P-TSOP(1)28-8x11.8-0.55
Package m specificatio		R1LV5256ESA CHINA -5SI XXXXXXXXX  R1LV5256ESA CHINA -5SR XXXXXXXXX  R1LV5256ESA CHINA -7SI XXXXXXXXX  R1LV5256ESA CHINA -7SI XXXXXXXXX  CHINA -7SR	R1LV5256ESA  MALAYSIA -5SI  Electrical characteristics  XXXXXXXXX  Date code  Country of origin (Back-End Line: Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test li	ne	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
Tray	Storage number	234pcs/tray	234pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape &	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
packing	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(3) 32pin-TSOP(I) 1Mb(5V) Part name: R1LP0108ESF

Item		Pre Change	Post Change
Orderable part name		R1LP0108ESF-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP0108ESF-5SI#B1 (Tray packing)
		R1LP0108ESF-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESF-5SI#S1 (Tape & Reel packing)
Assembly		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
_	f origin display	CHINA	MALAYSIA
JEITA Pac	kage Code	P-TSOP(1)32-8x18.4-0.50	P-TSOP(1)32-8x18.4-0.50
Package n specificatio	on	R1LP0108ESF -5S1 CHINA XXXXXXXXX  R1LP0108ESF -5SR CHINA XXXXXXXXX  R1LP0108ESF -7S1 CHINA XXXXXXXXX  R1LP0108ESF Date code  Country of origin (Back-End Line: Assembly)	R1LP0108ESF Part name Electrical characteristics XXXXXXXXX Date code  Country of origin (Back-End Line: Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test I	Packing	Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Talwan)
	specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 18.4mm)
Tray	Storage number	156pcs/tray	156pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.) Inner box size	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	(LxWxH) Packing	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	specification Embossed	Current specification	New specification
	tape	Current specification	New specification
	Storage number Inner box size	1,000pcs/reel	1,000pcs/reel
	(LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



Appendix A (cont.): Change Details
(4) 32pin-TSOP(I) 1Mb(3V) Part name: R1LV0108ESF

Item		Pre Change	Post Change
Orderable	part name	R1LV0108ESF-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LV0108ESF-5SI#B1 (Tray packing)
		R1LV0108ESF-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESF-5SI#S1 (Tape & Reel packing)
Assembly		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
	f origin display	CHINA	MALAYSIA
JEITA Paci	kage Code	P-TSOP(1)32-8x18.4-0.50	P-TSOP(1)32-8x18.4-0.50
Package m specification	on	R1LV0108ESF  -5S1 CHINA XXXXXXXXX  R1LV0108ESF  -5SR CHINA XXXXXXXXX  R1LV0108ESF  -7S1 CHINA XXXXXXXXX  R1LV0108ESF  Date code  Country of origin (Back-End Line: Assembly)	R1LV0108ESF Part name Electrical characteristics XXXXXXXX Date code  Country of origin (Back-End Line: Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test I		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 18.4mm)
Tray	Storage number	156pcs/tray	156pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-p performan		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(5) 32pin-sTSOP 1Mb(5V) Part name: R1LP0108ESA

Item		Pre Change	Post Change
Orderable p	part name	R1LP0108ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP0108ESA-5SI#B1 (Tray packing)
		R1LP0108ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESA-5SI#S1 (Tape & Reel packing)
Assembly I		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
	forigin display	CHINA	MALAYSIA
JEITA Pack	rage Code	P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package m specificatio	on T	R1LP0108ESA CHINA -5SI XXXXXXXXX  R1LP0108ESA CHINA -5SR XXXXXXXXX  R1LP0108ESA CHINA -7SI XXXXXXXXX  R1LP0108ESA CHINA -7SI XXXXXXXXX  CHINA -7SR Date code  Country of origin (Back-End Line: Assembly)	R1LP0108ESA  MALAYSIA -5SI  XXXXXXXXX  Date code  Country of origin (Back-End Line:Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test li		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
Tray	Storage number	234pcs/tray	234pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel	Embossed tape	Current specification	New specification
packing	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



Appendix A (cont.): Change Details
(6) 32pin-sTSOP 1Mb(3V) Part name: R1LV0108ESA

Item		Pre Change	Post Change
Orderable	part name	R1LV0108ESA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LV0108ESA-5SI#B1 (Tray packing)
		R1LV0108ESA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESA-5SI#S1 (Tape & Reel packing)
Assembly		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
_	f origin display	CHINA	MALAYSIA
JEITA Pack	kage Code	P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package m specificatio	on	R1LV0108ESA CHINA -5SI XXXXXXXXX  R1LV0108ESA CHINA -5SR XXXXXXXXX  R1LV0108ESA CHINA -7SI XXXXXXXXX  R1LV0108ESA CHINA -7SI XXXXXXXXX  CHINA -7SR CHINA -	R1LV0108ESA Part name MALAYSIA -5SI Electrical characteristics
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-Included)	Epoxy resin (Halogen-free)
Final test I		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
Tray	Storage number	234pcs/tray	234pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(7) 32pin-sTSOP 2Mb(3V) x8 Part name: R1LV0208BSA

Item		Pre Change	Post Change
Orderable part name		R1LV0208BSA-5SI/-7SI#B0 (Tray packing)	R1LV0208BSA-5SI#B1 (Tray packing)
		R1LV0208BSA-5SI/-7SI#S0 (Tape & Reel packing)	R1LV0208BSA-5SI#S1 (Tape & Reel packing)
Assembly	line	Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of	f origin display	CHINA	MALAYSIA
JEITA Pack	kage Code	P-TSOP(1)32-8x11.8-0.50	P-TSOP(1)32-8x11.8-0.50
Package m specification		R1LV0208BSA CHINA -5SI XXXXXXXXX  R1LV0208BSA CHINA -7SI CHINA -7SI XXXXXXXX  CHINA -7SI Date code  Country of origin (Back-End Line: Assembly)	R1LV0208BSA Part name MALAYSIA -5SI Electrical characteristics  XXXXXXXXX Date code  Country of origin (Back-End Line: Assembly)
	Lead frame material	42Alloy	Cu
Assembly	Lead plating	Sn-Cu	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-Included)	Epoxy resin (Halogen-free)
Final test I	ine	Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Talwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 8mm x 11.8mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 8mm x 11.8mm)
Tray	Storage number	234pcs/tray	234pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape &	Embossed tape	Current specification	New specification
packing	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-p performan		MSL 2	MSL 3
Shipping la	abel	Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(8) 32pin-TSOP(II) 4Mb(5V) Part name: R1LP0408DSB

Item		Pre Change	Post Change
Orderable part name		R1LP0408DSB-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)	R1LP0408DSB-5SI#B1 (Tray packing)
		R1LP0408DSB-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0408DSB-5SI#S1 (Tape & Reel packing)
Assembly I		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
	f origin display	CHINA	MALAYSIA
JEITA Pack	kage Code	P-TSOP(2)32-10.16x20.95-1.27	P-TSOP(2)32-10.16x20.95-1.27
Package m specificatio		R1LP0408DSB CHINA 5SI  XXXXXXXX  UUUUUUUUUUUUUUUUUU  R1LP0408DSB CHINA 5SR XXXXXXXX  UUUUUUUUUUUUUUUUUU  R1LP0408DSB CHINA 7SI XXXXXXXX  UUUUUUUUUUUUUUUUUU  R1LP0408DSB CHINA 7SI XXXXXXXX  UUUUUUUUUUUUUUUUUU  R1LP0408DSB CHINA 7SI AXXXXXXX  UUUUUUUUUUUUUUUUUUUU  Index mark Country of origin (Back-End Line:Assembly)	R1LP0408DSB Part name MALAYSIA 5SI Characteristics XXXXXXXX Date code UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU
	Lead frame material	Cu	Cu
Assembly	Lead plating	Sn (pure tin)	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-free)	Epoxy resin (Halogen-free)
Final test I	Packing	Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	specification	Current specification  JEDEC Tray with Renesas Logo	New specification  JEDEC Tray without Renesas Logo
	Tray	(TSOP II package size: 10.16mm x 20.95mm)	(TSOP II package size: 10.16mm x 20.95mm)
Tray backing	Storage number Laying direction	117pcs/tray  Direction from the top left position to the down side	117pcs/tray
	of Ics on a tray Number of	(when the position of chamfer in tray's corner is bottom left.) 8 trays + 1 tray (cover)	No change 10 trays + 1 tray (cover)
	trays (Max.) Inner box size	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape &	(LxWxH) Packing	Current specification	New specification
	specification Embossed tape	Current specification	New specification
Reel backing	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin)



Appendix A (cont.): Change Details
(9) 44pin-TSOP(II) 2Mb(3V) x16 Part name : R1LV0216BSB

Item		Pre Change	Post Change
Orderable part name		R1LV0216BSB-5SI/-7SI#B0 (Tray packing)	R1LV0216BSB-5SI#B1 (Tray packing)
Orderable part name		R1LV0216BSB-5SI/-7SI#S0 (Tape & Reel packing)	R1LV0216BSB-5SI#S1 (Tape & Reel packing)
Assembly I	line	Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of	forigin display	CHINA	MALAYSIA
JEITA Pack	rage Code	P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80
Package m specificatio		R1LV0216BSB  CHINA 5SI XXXXXXXX  COUNTY OF origin (Back-End Line: Assembly)	R1LV0216BSB Part name  MALAYSIA 5SI Electrical characteristics  XXXXXXXXX Date code  UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU
	Lead frame material	Cu Cu	Cu
Assembly	Lead plating	Sn (pure tin)	Sn (pure tin)
Material	Die bonding	Epoxy paste	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-free)	Epoxy resin (Halogen-free)
Final test I		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)
Tray	Storage number	135pcs/tray	135pcs/tray
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-p performan		MSL 3	MSL 3
Shipping la	abel	Current specification	No change in format (Changes in orderable part name, country of origin)



(10) 44pin-TSOP(II) 4Mb Fast 5V Part name: R1RP0416DSB

Item		Pre Change	Post Change
Orderable part name		R1RP0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR#D0 (Tray packing)	R1RP0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR#D1 (Tray packing)
		R1RP0416DSB-2LR/-2PR#S0 (Tape & Reel packing)	R1RP0416DSB-2LR/-2PR#S1 (Tape & Reel packing)
Assembly I		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
	f origin display	CHINA	MALAYSIA
JEITA Pack	kage Code	P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80
	-	R1RP0416DSB CHINA OPI XXXXXXXX UUUUUUUUUUUUUUUUUUUUUUUUUUUU	R1RP0416DSB MALAYSIA OPI XXXXXXX UUUUUUUUUUUUUUUUUUUUUUUUUUUUU
	Lead frame	42Alloy	Cu Cu
Assembly	material Lead plating	Sn-Cu	Sn (pure tin)
Assembly Material	Die bonding	Epoxy film	Epoxy paste
- ration rai	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-Included)	Epoxy resin (Halogen-free)
Final test I	ine	Renesas Semiconductor Belling (China)	Powertech Technology Inc. (Taiwan)
	Packing specification	Current specification	New specification
,	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)
Tray	Storage number	135pcs/tray	135pcs/tray
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's comer is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
	Packing specification	Current specification	New specification
Tape & Reel packing	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping la	abel	Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)



(11) 44pin-TSOP(II) 4Mb Fast 3V Part name: R1RW0416DSB

Item		Pre Change	Post Change		
Orderable part name  Assembly line Country of origin display JEITA Package Code		R1RW0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR/-2UR#D0 (Tray packing)	R1RW0416DSB-0PI/-0PR/-2LR/-2PI/-2PR/-2SR/-2UR#D1 (Tray packing)		
		R1RW0416DSB-0PI/-0PR/-2PI/-2PR#50 (Tape & Reel packing)	R1RW0416DSB-0PI/-0PR/-2PI/-2PR#S1 (Tape & Reel packing)		
		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)		
		CHINA	MALAYSIA		
		P-TSOP(2)44-10.16x18.41-0.80	P-TSOP(2)44-10.16x18.41-0.80		
	-	R1RW0416DSB CHINA OPI XXXXXXXX UUUUUUUUUUUUUUUUUUUUUUUUUUUU	R1RW0416DSB MALAYSIA OPI XXXXXXXX UUUUUUUUUUUUUUUUUUUUUUUUUUUU		
	Lead frame material	42Alloy	Cu		
Assembly		Sn-Cu	Sn (pure tin)		
Material	Die bonding	Epoxy film	Epoxy paste		
	Wire bonding	Au	Au		
Mold		Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)		
Final test I	ine	Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)	JEDEC Tray without Renesas Logo (TSOP II package size: 10.16mm x 18.41mm)		
Tray	Storage number	135pcs/tray	135pcs/tray		
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape & Reel	Embossed tape	Current specification	New specification		
packing	Storage number	1,000pcs/reel	1,000pcs/reel		
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm		
Moisture-p performan		MSL 2	MSL 3		
Shipping la	abel	Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)		



(12) 48pin-TSOP(I) 16Mb 3V Part name: R1LV1616HSA

Item		Pre Change	Post Change		
Orderable part name  R1LV1616HSA-4SI/-5SI#B0 (Tray pa R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Assembly line Country of origin display  JEITA Package Code  R1LV1616HSA-4SI/-5SI#B0 (Tray pa R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display) R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display) R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Country of origin display) R1LV1616HSA-4SI/-5SI#S0 (Tape & Ree Renesas Semiconductor Beijing (Ch Renesas Semiconduct		R1LV1616HSA-4SI/-5SI#B0 (Tray packing)	R1LV1616HSA-4SI/-5SI#B1 (Tray packing)		
		R1LV1616HSA-4SI/-5SI#S0 (Tape & Reel packing)	R1LV1616HSA-4SI/-5SI#S1 (Tape & Reel packing)		
			Amkor Technology Malaysia (Malaysia)		
			MALAYSIA		
			P-TSOP(1)48-12x18.4-0.50		
	on ge in display of characteristics)	R1LV1616HSA CHINA -4SI XXXXXXXX  R1LV1616HSA CHINA -5SI CHINA -5SI Characteristics Characteristics Characteristics Country of origin (Back-End Line: Assembly)	R1LV1616HSA MALAYSIA -4SI XXXXXXXX  R1LV1616HSA MALAYSIA -5SI XXXXXXXX  Country of origin (Back-End Line:Assembly)		
	Lead frame material	42Alloy	Cu		
Assembly	Lead plating	Sn-Cu	Sn (pure tin)		
Material	Die bonding	Epoxy film	Epoxy paste		
	Wire bonding	Au	Au		
	Mold	Epoxy resin (Halogen-Included)	Epoxy resin (Halogen-free)		
Final test I	line	Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Taiwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 12mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)		
Tray	Storage number	96pcs/tray	96pcs/tray		
packing	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's comer is bottom left.)		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape & Reel	Embossed tape	Current specification	New specification		
packing	Storage number	1,000pcs/reel	1,000pcs/reel		
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm		
Moisture-p performan		MSL 2	MSL 3		
Shipping la	abel	Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)		



Appendix A (cont.): Change Details
(13) 48pin-TSOP(I) 32Mb 3V Part name : R1LV3216RSA

Item		Pre Change	Post Change		
Orderable	e part name	R1LV3216RSA-5SI#B0 (Tray packing)	R1LV3216RSA-5SI#B1 (Tray packing)		
Or del able	e part name	R1LV3216RSA-5SI#S0 (Tape & Reel packing)	R1LV3216RSA-5SI#S1 (Tape & Reel packing)		
Assembly	line	Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)		
Country of	of origin display	CHINA	MALAYSIA		
Index mark		P-TSOP(1)48-12x18.4-0.50	P-TSOP(1)48-12x18.4-0.50		
Package r specificati		R1LV3216RSA Part name CHINA -5SI Characteristics Country of origin (Back-End Line: Assembly)	R1LV3216RSA  MALAYS I A -5S I  Country of origin (Back-End Line:Assembly)  Part name  Electrical characteristics Date code		
	Lead frame material	42Alloy	Cu		
Assembly Material	Lead plating	Sn-Cu	Sn (pure tin)		
	Die bonding	Epoxy film	Epoxy paste		
	Wire bonding	Au	Au		
	Mold	Epoxy resin (Halogen-Included)	Epoxy resin (Halogen-free)		
Final test line Packing		Renesas Semiconductor Beljing (China)	Powertech Technology Inc. (Talwan)		
	Packing specification	Current specification	New specification		
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 12mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)		
Tray	Storage number	96pcs/tray	96pcs/tray		
packing	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change		
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)		
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm		
	Packing specification	Current specification	New specification		
Tape &	Embossed tape	Current specification	New specification		
packing	Storage number	1,000pcs/reel	1,000pcs/reel		
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm		
Moisture- performa		MSL 2	MSL 3		
Shipping	label	Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)		



# Appendix B: Temperature Grade Unification

(1) 28pin-TSOP(I), 32pin-TSOP(I)

	Memory		Pre Change		Post Change			
Package Type	Cap., Supply Voltage	bit	Orderable Part Name	Access time	Operation temp.	Orderable Part Name	Access time	Operation temp.
28pin-	256Kb 5V	x8	R1LP5256ESA-5SI#B0	-40℃				
TSOP(I)			R1LP5256ESA-5SI#S0		~85℃			
			R1LP5256ESA-5SR#B0	55ns	-0℃			
			R1LP5256ESA-5SR#S0		~70℃	R1LP5256ESA-5SI#B1	55ns	-40℃
			R1LP5256ESA-7SI#B0		-40℃	R1LP5256ESA-5SI#S1	33(15	~85℃
			R1LP5256ESA-7SI#S0	70ns	~85℃			
			R1LP5256ESA-7SR#B0	70115	0℃			
			R1LP5256ESA-7SR#S0		~70℃			
	256Kb 3V	x8	R1LV5256ESA-5SI#B0		-40℃			
			R1LV5256ESA-5SI#S0	55ns	~85℃			
			R1LV5256ESA-5SR#B0	33113	-0℃	R1LV5256ESA-5SI#B1 R1LV5256ESA-5SI#S1		
			R1LV5256ESA-5SR#S0		~70℃		55ns	-40℃
			R1LV5256ESA-7SI#B0		-40℃			~85℃
			R1LV5256ESA-7SI#S0	70ns	~85℃			
			R1LV5256ESA-7SR#B0	70113	0℃			
			R1LV5256ESA-7SR#S0		~70℃			
32pin-	1Mb 5V	x8	R1LP0108ESF-5SI#B0	-40℃				
TSOP(I)			R1LP0108ESF-5SI#S0	55ns	~85℃			
			R1LP0108ESF-5SR#B0	55115	-0℃			
			R1LP0108ESF-5SR#S0		~70℃	R1LP0108ESF-5SI#B1	55ns	-40℃
			R1LP0108ESF-7SI#B0		-40℃	R1LP0108ESF-5SI#S1	33113	~85℃
			R1LP0108ESF-7SI#S0	70ns	~85℃			
			R1LP0108ESF-7SR#B0	70115	0℃			
			R1LP0108ESF-7SR#S0		~70℃			
	1Mb 3V	x8	R1LV0108ESF-5SI#B0		-40℃			
			R1LV0108ESF-5SI#S0	55ns	~85℃			
			R1LV0108ESF-5SR#B0		-0℃			
			R1LV0108ESF-5SR#S0		~70℃	R1LV0108ESF-5SI#B1	55ns	-40℃
			R1LV0108ESF-7SI#B0		-40℃	R1LV0108ESF-5SI#S1		~85℃
			R1LV0108ESF-7SI#S0	70ns	~85℃			
			R1LV0108ESF-7SR#B0		0℃			
			R1LV0108ESF-7SR#S0		~70℃			

<sup>• #</sup>B0: Tray packing, #S0: Tape & Reel packing. #B1: Tray packing, #S1: Tape & Reel packing.



# Appendix B (cont.): Temperature Grade Unification

(2) 32pin-sTSOP, 32pin-TSOP(II), 44pin-TSOP(II)

	Memory		Pre Chan	ige		Post Change			
Package Type	Cap., Supply Voltage	bit	Orderable Part Name	Access time	Operation temp.	Orderable Part Name	Access time	Operation temp.	
32pin-	1Mb 5V	x8	R1LP0108ESA-5SI#B0	-40℃					
sTSOP			R1LP0108ESA-5SI#S0	55ns	~85℃				
			R1LP0108ESA-5SR#B0	33115	-0℃				
			R1LP0108ESA-5SR#S0		~70℃	R1LP0108ESA-5SI#B1	55ns	-40℃	
			R1LP0108ESA-7SI#B0		-40℃	R1LP0108ESA-5SI#S1	33113	~85℃	
			R1LP0108ESA-7SI#S0	70ns	~85℃				
			R1LP0108ESA-7SR#B0	70115	0℃				
			R1LP0108ESA-7SR#S0		~70℃				
	1Mb 3V	x8	R1LV0108ESA-5SI#B0		-40℃				
			R1LV0108ESA-5SI#S0	55ns	~85℃				
			R1LV0108ESA-5SR#B0	33115	-0℃	R1LV0108ESA-5SI#B1 R1LV0108ESA-5SI#S1			
			R1LV0108ESA-5SR#S0		~70℃		55ns	-40℃	
			R1LV0108ESA-7SI#B0		-40℃		55115	~85℃	
			R1LV0108ESA-7SI#S0	70ns	~85℃				
			R1LV0108ESA-7SR#B0	70113	0℃				
			R1LV0108ESA-7SR#S0		~70℃				
	2Mb 3V	x8	R1LV0208BSA-5SI#B0	55ns		R1LV0208BSA-5SI#B1	SSDC	-40℃	
			R1LV0208BSA-5SI#S0	00113	-40℃				
			R1LV0208BSA-7SI#B0	70ns	~85℃	R1LV0208BSA-5SI#S1	55115	~85℃	
			R1LV0208BSA-7SI#S0	70113					
32pin-	4Mb 5V	x8	R1LP0408DSB-5SI#B0		-40℃				
TSOP(II)			R1LP0408DSB-5SI#S0	55ns	~85℃				
			R1LP0408DSB-5SR#B0	00115	-0℃				
			R1LP0408DSB-5SR#S0		~70℃	R1LP0408DSB-5SI#B1	55ns	-40℃	
			R1LP0408DSB-7SI#B0		-40℃	R1LP0408DSB-5SI#S1	55115	~85℃	
			R1LP0408DSB-7SI#S0	70ns	~85℃				
			R1LP0408DSB-7SR#B0	70113	0℃				
			R1LP0408DSB-7SR#S0		~70℃				
44pin-	2Mb 3V	x15	R1LV0216BSB-5SI#B0	55ns					
TSOP(II)			R1LV0216BSB-5SI#S0	33113	-40℃	R1LV0216BSB-5SI#B1	55ns	-40℃	
			R1LV0216BSB-7SI#B0	70ns	~85℃	R1LV0216BSB-5SI#S1	33113	~85℃	
			R1LV0216BSB-7SI#S0	70113					

<sup>• #</sup>B0: Tray packing, #S0: Tape & Reel packing. #B1: Tray packing, #S1: Tape & Reel packing.



(1)-a. Electrical characteristics (DC): 256Kb(5V) R1LP5256ESA

### Products

Item	Pre Change	Post Change
Orderable part name	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESA-5SI#B1
	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESA-5SI#S1

### DC conditions

Item	Symbol	Pre Change		Pre Change		Pre Change		Symbol	Post Change
Supply voltage	Vcc		4.5V~5.5V	Vcc	<b>←</b>				
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	_	-40°C to 85°C				
	la la	5SI, 7SI -40°C to 85°C	la la	-40-0 10 85-0					
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	<b>←</b>				
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	<b>←</b>				

### DC characteristics

Item	Symbol	F	Pre Change	Symbol	Po	ost Change
Oti Ct	Icc1(TTL, Min.Cycle)	35mA(r	nax.) / 25mA(typ.)	Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	4mA(r	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)		3mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 0.6uA(typ.)		~25℃	←
		~40℃	3uA(max.)	ISB1(MOS)	~40℃	<b>←</b>
oundby current	ISB1(MOS)	~70℃	8uA(max.)		~70℃	<b>←</b>
		~85°C (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
Output high voltage	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	<b>←</b>
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	<b>←</b>

## Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Symbol Post Chang	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
		~25℃	2uA(max.) / 0.6uA(typ.)		~25℃	←
		~40°C	3uA(max.)	IccDR(Vcc=3.0V)	~40°C	←
Data retention current	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	<b>←</b>	
Operation recovery time	tR	5ms(min.)		tR	<b>←</b>	



(1)-b. Electrical characteristics (AC): 256Kb(5V) R1LP5256ESA

### Products

Item	Pre Change	Post Change
Orderable part name	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESA-5SI#B1
	R1LP5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESA-5SI#S1

### AC characteristics

Item	Symbol		Pre Change	Symbol	Post Change
Seed and a Mari		5SI, 5SR	55ns(min.)	45.5	FF-state \$
Read cycle time	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	FEnglany )
Address access time	DV	7SI, 7SR	70ns(max.)	DVA	55ns(max.)
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
chip select access time	DACS	7SI, 7SR	70ns(max.)	DICS	SSIIs(max.)
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
output enable to output valid	LOE	7SI, 7SR	35ns(max.)		Jona (max.)
Output hold from address	tOH	5SI, 5SR	10ns(min.)	tOH	
change		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	
criip select to output iii low-2		7SI, 7SR	5ns(min.)		
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	+
low-Z	IOLZ	7SI, 7SR	5ns(min.)	tOL2	
Chip deselect to output in	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	Ons(min.) / 20ns(max.)
high-Z	U.MZ	7SI, 7SR	Ons(min.) / 25ns(max.)	0.712	ons(mm.)/ zons(max.)
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
nigh-Z	toH2	7SI, 7SR	Ons(min.) / 25ns(max.)		

Item	Symbol		Pre Change	Symbol	Post Change
Write and time	tWC	5SI, 5SR	55ns(min.)	tWC	FFdada 3
Write cycle time	twc	7SI, 7SR	70ns(min.)	twc	55ns(min.)
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	E0ne/min )
Address valid to end or write	LAW	7SI, 7SR	65ns(min.)	LAW	50ns(min.)
China and and a few dis-	1011	5SI, 5SR	50ns(min.)	1011	FOr effects 3
Chip select to end of write	tCW	7SI, 7SR	65ns(min.)	tCW	50ns(min.)
Malter and an order	41475	5SI, 5SR	40ns(min.)	****	40-state X
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	40ns(min.)
Address as book bloom		5SI, 5SR	Ons(min.)	***	<b>←</b>
Address setup time	tAS	7SI, 7SR	Ons(min.)	tAS	_
Malta vacavani tima	tWR	5SI, 5SR	Ons(min.)	tWR	<b>←</b>
Write recovery time		7SI, 7SR	Ons(min.)		<b>—</b>
Data to wells time availan	tDW	5SI, 5SR	25ns(min.)	tDW	2Fooderin )
Data to write time overlap	tDW	7SI, 7SR	30ns(min.)	tDW	25ns(min.)
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	1011	
Data hold from write time	ton.	7SI, 7SR	Ons(min.)	tDH	<b>←</b>
Output enable from end of	tow	5SI, 5SR	5ns(min.)	LOW.	<b>←</b>
write	tow	7SI, 7SR	5ns(min.)	tOW	-
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Onclario 3 / 20nelmou 3
high-Z	UHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	toH2	Ons(min.) / 20ns(max.)
Melto to output in high 7	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)		Onclario 3 / 20nelmon 3
Write to output in high-Z	CWH2	7SI, 7SR	Ons(min.) / 25ns(max.)	tWHZ	Ons(min.) / 20ns(max.)



(2)-a. Electrical characteristics (DC): 256Kb(3V) R1LV5256ESA

### Products

1100000		
Item	Pre Change	Post Change
Orderable part name	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESA-5SI#B1
	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESA-5SI#S1

### DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V~3.6V		Vcc	←
Operating temperature range	-	5SR, 7SR	0°C to 70°C	Ta	4005 to 0505
	Та	5SI, 7SI	-40°C to 85°C		-40°C to 85°C
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	-
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	<b>←</b>

### DC characteristics

Item	Symbol	Pre Change		Symbol	P	ost Change
	Icc1(TTL, Min.Cycle)	25mA(n	nax.) / 14mA(typ.)	Icc1(TTL, Min.Cycle)	<b>←</b>	
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
	ISB(TTL)	0.	33mA(max.)	ISB(TTL)		←
Standby current	ISB1(MOS)	~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
		~40℃	3uA(max.)		~40°C	←
Sandy Carrent		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	←
Outrot bish outros	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
Output high voltage	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=1mA	0.4V(max.)	VOL	IOL=1mA	←

### Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	<b>←</b>	
		~25℃	2uA(max.) / 0.6uA(typ.)		~25℃	←
		~40°C	3uA(max.)	IccDR(Vcc=3.0V)	~40°C	←
Data retention current	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	<b>←</b>	
Operation recovery time	tR	5ms(min.)		tR	<b>←</b>	



(2)-b. Electrical characteristics (AC): 256Kb(3V) R1LV5256ESA

р.	-		_	
М	ou	u	C	5

Item	Pre Change	Post Change		
Ordershie nest neme	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESA-5SI#B1		
Orderable part name	R1LV5256ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESA-5SI#S1		

### AC characteristics

Item	Symbol	1	Pre Change	Symbol	Post Change
Danid muda Musa	100	5SI, 5SR	55ns(min.)	*80	FF-edesia )
Read cycle time	tRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)
Address access time	tAA	5SI, 5SR	55ns(max.)	AAt	55ns(max.)
Address access unie	8	7SI, 7SR	70ns(max.)	DV	SSIIS(IIIAX.)
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
chip select access time	DACS	7SI, 7SR	70ns(max.)	DICS	SSHS(Hax.)
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
output enable to output valid	LOE	7SI, 7SR	35ns(max.)	IOE	Solis(Illax.)
Output hold from address	tOH	5SI, 5SR	10ns(min.)	tOH	4
change	ton	7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	
crip select to output in low-2		7SI, 7SR	5ns(min.)		
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	<b>+</b>
low-Z	1012	7SI, 7SR	5ns(min.)	tol	_
Chip deselect to output in	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	Ons(min.) / 20ns(max.)
high-Z	U.MZ	7SI, 7SR	Ons(min.) / 25ns(max.)	UCHZ	oris(min.)/ zoris(max.)
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)
high-Z	Onz	7SI, 7SR	Ons(min.) / 25ns(max.)	COTIE	

Item	Symbol		Pre Change	Symbol	Post Change
Weite aude time	tWC	5SI, 5SR	55ns(min.)	tWC	EFederic )
Write cycle time	twc	7SI, 7SR	70ns(min.)	twc	55ns(min.)
Address valid to and affinite	tAW	5SI, 5SR	50ns(min.)	tAW	E0nofesia )
Address valid to end of write	DAW	7SI, 7SR	65ns(min.)	DAW	50ns(min.)
		5SI, 5SR	50ns(min.)		
Chip select to end of write	tCW	7SI, 7SR	65ns(min.)	tCW	50ns(min.)
		5SI, 5SR	40ns(min.)		49-4-1-1
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	40ns(min.)
		5SI, 5SR	Ons(min.)		_
Address setup time	tAS	7SI, 7SR	Ons(min.)	tAS	<b>←</b>
	tWR	5SI, 5SR	Ons(min.)	tWR	_
Write recovery time		7SI, 7SR	Ons(min.)		<b>←</b>
Data to write time quarks		5SI, 5SR	25ns(min.)	tDW	25 notario 3
Data to write time overlap	tDW	7SI, 7SR	30ns(min.)	tow	25ns(min.)
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	+DU	_
Data hold from write time	ton	7SI, 7SR	Ons(min.)	tDH	<b>←</b>
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	tOW	_
write	tow	7SI, 7SR	5ns(min.)	tow	<b>←</b>
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	1017	One factor 3 / 20 cofeeper 3
high-Z	tonz	7SI, 7SR	Ons(min.) / 25ns(max.)	tOHZ	Ons(min.) / 20ns(max.)
Welle to entent in high 7	*******	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	One factor 3 / 20 cofeeper 3
Write to output in high-Z	tWHZ	7SI, 7SR	Ons(min.) / 25ns(max.)		Ons(min.) / 20ns(max.)



(3)-a. Electrical characteristics (DC): 1Mb(5V) R1LP0108ESF, R1LP0108ESA

### Products

Item	Pre Change	Post Change
	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESF-5SI#B1
Orderable part name	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESF-5SI#S1
Orderable part name	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESA-5SI#B1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESA-5SI#S1

### DC conditions

Item	Symbol	Pre Change		Symbol	Post Change	
Supply voltage	Vcc	4.5V~5.5V		Vcc	<b>←</b>	
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Та	-40°C to 85°C	
	la la	5SI, 7SI	-40°C to 85°C	la la	-40 € 10 83 €	
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	4-	
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	<b>←</b>	

### DC characteristics

Item	Symbol	Pre Change		Symbol	Po	ost Change
5	Icc1(TTL, Min.Cycle)	35mA(r	max.) / 25mA(typ.)	Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	5mA(r	max.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)		3mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
		~40°C	3uA(max.)		~40℃	<b>←</b>
oundby current	ISB1(MOS)	~70℃	8uA(max.)		~70℃	<b>←</b>
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	<b>←</b>
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	<b>←</b>
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

### Capacitance

- and an				
Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current		~25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
		~40℃	3uA(max.)		~40℃	<b>←</b>
	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	<b>←</b>	



Appendix C (cont.): Electrical Characteristics
(3)-b. Electrical characteristics (AC): 1Mb(5V) R1LP0108ESF, R1LP0108ESA

Products

Item	Pre Change	Post Change
	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESF-5SI#B1
Orderable part name	R1LP0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESF-5SI#S1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESA-5SI#B1
	R1LP0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESA-5SI#S1

### AC characteristics

Read Cycle		1				
Item	Symbol		Pre Change	Symbol	Post Change	
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)	
Read Cycle time	tric	7SI, 7SR	70ns(min.)	tric	SSIIS(IIIII.)	
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)	
Address access time	DV	7SI, 7SR	70ns(max.)	DO	SSIIS(IIIAX.)	
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	FEnelman )	
unip select access time	DICSI / DICS2	7SI, 7SR	70ns(max.)	UICSI / UICS2	55ns(max.)	
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)	
Output enable to output valid	IOE	7SI, 7SR	35ns(max.)	toe	Suis(illax.)	
Output hold from address	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)	
change	ton	7SI, 7SR	10ns(min.)	ton	Sits(min.)	
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)	
criip select to output iii low-2		7SI, 7SR	10ns(min.)	10121 / 10122	Sis(iiii.)	
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←	
ow-Z	1012	7SI, 7SR	5ns(min.)	TOLZ	-	
Chip deselect to output in	ICH71 / ICH72	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ1 / tCHZ2	One(min ) / 20ne/may )	
high-Z	tCHZ1 / tCHZ2	7SI, 7SR	Ons(min.) / 25ns(max.)	tichzi / tichzz	0ns(min.) / 20ns(max.)	
Output disable to output in	1017	5SI, 5SR	Ons(min.) / 20ns(max.)	1017	Oneforin 1 / 20me/may 1	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	

Item	Symbol		Pre Change	Symbol	Post Change	
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)	
write cycle time	IWC	7SI, 7SR	70ns(min.)	twc	SSIIS(IIIII.)	
Address and after the		5SI, 5SR	50ns(min.)	tAW	FO-dala )	
Address valid to end of write	tAW	7SI, 7SR	55ns(min.)	tAW	50ns(min.)	
Chin adapt to and affects	15111	5SI, 5SR	50ns(min.)	LCIU.	FO-dala 3	
Chip select to end of write	tCW	7SI, 7SR	55ns(min.)	tCW	50ns(min.)	
Material and a solution		5SI, 5SR	45ns(min.)		4F-st-st-3	
Write pulse width	tWP	7SI, 7SR	50ns(min.)	tWP	45ns(min.)	
Address sales time	***	5SI, 5SR	Ons(min.)	tAS	<b>←</b>	
Address setup time	tAS	7SI, 7SR	Ons(min.)		<u> </u>	
Melto vocavioni timo	tWR	5SI, 5SR	Ons(min.)	tWR	<b>←</b>	
Write recovery time	twk	7SI, 7SR	Ons(min.)	twk	-	
Data to unito timo overlan	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)	
Data to write time overlap	tDW	7SI, 7SR	30ns(min.)	tDW		
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	_	
Data noid from write time	ton.	7SI, 7SR	Ons(min.)	LDH	<b>←</b>	
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	tow	_	
write	LOW	7SI, 7SR	5ns(min.)	tow	<b>←</b>	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	One(min ) / 20ne/may )	
high-Z	BORZ	7SI, 7SR	Ons(min.) / 25ns(max.)	ton2	Ons(min.) / 20ns(max.)	
Write to output in high 7	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)	
Write to output in high-Z	twnz	7SI, 7SR	Ons(min.) / 25ns(max.)	WHZ		



(4)-a. Electrical characteristics (DC): 1Mb(3V) R1LV0108ESF, R1LV0108ESA

### Products

1100000		
Item	Pre Change	Post Change
	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESF-5SI#B1
Orderable part name	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESF-5SI#S1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESA-5SI#B1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESA-5SI#S1

### DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V~3.6V		Vcc	<b>←</b>
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	To 4090 to 95	-40°C to 85°C
	la la	5SI, 7SI	-40°C to 85°C	Ta	-40°C to 85°C
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	<b>←</b>
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	<b>←</b>

### DC characteristics

DC Criai acteristics						
Item	Symbol	Pre Change		Symbol	Po	ost Change
	Icc1(TTL, Min.Cycle)	25mA(n	nax.) / 15mA(typ.)	Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)	0.	33mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	~25℃	←
	ISB1(MOS)	~40°C	3uA(max.)		~40℃	←
Sunday current		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

### Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
	IccDR(Vcc=3.0V)	~25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	~25℃	←
		~40℃	3uA(max.)		~40℃	←
Data retention current		~70℃	8uA(max.)		~70℃	←
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



(4)-b. Electrical characteristics (AC): 1Mb(3V) R1LV0108ESF, R1LV0108ESA

Products

Item	Pre Change	Post Change
	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESF-5SI#B1
Orderable part name	R1LV0108ESF-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESF-5SI#S1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESA-5SI#B1
	R1LV0108ESA-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESA-5SI#S1

AC characteristics Read Cycle

Item	Symbol		Pre Change	Symbol	Post Change	
Bood audo timo	tRC	5SI, 5SR	55ns(min.)	tRC		
Read cycle time	IRC	7SI, 7SR	70ns(min.)	IRC	55ns(min.)	
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)	
Address access unie	DO	7SI, 7SR	70ns(max.)	DO	SSHS(Max.)	
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)	
unip select access time	01C31 / 01C32	7SI, 7SR	70ns(max.)	UICSI / UICS2	SSIIS(IIIAX.)	
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)	
output enable to output valid	IOE	7SI, 7SR	35ns(max.)	IOE	Jona, mar.)	
Output hold from address	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)	
change	ton	7SI, 7SR	10ns(min.)	tori	5.5()	
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)	
critip select to output in low-2	10121 / 10122	7SI, 7SR	10ns(min.)	tctzr / tctzz	Sis(iiii.)	
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	<b>←</b>	
ow-Z	1012	7SI, 7SR	5ns(min.)	TOLZ	-	
Chip deselect to output in	tCHZ1 / tCHZ2	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ1 / tCHZ2	Ons(min.) / 20ns(max.)	
high-Z	CONET / CONEZ	7SI, 7SR	Ons(min.) / 25ns(max.)	CONET / CONEZ	ons(min.) / Zons(max.)	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tonz.		

Item	Symbol		Pre Change	Symbol	Post Change	
Write aude time	tWC	5SI, 5SR	55ns(min.)	tWC	FFne/min )	
Write cycle time	twc	7SI, 7SR	70ns(min.)	twc	55ns(min.)	
Address wild be and affective	14141	5SI, 5SR	50ns(min.)		FOr effects 3	
Address valid to end of write	tAW	7SI, 7SR	55ns(min.)	tAW	50ns(min.)	
Ohio colors to and of write	tCW	5SI, 5SR	50ns(min.)	tCW	EQuation )	
Chip select to end of write	tew	7SI, 7SR	55ns(min.)	tcw	50ns(min.)	
Welte mules width	tWP	5SI, 5SR	45ns(min.)	tWP	4Footoolo )	
Write pulse width	twp	7SI, 7SR	50ns(min.)	twp	45ns(min.)	
Address setup time	tAS	5SI, 5SR	Ons(min.)	tAS	4	
Address setup time	UNS	7SI, 7SR	Ons(min.)			
Write recovery time	tWR	5SI, 5SR	Ons(min.)	tWR	<b>←</b>	
write recovery time	LVVK	7SI, 7SR	Ons(min.)	LWK	_	
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)	
Data to write time overlap	LDW	7SI, 7SR	30ns(min.)	LDW	zons(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)	tDH	<b>←</b>	
Data floid from write time	ton	7SI, 7SR	Ons(min.)	tun .	_	
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	tOW	-	
write	LOW	7SI, 7SR	5ns(min.)	tow	<b>←</b>	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	One(min ) / 20ne/may )	
high-Z	ONZ	7SI, 7SR	Ons(min.) / 25ns(max.)		Ons(min.) / 20ns(max.)	
Write to output in high-Z	19947	5SI, 5SR	Ons(min.) / 20ns(max.)	NWU7	One(min ) / 20ne/enry )	
write to output in high-2	tWHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tWHZ	Ons(min.) / 20ns(max.)	



Appendix C (cont.): Electrical Characteristics (5)-a. Electrical characteristics (DC): 2Mb(3V) x8 R1LV0208BSA

### Products

rioducts		
Item	Pre Change	Post Change
Orderable part name	R1LV0208BSA-5SI, -7SI#B0	R1LV0208BSA-5SI#B1
	R1LV0208BSA-5SI, -7SI#S0	R1LV0208BSA-5SI#S1

### DC conditions

DC CONDICTORS								
Item	Symbol	Pre Change	Symbol	Post Change				
Supply voltage	Vcc	2.7V~3.6V	Vcc	←				
Operating temperature range	Ta	-40°C to 85°C	Ta	+				
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)	VIH	<b>←</b>				
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)	VIL	<b>←</b>				

### DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
O	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)		←
Operating Current	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)	0.	33mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 1uA(typ.)	ISB1(MOS)	~25℃	←
		~40℃	3uA(max.)		~40℃	←
	ISB1(MOS)	~70℃	8uA(max.)		~70℃	←
		~85℃	10uA(max.)		~85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
V V	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

### Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
		~25℃	2uA(max.) / 1uA(typ.)	IccDR(Vcc=3.0V)	~25℃	<b>-</b>
Data retention current	IccDR(Vcc=3.0V)	~40℃	3uA(max.)		~40℃	<b>+</b>
Data retenuori current		~70℃	8uA(max.)		~70℃	<b>←</b>
		~85℃	10uA(max.)		~85℃	↓
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	<b>←</b>	



(5)-b. Electrical characteristics (AC): 2Mb(3V) x8 R1LV0208BSA

### Products

1100000									
Item Pre Change		Post Change							
Orderable part name	R1LV0208BSA-5SI, -7SI#B0	R1LV0208BSA-5SI#B1							
	R1LV0208BSA-5SI, -7SI#S0	R1LV0208BSA-5SI#S1							

# AC characteristics Read Cycle

Item	Symbol		Pre Change	Symbol	Post Change	
Dood and time	tRC	5SI	55ns(min.)	tRC	FFdesir \	
Read cycle time	IRC	781	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI	55ns(max.)	tAA	55ns(max.)	
Address access time	DV	7SI	70ns(max.)	DO	SSHS(Max.)	
Chip select access time	tACS1 / tACS2	5SI	55ns(max.)	tACS1 / tACS2	55ns(max.)	
unip select access time	DICS1 / DICS2	781	70ns(max.)	DICSI / DICS2	SSIIS(Max.)	
Outside analysis to autside will d	105	5SI	30ns(max.)	LOE.	30ns(max.)	
Output enable to output valid	tOE	781	35ns(max.)	tOE		
Output hold from address	tOH	5SI	10ns(min.)	1011	-	
change	ton	781	10ns(min.)	tOH		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI	10ns(min.)	tCLZ1 / tCLZ2	. ←	
chip select to output in low-2		7SI	10ns(min.)	10121 / 10122	-	
Output enable to output in	tOLZ	5SI	5ns(min.)	tOLZ	-	
ow-Z	toLz	7SI	5ns(min.)	TOLZ	+	
Chip deselect to output in	tCHZ1 / tCHZ2	5SI	Ons(min.) / 20ns(max.)	tCHZ1 / tCHZ2	One/min \ / 20ne/may \	
high-Z	CONZI / CONZZ	781	Ons(min.) / 25ns(max.)	CHZI / CHZZ	Ons(min.) / 20ns(max.)	
Output disable to output in	tOHZ	5SI	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
high-Z	tOHZ	781	Ons(min.) / 25ns(max.)	TONZ		

Item	Symbol		Pre Change	Symbol	Post Change	
Meller and News	41415	5SI	55ns(min.)		EFectorie N	
Write cycle time	tWC	7SI	70ns(min.)	tWC	55ns(min.)	
Address valid to end of write	tAW	5SI	50ns(min.)	tAW	E0nofesia )	
Address valid to end of write	DAW	7SI	55ns(min.)	DAW	50ns(min.)	
Chip select to end of write	tCW	5SI	50ns(min.)	tCW	50ns(min.)	
Chip select to end of write	ICW	7SI	55ns(min.)	CCW	Sons(min.)	
Write pulse width	tWP	5SI	45ns(min.)	tWP	45ns(min.)	
write pulse width	LWF	781	50ns(min.)	LWF	45ns(min.)	
Address setup time	tAS	5SI	Ons(min.)	tAS	←	
Address setup time	UNS	7SI	Ons(min.)			
Write recovery time	tWR	5SI	Ons(min.)	tWR	←	
Write recovery diffe	LWK	7SI	Ons(min.)			
Data to write time overlap	tDW	5SI	25ns(min.)	tDW	25ns(min.)	
bata to write time overlap	tow.	7SI	30ns(min.)	tow .	zons(min.)	
Data hold from write time	tDH	5SI	Ons(min.)	tDH	<b>←</b>	
Data fiold from write time	ton.	7SI	Ons(min.)		_	
Output enable from end of	tOW	5SI	5ns(min.)	tow	-	
write	tow	7SI	5ns(min.)	tow		
Output disable to output in	tOHZ	5SI	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
high-Z	WHZ.	7SI	Ons(min.) / 25ns(max.)	tonz.	ons(mm.)/ zons(max.)	
Write to output in high-Z	tWHZ	5SI	Ons(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)	
Write to output in high-2	CWITZ	781	Ons(min.) / 25ns(max.)	CWHZ		



(6)-a. Electrical characteristics (DC): 4Mb(5V) x8 R1LP0408DSB

### Products

rioduces		
Item	Pre Change	Post Change
Orderable part same	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSB-5SI#B1
Orderable part name	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSB-5SI#S1

### DC conditions

Item	Symbol	Pre Change		Symbol	Post Change	
Supply voltage	Vcc	4.5V~5.5V		Vcc	<b>←</b>	
Oncombine to construct on the construction of	-	5SR, 7SR	0°C to 70°C		-40°C to 85°C	
Operating temperature range	Та	5SI, 7SI	-40°C to 85°C	Та		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	<b>←</b>	
Input low voltage	VIL	-0.3V(i	-0.3V(min.) / 0.8V(max.)		<b>←</b>	

### DC characteristics

Item	Symbol	Pre Change		Symbol	Po	st Change
	Icc(TTL)	10mA(max.) / 5mA(typ.)		Icc(TTL)	←	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(	max.) / 15mA(typ.)	Icc1(TTL, Min.Cycle)		←
	Icc2(MOS, Cycle=ius)	5mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	←	
	ISB(TTL)	0.5mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
		~25°C	2.5uA(max.) / 0.8uA(typ.)		~25℃	<b>←</b>
Standby current		~40°C	3uA(max.) / 1uA(typ.)		~40℃	←
	ISB1(MOS)	~70°C	8uA(max.)	ISB1(MOS)	~70℃	<b>←</b>
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>-</b>
Subsuit high units as	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	<b>←</b>
Output high voltage	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2.1mA	0.4V(max.)	VOL	IOL=2.1mA	<b>←</b>

### Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR		2.0V(min.)		←	
		~25℃	2.5uA(max.) / 0.8uA(typ.)		~25°C	<b>-</b>
		~40°C	3uA(max.) / 1uA(typ.)	IccDR(Vcc=3.0V)	~40°C	<b>←</b>
Data retention current	IccDR(Vcc=3.0V)	~70℃	8uA(max.)		~70℃	<b>←</b>
		~85℃ (for 5SI, 7SI)	10uA(max.)		~85℃	<b>←</b>
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	



Appendix C (cont.): Electrical Characteristics (6)-b. Electrical characteristics (AC): 4Mb(5V) x8 R1LP0408DSB

Рг		

Item	Pre Change	Post Change
Orderable and asses	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSB-5SI#B1
Orderable part name	R1LP0408DSB-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSB-5SI#S1

### AC characteristics

1	_	 	

Item	Symbol		Pre Change	Symbol	Post Change	
Dand and there	tRC	5SI, 5SR	55ns(min.)	tRC	4	
Read cycle time	BRC	7SI, 7SR	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI, 5SR	55ns(max.)		FEncional )	
Address access time	DOL	7SI, 7SR	70ns(max.)	tAA	55ns(max.)	
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)	
chip select access time	DACS	7SI, 7SR	70ns(max.)	UNCS	oons(max.)	
Output enable to output valid	tOE	5SI, 5SR	25ns(max.)	tOE	25ns(max.)	
output enable to output valid	IOE	7SI, 7SR	35ns(max.)	toe.	25/15(//lax.)	
This select to section to less 7	tCLZ	5SI, 5SR	10ns(min.)	tCLZ	-	
Chip select to output in low-Z		7SI, 7SR	10ns(min.)			
Output enable to output in	tOLZ	5SI, 5SR	5ns(min.)	tOLZ		
ow-Z	toL2	7SI, 7SR	5ns(min.)		+	
Chip deselect to output in	tCHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tCHZ	One/min \ / 20ne/may \	
high-Z	tich2	7SI, 7SR	Ons(min.) / 25ns(max.)	tonz	Ons(min.) / 20ns(max.)	
Output disable to output in	1017	5SI, 5SR	Ons(min.) / 20ns(max.)	10117	Onelmin \ / 20nelmay \	
high-Z	tOHZ	7SI, 7SR	Ons(min.) / 25ns(max.)	tOHZ	Ons(min.) / 20ns(max.)	
Output hold from address	1011	5SI, 5SR	10ns(min.)	HOH	-	
change	tOH	7SI, 7SR	10ns(min.)	tOH	-	

Item	Symbol		Pre Change	Symbol	Post Change	
Market and a Mark		5SI, 5SR	55ns(min.)		FF-referie 3	
Write cycle time	tWC	7SI, 7SR	70ns(min.)	tWC	55ns(min.)	
Chin celest to and of units	tcw	5SI, 5SR	50ns(min.)	tCW	Final min	
Chip select to end of write	tCW	7SI, 7SR	60ns(min.)	tcw	50ns(min.)	
Address setup time	tAS	5SI, 5SR	Ons(min.)	tAS	<b>+</b>	
Address setup time	DAS	7SI, 7SR	Ons(min.)	UAS	-	
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	E0ne/min )	
Address valid to end of write	DAW	7SI, 7SR	60ns(min.)	D(W	50ns(min.)	
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)	
write pulse width	CHP	7SI, 7SR	50ns(min.)		10.0(1111.)	
Write recovery time	tWR	5SI, 5SR	Ons(min.)	tWR	<b>←</b>	
write recovery time		7SI, 7SR	Ons(min.)			
Write to output in high-Z	tWHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tWHZ	Ons(min.) / 20ns(max.)	
Write to output in high-2	CWIL	7SI, 7SR	Ons(min.) / 25ns(max.)			
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)	
Data to write time overlap	LDW	7SI, 7SR	30ns(min.)	W.	25/ls(min.)	
Data hold from write time	tDH	5SI, 5SR	Ons(min.)		<b>←</b>	
Data noid from write time	ton	7SI, 7SR	Ons(min.)	tDH		
Output enable from end of	tOW	5SI, 5SR	5ns(min.)	1011	-	
write	tow	7SI, 7SR	5ns(min.)	tOW	-	
Output disable to output in	tOHZ	5SI, 5SR	Ons(min.) / 20ns(max.)	tOHZ	Operania ) / 20perany )	
high-Z	tonz	7SI, 7SR	Ons(min.) / 25ns(max.)	tonz	Ons(min.) / 20ns(max.)	



(7)-a. Electrical characteristics (DC): 2Mb(3V) x16 R1LV0216BSB

Item	Pre Change	Post Change
Orderable part name	R1LV0216BSB-5SI, -7SI#B0	R1LV0216BSB-5SI#B1
	R1LV0216BSB-5SI, -7SI#S0	R1LV0216BSB-5SI#S1

### DC conditions

DC CONDICONS						
Item	Symbol	Pre Change	Symbol	Post Change		
Supply voltage	Vcc	2.7V~3.6V	Vcc	<b>←</b>		
Operating temperature range	Ta	-40°C to 85°C	Ta	+		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)	VIH	-		
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)	VIL	<b>←</b>		

### DC characteristics

Item	Symbol	P	re Change	Symbol	Po	st Change
	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	<b>←</b>	
Operating Current	Icc2(MOS, Cycle=1us)	5mA(n	nax.) / 2mA(typ.)	Icc2(MOS, Cycle=1us)		←
Standby current	ISB(TTL)	0.	.5mA(max.)	ISB(TTL)		←
		~25℃	2uA(max.) / 1uA(typ.)	ISB1(MOS)	~25℃	←
		~40℃	3uA(max.)		~40℃	←
	ISB1(MOS)	~70℃	8uA(max.)		~70℃	←
		~85℃	10uA(max.)		~85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
Output high voltage	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

### Capacitance

capacitairee				
Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	<b>←</b>	
Data retention current	IccDR(Vcc=3.0V)	~25℃	2uA(max.) / 1uA(typ.)	IccDR(Vcc=3.0V)	~25℃	<b>.</b>
		~40℃	3uA(max.)		~40℃	↓
		~70℃	8uA(max.)		~70℃	←
		~85℃	10uA(max.)		~85℃	↓
Chip deselect time to data retention	tCDR	Ons(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	<b>←</b>	



Appendix C (cont.): Electrical Characteristics (7)-b. Electrical characteristics (AC): 2Mb(3V) x16 R1LV0216BSB

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0216BSB-5SI, -7SI#B0	R1LV0216BSB-5SI#B1
	R1LV0216BSB-5SI, -7SI#S0	R1LV0216BSB-5SI#S1

### AC characteristics

Item	Symbol		Pre Change	Symbol	Post Change	
Donal and a Marc	100	5SI	55ns(min.)	+D.C	FF-odosio 3	
Read cycle time	tRC	7SI	70ns(min.)	tRC	55ns(min.)	
Address access time	tAA	5SI	55ns(max.)	tAA 55ns/max.	55ns(max.)	
Address access time	DO	7SI	70ns(max.)	DO	SSHS(Max.)	
Chip select access time	tACS	5SI	55ns(max.)	tACS	55ns(max.)	
unip select access time	DACS	7SI	70ns(max.)	DACS	SSIS(IIIAX.)	
Output enable to output valid	tOE	5SI	30ns(max.)	tOE	30ns(max.)	
output enable to output valid	toE	7SI	35ns(max.)	toE	Sons(max.)	
Output hold from address	tOH	5SI	10ns(min.)	tOH	-	
change	ton	7SI	10ns(min.)	ton		
	tBA	5SI	55ns(max.)	tBA	55ns(max.)	
LB#,UB# access time	tbA	7SI	70ns(max.)	tbA	sons(max.)	
Chip select to output in low-Z	tCLZ	5SI	10ns(min.)	tCLZ	÷	
chip select to output in low-2	ticiz	781	10ns(min.)		_	
LB#,UB# enable to low-Z	tBLZ	5SI	10ns(min.)	tBLZ	-	
LB#,0B# enable to low-2	IBLZ	781	10ns(min.)		_	
Output enable to output in	tOLZ	5SI	5ns(min.)	tOLZ	-	
low-Z	toL2	781	5ns(min.)			
Chip deselect to output in	tCHZ	5SI	Ons(min.) / 20ns(max.)	tCHZ	Onelwin \ / 20nelmay \	
high-Z	U.HZ	781	Ons(min.) / 25ns(max.)	U.HZ	Ons(min.) / 20ns(max.)	
LB#,UB# disable to high-Z	tBHZ	5SI	Ons(min.) / 20ns(max.)	tBHZ	Onelmin \ / 20nelmer \	
Lb#,Ub# disable to high-Z	UDFIZ	7SI	Ons(min.) / 25ns(max.)	UDFIZ	Ons(min.) / 20ns(max.)	
Output disable to output in	tOHZ	5SI	Ons(min.) / 20ns(max.)	tOHZ	One(min ) / 20me/may )	
high-Z	WHZ	7SI	Ons(min.) / 25ns(max.)	UHZ	Ons(min.) / 20ns(max.)	

Item	Symbol		Pre Change	Symbol	Post Change
Marke and Mark	*****	5SI	55ns(min.)		EF-state 3
Write cycle time	tWC	781	70ns(min.)	tWC	55ns(min.)
Address valid to end of write	tAW	5SI	50ns(min.)		FOne(min )
Address valid to end or write	DAW	781	55ns(min.)	tAW	50ns(min.)
Chip select to end of write	tCW	5SI	50ns(min.)	tCW	E0ne/min )
Chip select to end of write	CCAA	781	55ns(min.)	ticw	50ns(min.)
Write pulse width	tWP	5SI	45ns(min.)	tWP	45ns(min.)
write pulse width	LWP	7SI	50ns(min.)	LWP	45ns(min.)
LB#,UB# valid to end of write	tBW	5SI	50ns(min.)	tBW 50	50ns(min.)
LB#, UB# Valid to end of Write	LDW	7SI	55ns(min.)		Sons(min.)
Address setup time	tAS	5SI	Ons(min.)	tAS	<b>←</b>
Address setup time	UIS	7SI	Ons(min.)	043	_
Write recovery time	tWR	5SI	Ons(min.)	tWR	<b>←</b>
write recovery time	LWK	7SI	Ons(min.)	twk	-
Data to write time overlap	tDW	5SI	25ns(min.)	tDW	25ns(min.)
Data to write time overlap	LDW	7SI	30ns(min.)	LDW	
Data hold from write time	tDH	5SI	Ons(min.)	tDH ←	-
Data floid from write time	CDIT	7SI	Ons(min.)		_
Output enable from end of	tOW	5SI	5ns(min.)	tOW	←
write	tow	7SI	5ns(min.)	1011	-
Output disable to output in	tOHZ	5SI	Ons(min.) / 20ns(max.)	tOHZ	Ons(min.) / 20ns(max.)
high-Z	CONE	7SI	Ons(min.) / 25ns(max.)	OONE	ons(mm.)/ zons(max.)
Write to output in high 7	tWHZ	5SI	Ons(min.) / 20ns(max.)	tWHZ	One(min ) / 20ne/may )
Write to output in high-Z	twhz	781	Ons(min.) / 25ns(max.)	twH2	Ons(min.) / 20ns(max.)



## Appendix D: JEDEC Tray and Tape & Reel Unification Details

- (1) Change the specification of the JEDEC tray
  - The package seat position in tray pocket is to be changed (see below).
  - No change in outline dimensions and pocket pitch for JEDEC tray.

	Dackage	Pre Change		Post Change		
	Package type	Tray type name	PKG seat position (mm)	Tray type name	PKG seat position (mm)	
JEDEC tray	28pin-TSOP(I), 32pin-sTSOP	L196-10	2.0	EA50813	1.85	
	32pin-TSOP(I)	L196-20	2.1	EA50820	1.5	
	32pin-TSOP(II)	L196-93	2.0	EA80817	2.0	
	44pin-TSOP(II)	L196-92	2.0	EA80815	2.0	
	48pin-TSOP(I)	L196-126	2.0	EA51220	1.5	



Cross section of tray pocket

## (2) Laying direction of ICs on a tray

- Regarding R1RP0416DSB, R1RW0416DSB and R1LV1616HSA, laying direction of ICs on a tray is to be changed (see below).
- No change in other products, because the direction is already same as the "Post Change" as shown below.

	Pre Change	Post Change
Laying direction of ICs on a tray	Direction 1	Direction
Orderable part name	R1RP0416DSB-xxx #D0 R1RW0416DSB-xxx #D0 R1LV1616HSA-xxx #B0	R1RP0416DSB-xxx #D1 R1RW0416DSB-xxx #D1 R1LV1616HSA-xxx #B1



## Appendix D (cont.): JEDEC Tray and Tape & Reel Unification Details

- (3) Change the specification of the Tape & Reel
  - The package seat position in taping pocket is to be changed (see below).
  - No change in width and pitch of embossed carrier tape.
  - No change in reel diameter.

	Deelsess	Pre Cha	ange	Post Change		
	Package type	Emboss type name	PKG seat position (mm)	Emboss type name	PKG seat position (mm)	
Embossed carrier	28pin-TSOP(I), 32pin-sTSOP	MTE2412H-28P2C-A	1.3	TSOP28	1.4	
tape	32pin-TSOP(I)	MTE3212H-32P3H-A	1.25	TSOP32-1	1.4	
	32pin-TSOP(II)	MTE3216H-50P3W	1.2	TSOP32-6	1.3	
	44pin-TSOP(II)	MTE3216H-28P3Y	1.2	TSOP44-3	1.3	
	48pin-TSOP(I)	TE3216-16P	1.2	TSOP48-3	1.2	



Cross section of taping pocket