Dual Channel, Configurable, Isolated Digital Input

Data Sheet

ADE1202

FEATURES

- **Dual channel, configurable, isolated digital input**
- **Programmable trip threshold**
- **On-chip debounce filter**
- **On-chip data and power Isolation**
- **Application circuit monitors wide voltage range**
  - **10 V dc to 300 V dc**
  - **8 V rms to 240 V rms ac (with 10 ms + pickup)**
  - **Negative dc protected**
- **Programmable wetting current**
  - **Pulse up to 50 mA**
  - **Constant current up to 6.3 mA**
- **Safety and regulatory approvals**
  - **UL recognition**
    - **3750 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A (pending)**
    - **CSA 61010-1: 300 V rms**
  - **VDE certificate of conformity (pending)**
    - **DIN V VDE V 0884-11 (VDE V 0884-11):2017-1**
    - **V_{IORM} = 565 V peak**
- **EMC robust solution supports relay protection system level requirements**
- **ADC samples available for system diagnostics**
- **Internal SAR ADC with PGA**
- **Single 3.3 V Supply**
  - **Integrated *iso*Power, isolated dc-to-dc converter**
- **Interfaces**
  - **SPI**
  - **$\overline{\text{DOUT}}$x output reflects state of digital input**
  - **$\overline{\text{IRQ}}$ interrupt pin**
- **Operating temperature: −40°C to +125°C**
- **20-lead, LGA package with 6.8 mm creepage**

APPLICATIONS

- **Energy transmission and distribution**
  - **Multifunction relay protection**
  - **Substation battery monitoring**
  - **Bay or substation interlocking**
  - **Merge unit**
  - **Circuit breaker status indication**
  - **Remote terminal unit**
- **Building automation**

GENERAL DESCRIPTION

The ADE1202[1] is a dual channel, configurable, isolated digital input monitoring solution for energy transmission and distribution applications. The ADE1202 is configured through the serial port interface (SPI) to perform an isolated measurement of the digital input that is also called binary input or contact input. The ADE1202 digital output signal on the DOUTx pins reflects the state of the input signal after user configurable signal conditioning. The SPI protocol supports addressing to allow up to eight devices sharing one 4-wire SPI port.

The ADE1202 application circuit accepts a wide range of input voltages from 10 V dc to 300 V, or 8 V rms to 240 V rms. The programmable wetting current and robust application circuit enable the device to meet stringent, system level electromagnetic capability (EMC) requirements.

The ADE1202 includes an *iso*Power® integrated, isolated dc-to-dc converter that eliminates the need for an external isolated power supply. The *i*Coupler® chip scale transformer technology is used to isolate the logic signals between the high voltage, isolated side and the low voltage, nonisolated side of the digital input monitor. This technology creates a small form factor design that includes data and power isolation.

An integrated successive approximation register (SAR) analog-to-digital converter (ADC) and a programmable gain amplifier (PGA) from 1× to 10× measure the analog inputs. The ADC waveforms are available through the SPI port to allow system level diagnostics.

Note that throughout this data sheet, multifunction pins, such as DOUT2/$\overline{\text{IRQ}}$, are referred to either by the entire pin name or by a single function of the pin, for example, DOUT2, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Dual channel, configurable, isolated digital input.
2. Single hardware design supports 24 V to 300 V systems.
3. Robust architecture.
4. Enables system level diagnostics.

[1] Protected by U.S. Patent Number 2017/0250043. Other patents pending.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

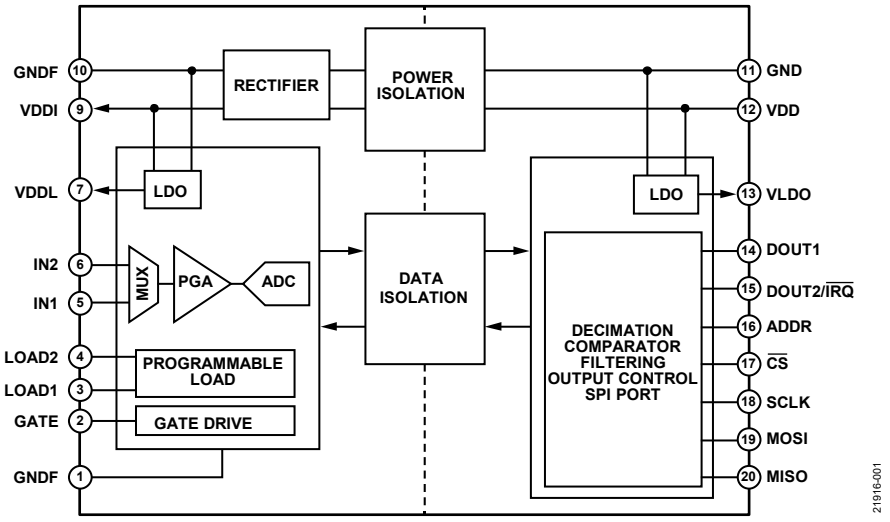


Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, and all specifications at T_A = −40°C to +125°C, unless otherwise noted.

Table 1. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS (IN1, IN2)						
Input Voltage Range	V_{IN}	0		1.25/PGA	V	PGA = 1, 2, 5, and 10
Input Sampling Current	I_{INx}	−50		+50	nA	PGA = 1, 2, 5, and 10
GATE DRIVE (GATE)						
Output Voltage	$V_{GATENOM}$		6.9		V	
Output Current	I_{GATE}			3.5	µA	$V_{GATENOM}$ = 6.6 V
PROGRAMABLE LOAD (LOADx)						
Leakage Resistance			58		kΩ	Programmable load is disabled
Constant Current						
Resolution			6		bits	
Range		0.11		6.3	mA	Typical programmable range
Total Unadjusted Error (TUE)[1]		−4.5		+4.5	%FSR	
TUE at 25°C[1]		−2		+3.5	%FSR	
Integral Nonlinearity (INL)		−1		+1	LSB	
Differential Nonlinearity (DNL)		−0.5		+0.5	LSB	
Offset		8	10	15	µA	
Gain Error		−7	+0.1	+5.7	%FSR	Measured at Code 63 compared to ideal value of 6.3 mA
Code 22[1]		2		2.5	mA	
Code 63[1]		5.8		6.7	mA	
Pulsed Current						
Resolution			8		bits	
Range		0.21		51	mA	Typical programmable range
TUE[1]		−4.5		+4.5	%FSR	
TUE at 25°C[1]		−2		+3.5	%FSR	
INL		−0.8		+2.1	LSB	
DNL		−1.2		+1.4	LSB	
Offset		9	10	14.5	µA	
Gain Error		−7	+0.2	+6	%FSR	Measured at Code 255 compared to ideal value of 51 mA
Code 255[1]		47		54	mA	
THERMAL SHUTDOWN						See Thermal Shutdown section
Threshold[1]	T_{SD}		170		°C	Junction temperature
Hysteresis[1]			25		°C	
ISOLATION COMMON-MODE TRANSIENT IMMUNITY (CMTI)						Common-mode voltage ($\|V_{CM}\|$) = 2 kV
Static			50		kV/ µS	
ADDR PIN INPUT						
Input Current	I_{INH}			1	µA	
Input Current	I_{INL}			1	µA	
LOGIC INPUTS (MOSI, SCLK, $\overline{CS}$)						
Input High Voltage	V_{INH}	2.4			V	
Input Low Voltage	V_{INL}			0.8	V	
Input High Current	I_{INH}			1	µA	
Input Low Current	I_{INL}			10	µA	
Input Capacitance[1]	C_{IN}			10	pF	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (MISO, DOUT1, DOUT2/$\overline{IRQ}$)						The DOUT2/$\overline{IRQ}$ pin is open-drain when configured as $\overline{IRQ}$
Output High Voltage	V_{OH}	2.4			V	Source current (I_{SOURCE}) = 3.5 mA
Output Low Voltage	V_{OL}			0.4	V	Sink current (I_{SINK}) = 3.5 mA
POWER SUPPLY						
Operating Voltage Range	V_{DD}	2.97		3.63	V	
Supply Current	I_{DD}	3.3	4.3	6.7	mA	

[1] Guaranteed by design and characterization.

Table 2. SAR, ADC, and PGA Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPEED AND PERFORMANCE					
ADC Resolution		8		bits	No missing codes
Throughput[1]		100		kSPS	
SIGNAL-TO-NOISE RATIO (SNR)					
PGA = 1, 2, 5		48		dB	
PGA = 10		46		dB	
DC ACCURACY					
INL		±0.25		LSB	
DNL		±0.25		LSB	
Gain Error	−2.5		+2.5	%FSR	PGA = 1, 2, 5, 10
Offset Error	−3		+3	LSB	PGA = 1, 2, 5, 10

[1] The ADC is multiplexed between sampling IN1 and IN2, resulting in 50 kSPS per channel.

TIMING CHARACTERISTICS

Table 3. Input Signal Timing Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Signal Filter Resolution[1]		20		µs	
Time Delay from Step Change on INx Input to DOUTx Change State	60	86	110	µs	BIN_FILTER_VAL = 3, with step on INx from 0 V to 0.8 V
Power-Up Time		110		ms	With initial VDDI = 0 V, using recommended circuit in Figure 23
ADDR Pin Load Time[1]		320		µs	After power-on (see Figure 25)

[1] Guaranteed by design.

Table 4. Programmable Load Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Turn On Rise Time	t_R	2		9	µs	In high idle mode with a 50 mA pulse
Pulsed Current On Time	t_{PK}	4	4.1	4.3	ms	HIGH_TIME = 400
Turn Off Fall Time	t_F			0.025	µs	

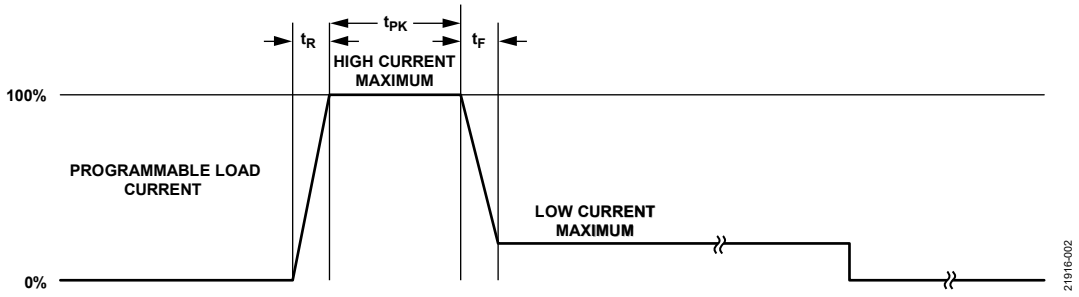


Figure 2. Programmable Load Switching Characteristics

Table 5. SPI Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ to SCLK Negative Edge	t_{SS}	10			ns
SCLK Frequency[1]	f_{SCLK}	0.00025		10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Rise Time	t_{SR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}			100	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0			ns

[1] Guaranteed by design and characterization.

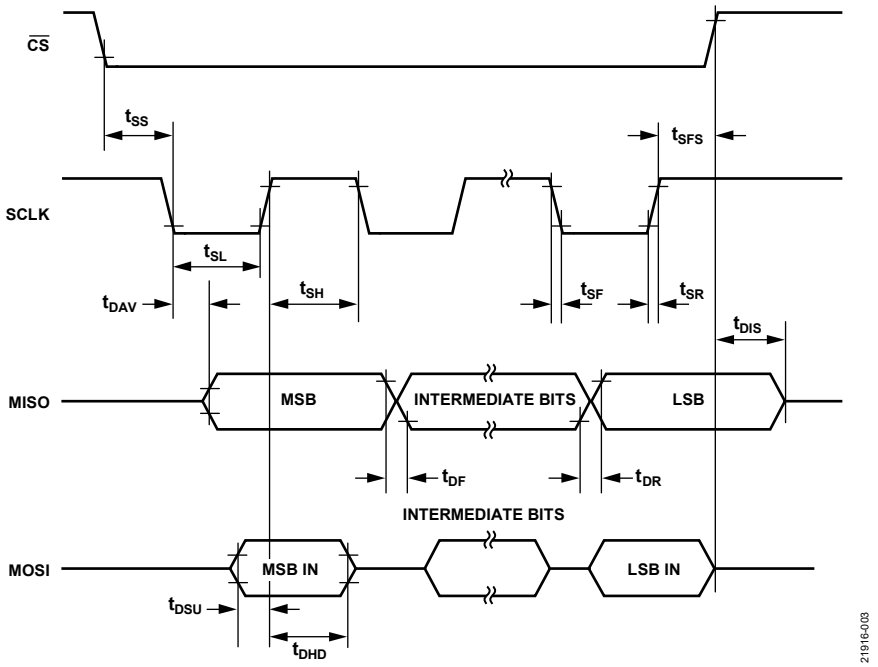


Figure 3. SPI Timing

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 6.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	6.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	6.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB)	L (PCB)	6.8	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21	µm min	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.25		pF	f = 1 MHz

[1] The device is considered a 2-terminal device. Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.

REGULATORY INFORMATION

The ADE1202 is pending approval by the organizations listed in Table 8.

Table 8. Approvals

UL	CSA (Pending)	VDE (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-1[2]
Single Protection, 3750 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 640 V rms (904 V peak) Reinforced insulation at 320 V rms (452 V peak) IEC 60601-1 Edition 3.1: 1 means of patient protection (MOPP), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms Mains, 640 V rms (904 V peak) Reinforced insulation at 300 V rms Mains, 320 V secondary (452 V peak)	Reinforced insulation, V_{IORM} = 565 V peak, V_{IOTM} = 8 kV peak, $V_{IMPULSE}$ = 8 kV peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage of ≥4500 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-11, each product is proof tested by applying an insulation test voltage of ≥1059 V peak for 1 sec.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

This isolator is suitable for electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on a package denotes VDE 0884 approval for a 707 V peak working voltage.

Table 9.

Description	Symbol	Test Conditions/Comments	Characteristic	Unit
Installation Classification per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage	V_{IORM}		565	V peak
Input to Output Test Voltage, Method b1	$V_{pd(m)}$	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	1060	V peak
Input to Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{pd(m)}$	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{pd(m)}$	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	678	V peak
Highest Allowable Overvoltage	V_{IOTM}		8000	V peak
Impulse	$V_{IMPULSE}$	1.2 µs rise time, 50 µs, 50% fall time in air, to the preferred sequence	8000	V peak
Withstand Isolation Voltage	V_{ISO}	1 minute withstand rating	3750	V_{RMS}
Surge Isolation Voltage Reinforced	V_{IOSM}	V peak = $1.3 \times V_{IMPULSE}$, 1.2 µs rise time, 50 µs, 50% fall time	10400	V peak
Safety Limiting Values		Maximum value allowed in the event of a failure (see Figure 4)		
Maximum Ambient Temperature	T_S		125	°C
Total Power Dissipation[1] at 25°C	I_{S1}		0.75	W
Insulation Resistance at T_S	R_S	V_{IO} = 500 V	$>10^9$	Ω

[1] This is the maximum power dissipation to guarantee insulation integrity.

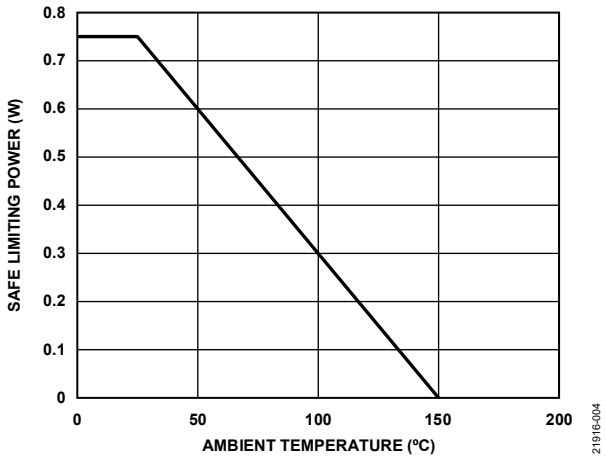


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature, per DIN V VDE V 0884-11

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
VDD to GND	−0.3 V to +3.7 V
IN1, IN2 to GNDF	−0.2 V to +2 V
LOAD1, LOAD2 to GNDF	−0.3 V to +7.7 V
GATE to GNDF	−0.3 V to +7.7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[1]	300°C
Electrostatic Discharge (ESD)	
Human Body Model[2]	±5 kV
Field Induced Charged Device Model (FICDM)[3]	±1.5 kV

[1]Analog Devices, Inc., recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.
[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.
[3] Applicable standard: JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance. θ_{JC} is the junction to case thermal resistance. Ψ_{JT} is the junction to top characterization parameter.

Table 11. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
CC-20-5	168	76	12	°C/W

[1] Based on simulated data using a JEDEC 2s2p thermal test board in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

ESD CAUTION

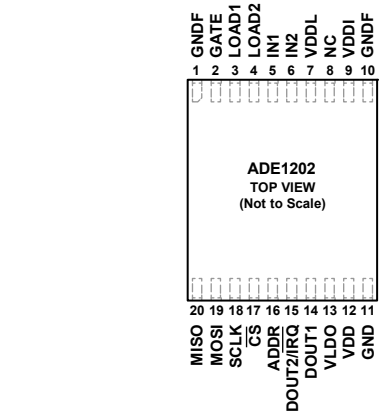
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 12. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard[2]
AC Voltage			
Bipolar Waveform			
Basic Insulation	636	V peak	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	537	V peak	Lifetime limited by package creepage per IEC 60664-1
Unipolar Waveform			
Basic Insulation	1242	V peak	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	621	V peak	Lifetime limited by package creepage per IEC 60664-1
DC Voltage			
Basic Insulation	760	V peak	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	380	V peak	Lifetime limited by package creepage per IEC 60664-1

[1] The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Wear Out section for more details.
[2] Insulation lifetime for the specified test condition is greater than 50 years.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THIS PIN IS INTERNALLY PULLED DOWN TO GNDF. IT IS RECOMMENDED TO TIE THIS PIN TO GNDF EXTERNALLY.

21916-005

Figure 5. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GNDF	The GNDF pin located at Pin 1 is used to provide a return path for current from the internal programmable load. Both Pin 1 and Pin 10 must be connected to ground externally. See the Layout Guidelines section for recommendations on how to connect this pin.
2	GATE	Use this pin to drive the gate pins of two enhancement mode field effect transistors (FETs), one for each channel of the ADE1202.
3, 4	LOAD1, LOAD2	Programmable Loads. Use these pins to command a preset current required for loading the relay contacts.
5, 6	IN1, IN2	Digital Input Pins. The scaled input signals are applied at these pins.
7	VDDL	1.8 V Output of the Analog Low Dropout (LDO) Regulator. Do not connect external load circuitry to this pin. Decouple this pin to GNDF with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations on how to connect this pin.
8	NC	No Connect. This pin is internally pulled down to GNDF. It is recommended to tie this pin to GNDF externally.
9	VDDI	Isolated Secondary Side Power Supply Output Pin. This pin provides access to the 2.0 V, on-chip isolated power supply. Decouple this pin to GNDF with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations on how to connect this pin. Do not connect external load circuitry to this pin.
10	GNDF	The GNDF pin located at Pin 10 is used as a reference for the internal, isolated power supply and the LDO regulator. Both Pin 1 and Pin 10 must be connected to ground externally. See the Layout Guidelines section for recommendations on how to connect this pin.
11	GND	GND Pin. This pin is the system controller side ground pin.
12	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE1202. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to the GND pin with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations on how to connect this pin.
13	VLDO	1.8 V Output of the LDO Regulator. Decouple this pin to the GND pin with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations on how to connect this pin. Do not connect external load circuitry to this pin.
14	DOUT1	Digital Data Output Pin. This pin operates in a push/pull mode. This pin transitions to logic high, V_{INH}, or logic low, V_{INL}, replicating the digital input signal at the IN1 pin.
15	DOUT2/$\overline{IRQ}$	Digital Data Output Pin. When configured as DOUT2, this pin operates in a push/pull mode and transitions to V_{INH} or V_{INL} replicating the digital input signal at the IN2 pin. When configured as an interrupt, $\overline{IRQ}$, the pin is open-drain and a 10 kΩ pull-up resistor to the VDD voltage is recommended.
16	ADDR	Address Mode Pin. This pin is used for multichip addressing. If multichip addressing is not used, connect this pin to ground. The address divider requires 1% resistors, as described in the SPI ADE1202 Addressing section.
17	$\overline{CS}$	Chip Select for SPI Port.
18	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock.
19	MOSI	Data Input for SPI Port.
20	MISO	Data Output for SPI Port.

TYPICAL PERFORMANCE CHARACTERISTICS

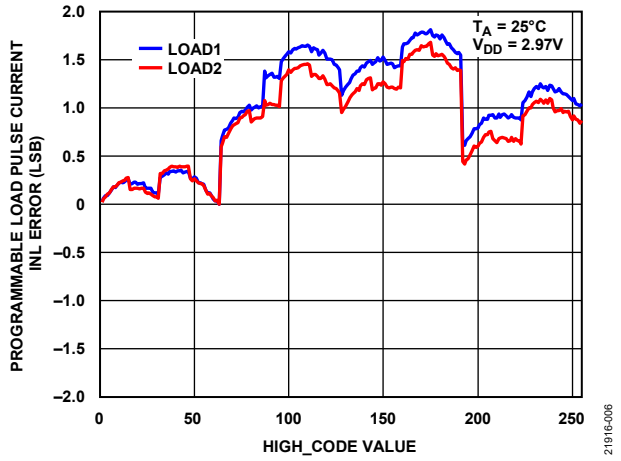


Figure 6. Programmable Load Pulse Current INL Error vs. HIGH_CODE Value

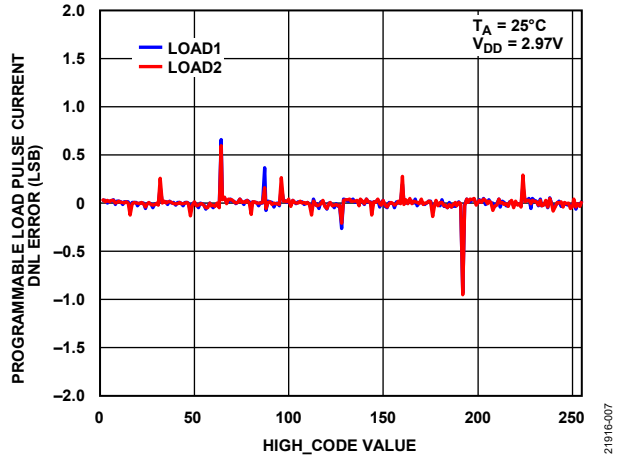


Figure 7. Programmable Load Pulse Current DNL Error vs. HIGH_CODE Value

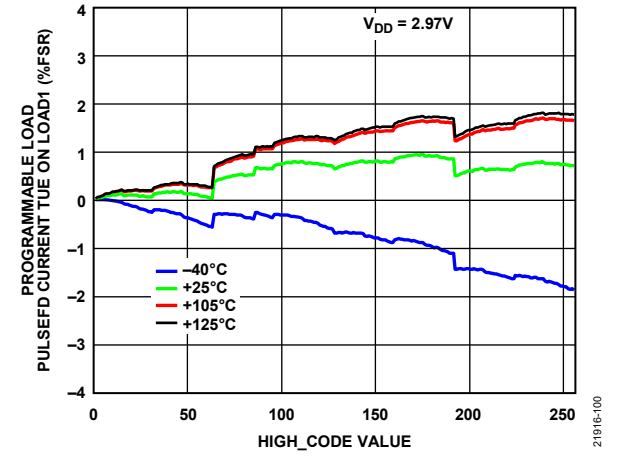


Figure 8. Programmable Load Pulsed Current TUE on LOAD1 vs. HIGH_CODE Value over Temperature

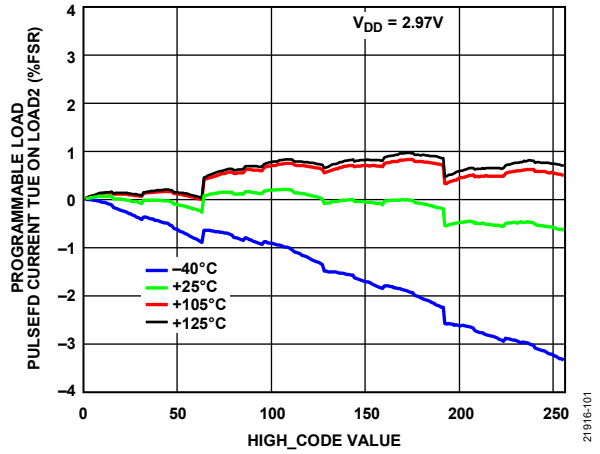


Figure 9. Programmable Load Pulse Current TUE on LOAD2 vs. HIGH_CODE Value over Temperature

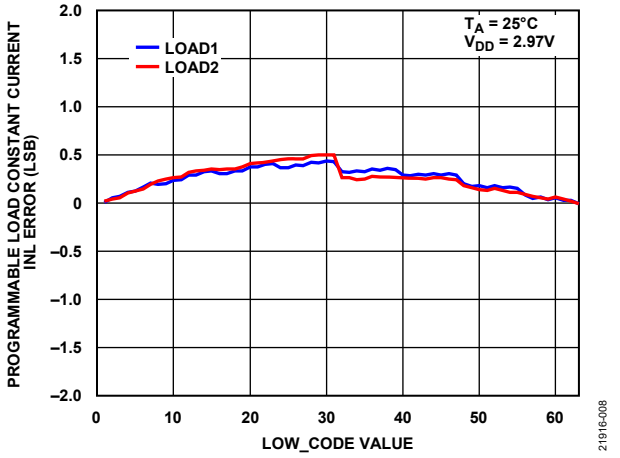


Figure 10. Programmable Load Constant Current INL Error vs. LOW_CODE Value

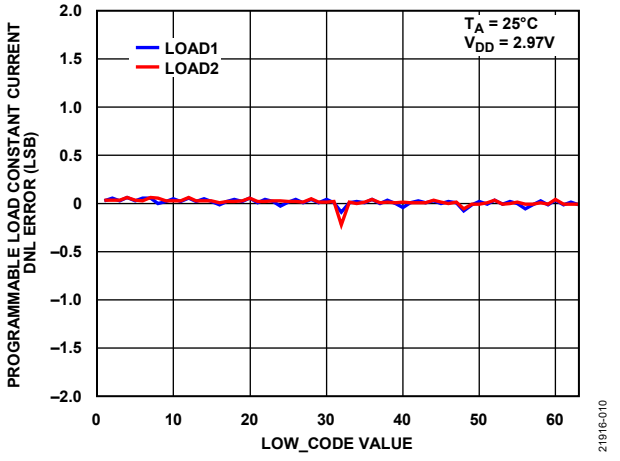


Figure 11. Programmable Load Constant Current DNL Error vs. LOW_CODE Value

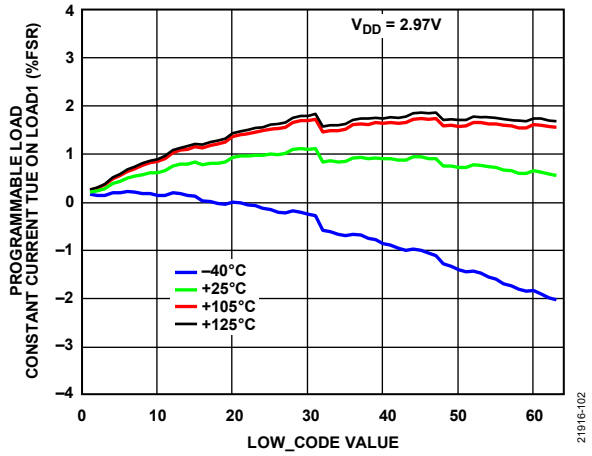


Figure 12. Programmable Load Constant Current TUE on LOAD1 vs. LOW_CODE Value over Temperature

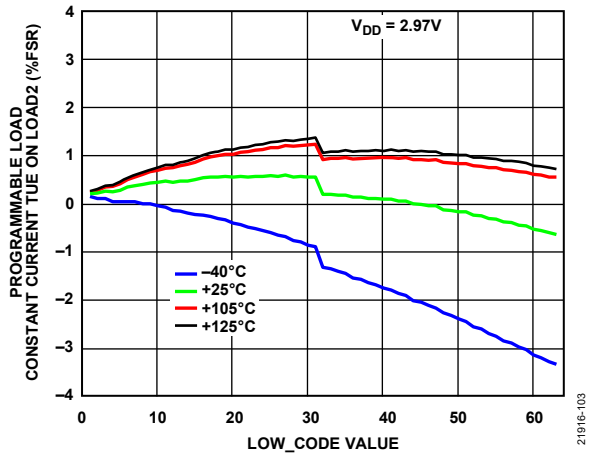


Figure 13. Programmable Load Constant Current TUE on LOAD2 vs. LOW_CODE Value over Temperature

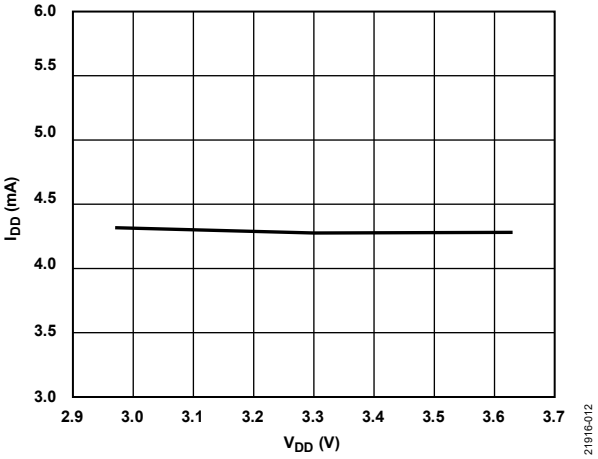


Figure 14. I_{DD} vs. V_{DD}

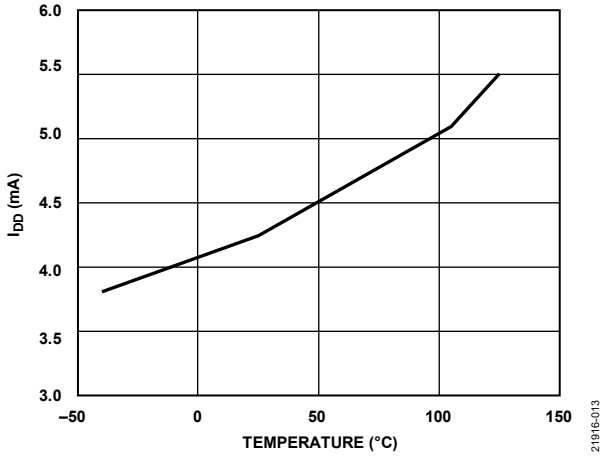


Figure 15. I_{DD} vs. Temperature

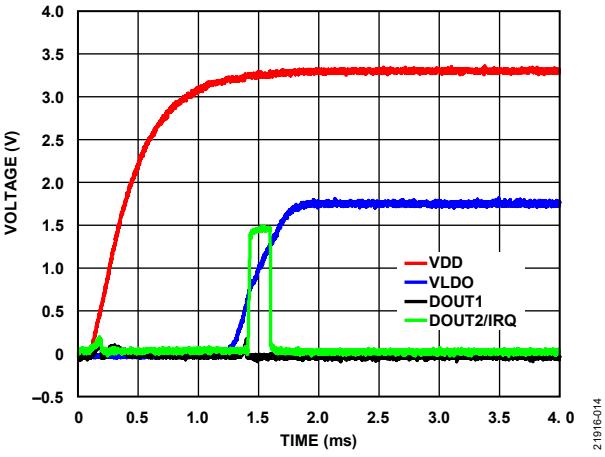


Figure 16. Power-Up of Nonisolated Side (VDD, VLDO, DOUT1, and DOUT2/IRQ Pins)

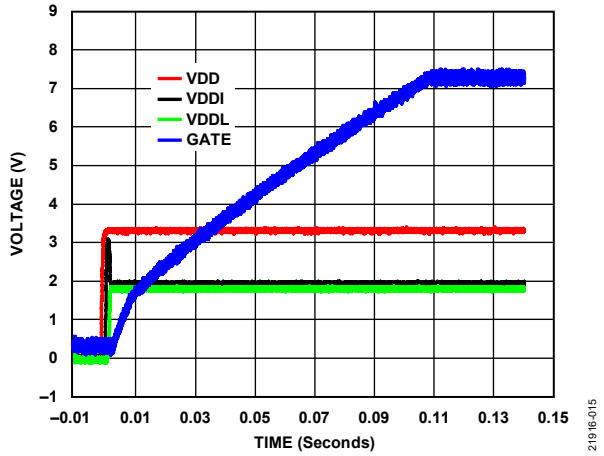


Figure 17. Power-Up of Isolated Side (VDDI, VDDL, and GATE Pins) when VDD Pin is Supplied on Nonisolated Side

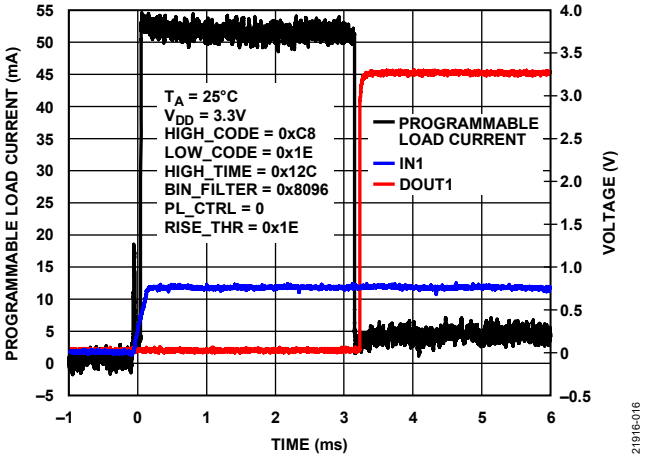


Figure 18. Typical Input, Digital Output, and Programmable Load Current Signals (IN1, DOUT1, and Programmable Load Current on Channel 1) in Low Idle Mode

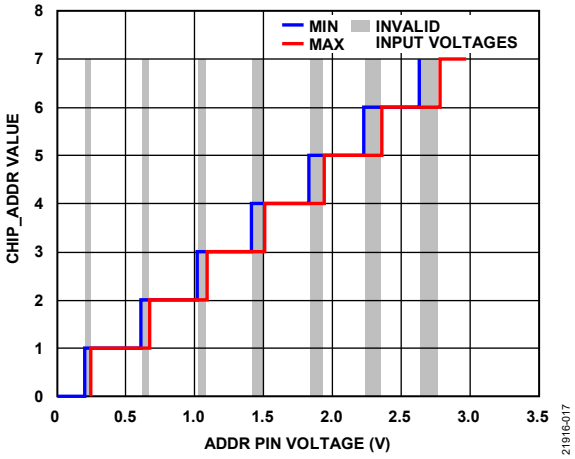


Figure 21. Decoded SPI Address (CHIP_ADDR) Value vs. ADDR Pin Voltage

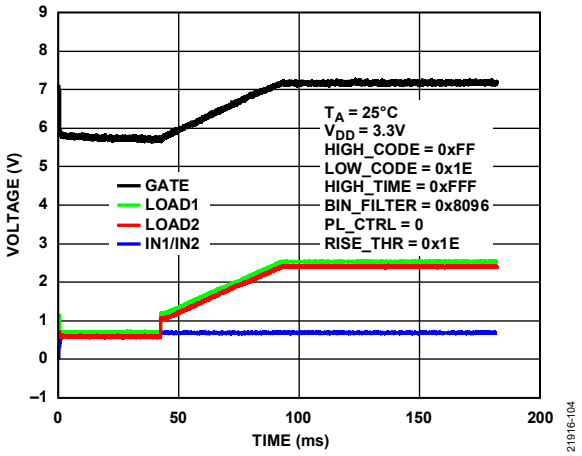


Figure 19. Typical Input, Gate, LOAD1, and LOAD2 Signals when Both External FETs Conducting (IN1 = IN2, Gate, LOAD1, LOAD2)

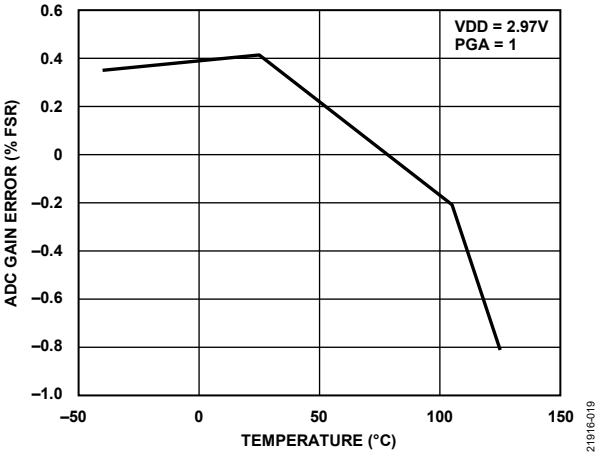


Figure 22. ADC Gain Error vs. Temperature

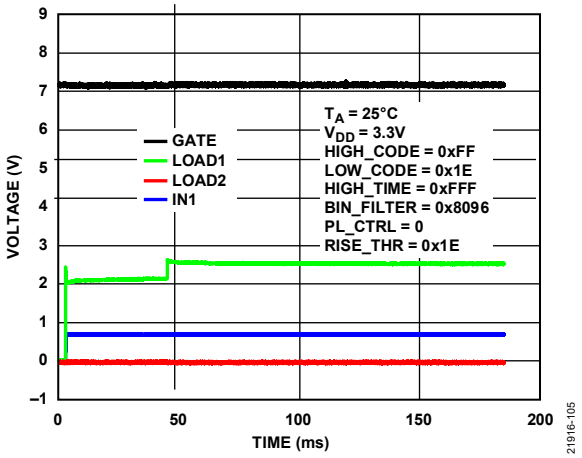


Figure 20. Typical Input, Gate, LOAD1, and LOAD2 Signals when the External FET on Channel 1-Conducting and Channel 2 Input Floating (IN1, Gate, LOAD1, LOAD2)

TEST CIRCUIT

The typical ADE1202 application circuit is shown in Figure 23.

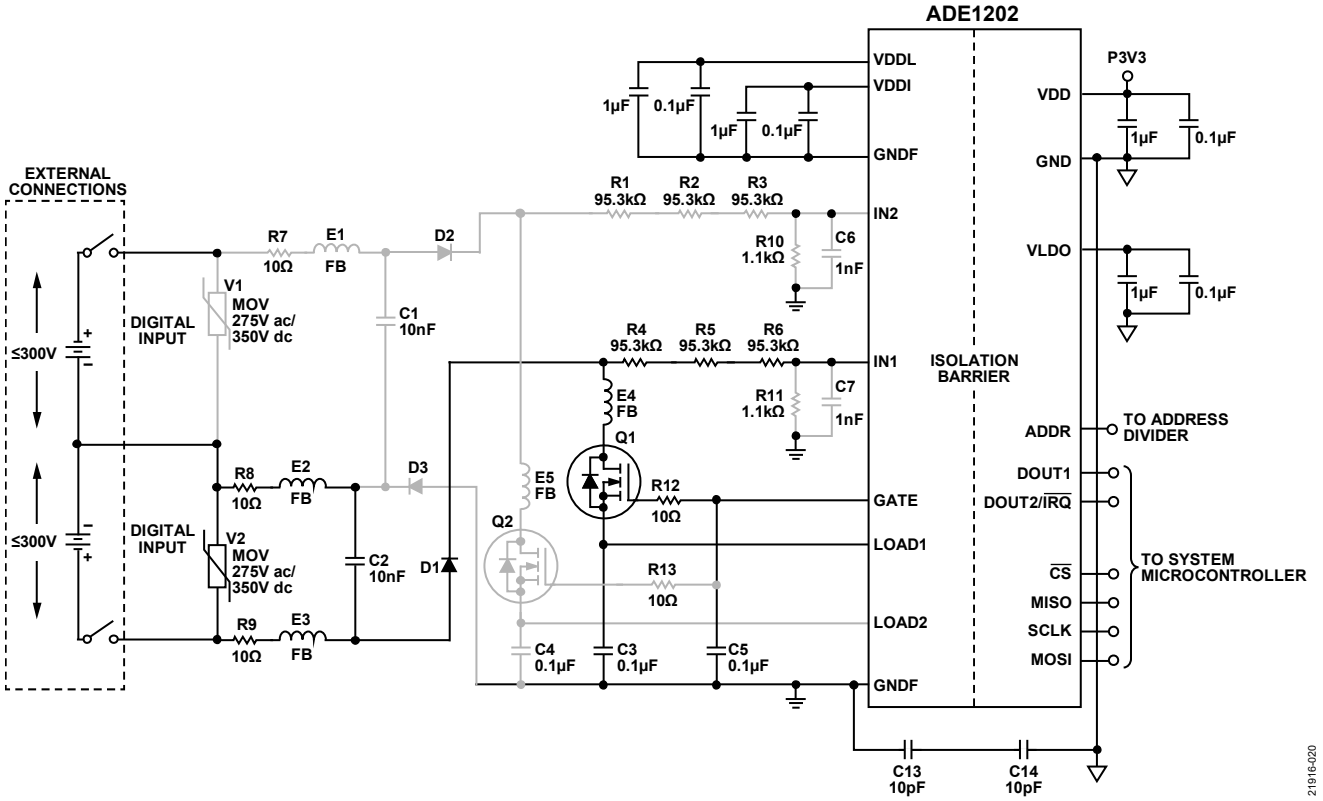


Figure 23. ADE1202 Typical Application Circuit

THEORY OF OPERATION

The ADE1202 is a dual channel, configurable, isolated digital input monitor designed for energy transmission and distribution applications. The ADE1202 contains an isolated and a nonisolated side (see Figure 24).

Only a single 3.3 V supply is required to power the ADE1202. The isolated side (the VDDI pin and GNDF pin) is supplied from an internal, isolated dc-to-dc converter, which is generated from the VDD pin and GND pin on the nonisolated side. The *iso*Power technology eliminates the need for an external, isolated power supply.

The isolated side of the device contains a PGA, an SAR ADC, a programmable load, and a gate drive.

Digital isolators allow the isolated side to communicate with the nonisolated side.

The nonisolated side signal conditions the ADC data coming from the isolated side and creates the DOUT1 and DOUT2 digital outputs. The digital outputs reflect the status of the IN1 and IN2 digital inputs from the isolated side.

The SPI is used to initialize the ADE1202 and can be used to monitor status and ADC waveforms during operation.

POWER SUPPLY AND CONDITIONING

VDD, VLDO, and GND Pins

Connect the VDD pin to a 3.3 V logic level supply. Decouple these pins to the GND pin with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations on how to make these connections.

GNDF Pins

The GNDF pins are used to reference the high voltage side circuits after the isolation barrier. The GNDF pin located at Pin 1 is used to provide a return path for current from the internal programmable load. The GNDF pin located at Pin 10 is used as a reference for internal, isolated power supply and the LDO regulator. Both Pin 1 and Pin 10 are required to be connected to the high voltage ground plane on the PCB. The detailed grounding method is described in the Layout Guidelines section.

VDDI and VDDL Supplies

The VDDI pin is the 2.0 V, isolated side power supply output, and the VDDL pin is the 1.8 V output of the analog LDO regulator. Decouple these pins to GNDF (Pin 10) with the recommended capacitors shown in Table 16, and see the Layout Guidelines section for recommendations.

Note that no external component can be supplied from the VDDI and GNDF isolated power supply outputs.

Power-Up

At power-up, the following steps must be taken by the host controller managing a system formed by one or multiple ADE1202 devices:

1. Supply 3.3 V to the VDD pin. The dc-to-dc converter powers up and supplies the isolated side of the ADE1202. The full device becomes functional. See Table 3 for the power-up time.
2. To determine when the ADE1202 devices are ready to accept commands, read the INT_STATUS register of each device until Bit 14 (RSTDONE) is set to 1.
3. Use the SPI to initialize the configuration registers (BIN_FILTER, PL_EN, and PGA_GAIN) of each ADE1202.
4. Write 0xADE1 to the LOCK register to complete the configuration process.

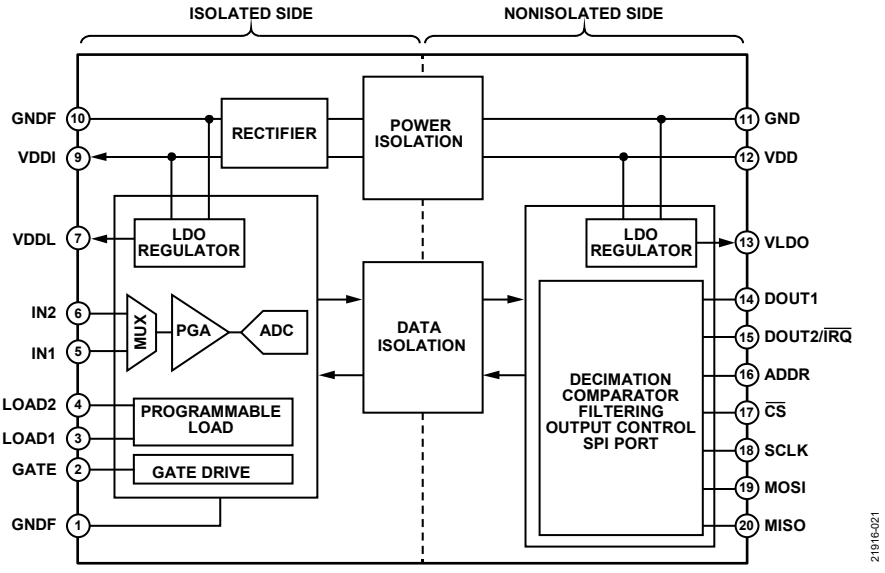


Figure 24. ADE1202 Nonisolated and Isolated Sides

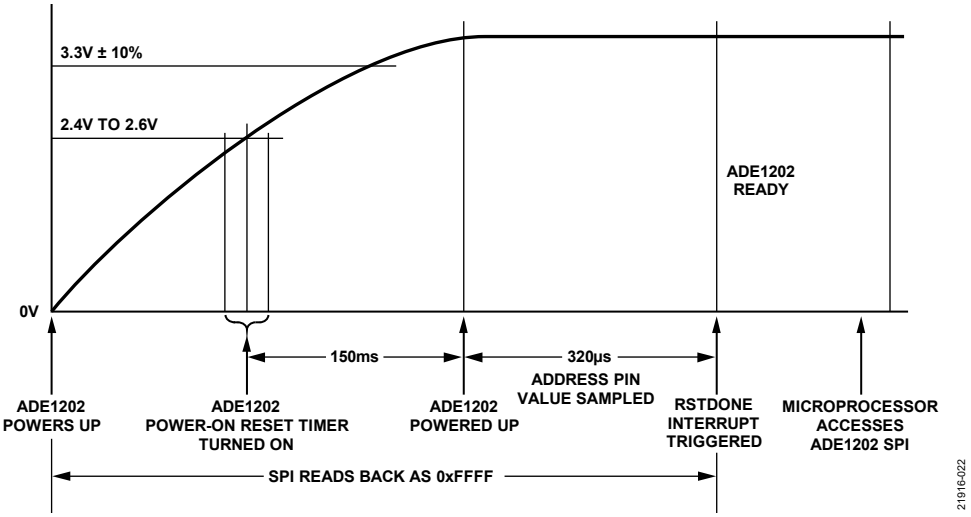


Figure 25. Power-Up Procedure for ADE1202 System

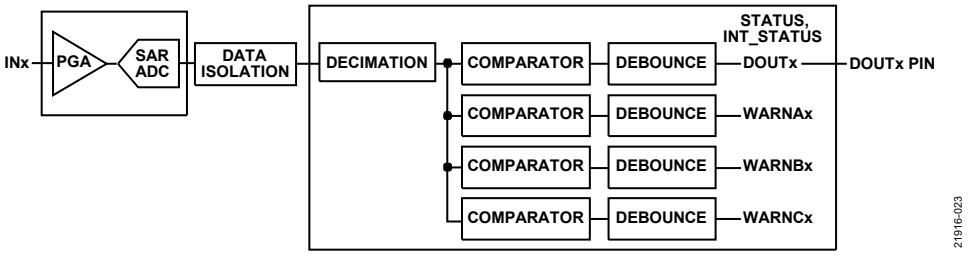


Figure 26. Digital Input Signal Path

DIGITAL INPUTS SIGNAL PATH

A typical ADE1202 application circuit is shown in Figure 23, which includes external scaling using a voltage divider. The acceptable input voltage between the INx and GNDF pins is given in Table 1.

Using the application circuit shown in Figure 23, ac input signals are half wave rectified, as shown in Figure 23, and require 10 ms + pickup time.

Figure 26 shows a detailed view of the digital signal conditioning done within the ADE1202 IC to generate a DOUTx digital output signal based on the input measured on the INx pins.

The following sections describe the functionality of each circuit in detail.

PGA

The PGA stage allows four scaling factors, as shown in Table 14. The input voltage range is the same as the INx input voltage range (V_{IN} in Table 1 and Table 14). To configure the gain over the SPI, write to the PGA_GAIN register (Address 0x201), Bits[1:0] (PGA_GAIN). It is recommended to choose the gain that maximizes the range of the internal ADC, as shown in Table 14, without setting the system thresholds outside the range of the PGA.

By default, the PGA_GAIN bits are cleared to 00, which means the PGA is set to 1.

Table 14. PGA Gain Settings

V_{IN}	PGA	PGA_GAIN Register, Bits[1:0]
1.25	1×	00
0.625	2×	01
0.25	5×	10
0.125	10×	11

SAR ADC

After the PGA stage, the ADE1202 SAR ADC produces 8-bit outputs, as shown in Figure 26. The ADE1202 has two multiplexed channels that share one ADC. The ADC samples at 100 kSPS and each INx channels is sampled at 50 kSPS. The digitized data is then passed through the isolation barrier.

To get an indication of when new ADC samples are ready, configure the DOUT2/$\overline{\text{IRQ}}$ pin as an interrupt by setting the IRQ_PIN_MODE bit in the CTRL register, and write 0x8000 to the MASK register. The DOUT2/$\overline{\text{IRQ}}$ pin goes high for 1 µs and then low for 9 µs at a rate of 100 kSPS, indicating when new ADC samples are ready. When reading ADC samples, Bit 15 in the MASK register, DREADY, must be the only interrupt enabled so that MASK = 0x8000.

Decimation

The data from the ADC is passed through a decimator. The decimation filter averages N samples and then decimates by N, where N is 2, 4, or 8, as configured in the DECRATE bits (Bits[2:1]) in the BIN_CTRL register (see Table 15). The decimation filter topology is shown in Figure 27. To enable the decimation, set Bit 0 (DECIMATE) to 1 in the BIN_CTRL register. By default, the decimator is disabled and the data from the ADC bypasses the decimator.

Table 15. Decimation Settings

DECRATE Bit Setting	Number of Samples
00	Bypass the decimator
01	2
10	4
11	8

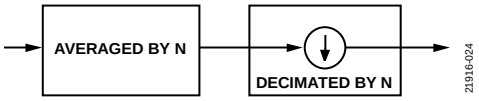


Figure 27. Decimation Filter Topology

Digital Datapaths

Four datapaths process the data coming out of the decimator, including comparators and debounce filtering.

One datapath, DOUTx, is capable of driving the DOUTx output, as shown in Figure 26. The output can also be read over the SPI.

Three additional datapaths, WARNAx, WARNBx, and WARNCx are provided for the user to configure warnings. The output of the warning datapaths can be read over the SPI.

Both digital input channels, IN1 and IN2, share the same digital datapath settings.

Set Bit 15 of the BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER registers to enable the comparator and debounce filters.

Comparator Function

Each comparator includes a high threshold level and a low threshold level. The thresholds are programmable between 0x00 and 0xFF. An INx pin voltage of 1.25 V/PGA translates to 0xFF. To calculate the threshold register value based on the desired threshold voltage and input signal level, use the following equation:

$$THR = (THRESHOLD/(1.25/PGA)) \times 255 \quad (1)$$

where:
THR is the value that is written in the BIN_THR, WARNA_THR, WARNB_THR, and WARNC_THR control registers.
THRESHOLD is the desired threshold level expressed in V.
PGA is the PGA gain selected by the PGA_GAIN register.

The BIN_THR register contains the configuration used for the DOUT1 and DOUT2 datapaths, which can be output on the DOUT1 pin and DOUT2 pin.

The WARNA_THR, WARNB_THR, and WARNC_THR registers contain the configuration for the warning channels.

Each comparator has four configurable modes: hysteretic mode, midrange mode, greater than (GT) mode, and lesser than (LT) mode. They are selected by the BIN_MODE, WARNA_MODE, WARNB_MODE, and WARNC_MODE bits in the BIN_CTRL register. After reset, the DOUT1 and DOUT2 channels are in hysteretic mode, the WARNAx channel is in GT mode, the WARNBx channel is in midrange mode, and the WARNCx channel is in LT mode.

Comparator in Hysteretic Output Mode

In hysteretic output mode, when the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. The behavior of the comparator in the hysteretic output mode is shown in Figure 28.

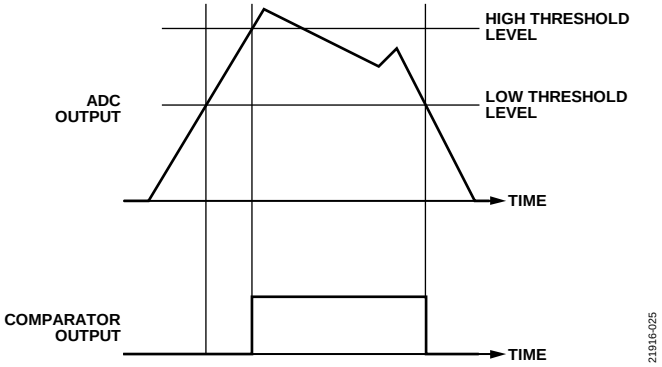


Figure 28. Comparator Behavior in Hysteretic Output Mode

Comparator in Midrange Output Mode

In midrange output mode, when the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. The output is set low when the ADC output drops below the low threshold level or goes above the high threshold level. The behavior of the comparator in the midrange output mode is shown in Figure 29.

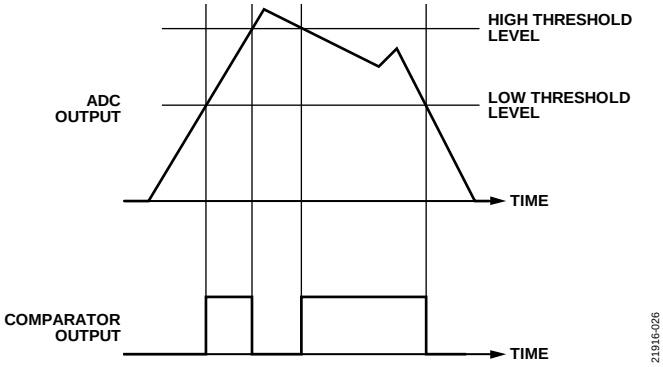


Figure 29. Comparator Behavior in Midrange Output Mode

Comparator in GT Mode

In GT mode, when the ADC output is greater than the high threshold level, the comparator output is set high. The comparator output is set low when the ADC output drops below the high threshold level. The behavior of the comparator in GT output mode is shown in Figure 30.

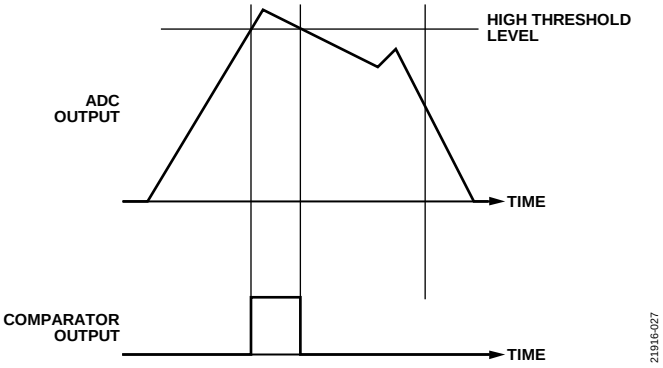


Figure 30. Comparator Behavior in GT Output Mode

Comparator in LT Mode

In LT mode, when the ADC output is lower than or equal to the high threshold level, the comparator output is set high. The comparator output is set low when the ADC output is greater than the high threshold level. The behavior of the comparator in LT output mode is shown in Figure 31.

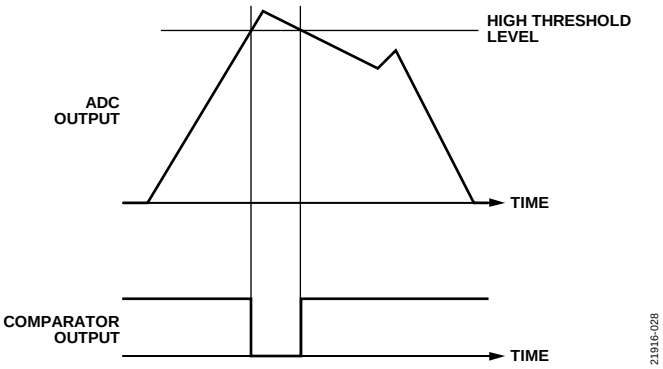


Figure 31. Comparator Behavior in LT Output Mode

Debounce Function

A debounce filter follows the comparator in each datapath.

Each debounce filter consists of a counter that increments every 20 µs. The maximum debounce time is 163.82 ms. A filter length of 0 means the debounce filter is bypassed. To calculate the filter length, use the following equation:

Filter Length = (*Debounce Time*/*Channel Update*)

where:
Filter Length is the value that is written in the BIN_FILTER_VAL, WARNA_FILTER_VAL, WARNB_FILTER_VAL, and WARNC_FILTER_VAL bit fields.
Debounce Time is the desired length of the filter expressed in µs.
Channel Update is 20 µs.

The debounce filter can function in two modes, managed by Bit 14 of the BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER registers. If Bit 14 is 0 (the default value) the filter is in up/clear mode. If Bit 14 is 1, the filter is in up/down mode.

Debounce Function Up/Clear Mode

In up/clear mode, the filter counter increments while the comparator output is high until the counter reaches the filter length. If the comparator output goes low before the filter length has been reached, the counter is cleared.

When the filter length has been reached, the filter output goes high. The counter stops incrementing when the comparator output is high. The counter is decremented when the comparator output goes low. When the counter decrements to 0, the filter output goes low. If the comparator output goes from low to high before the counter decrements to 0, the counter is reset to the filter length.

Debounce Function Up/Down Mode

In up/down mode, the filter counter increments while the comparator output is high until the counter reaches the filter length. If the comparator output is low, the counter is decremented.

When the filter length has been reached, the filter output goes high. The counter stops incrementing when the comparator output is high. When the comparator output is low, the counter is decremented. When the counter decrements to 0, the filter output goes low.

See Figure 32 for an example of the debounce filter working in up/down mode and up/clear mode.

The output of the debounce filter can be read through the SPI in the corresponding DOUTx, WARNAx, WARNBx, and WARNCx bits in the STATUS register, and the DOUT1 filter output represents the status for the IN1 filter output, and the DOUT2 filter output represents the status of the DOUT2 debounce filter output.

The status of the DOUT1 and DOUT2 filter outputs is reflected on the DOUT1 pin and the DOUT2/$\overline{\text{IRQ}}$ pin based on the setting of the IRQ_PIN_MODE bit (Bit 2) in the CTRL register. The debounce filter outputs can be configured to trigger an interrupt on the DOUT2/$\overline{\text{IRQ}}$ pin (see the Interrupt section).

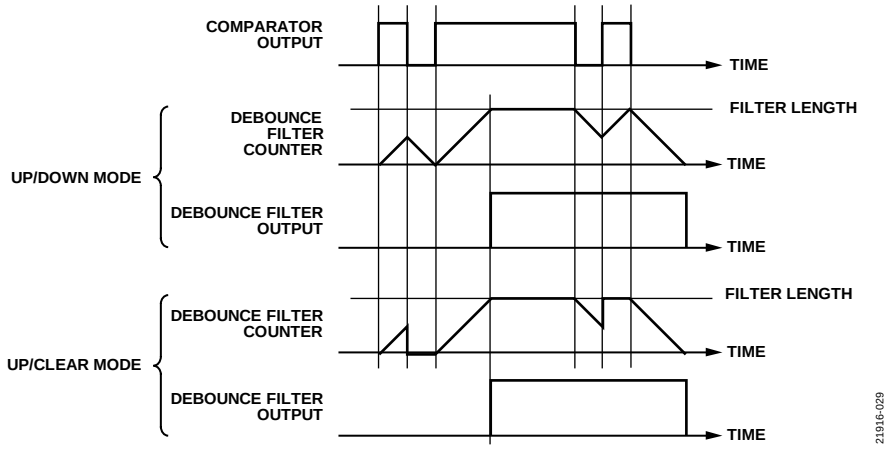


Figure 32. Debounce Filter Function Example

INVALID MODE

The register protection feature must be disabled when configuring the ADE1202 (see the Protecting the Integrity of Configuration Registers section). During this time, the state of the DOUT1 pin and DOUT2 pin does not reflect the state of the inputs on the IN1 pin and IN2 pin, and the IC is in invalid mode. The IC remains in this mode until the register protection is enabled.

During invalid mode, the ADE1202 output on the DOUT1 pin and DOUT2 pin is set based on Bits[5:4] (INVALID_MODE) and Bit 3 (FORCEVAL) of the BIN_CTRL register.

If the INVALID_MODE bits are equal to 00, the DOUT1 and DOUT2 filter outputs are set to the value configured in the FORCEVAL bit in the BIN_CTRL register. If the bits are equal to 01, the DOUT1 and DOUT2 filter outputs are set to the DOUTx output from the digital datapath. If the bits are equal to 10, the DOUT1 and DOUT2 filter outputs toggle the value they had upon entering invalid mode. If the bits are equal to 11, the DOUT1 and DOUT2 filter outputs hold the current value.

PROGRAMMABLE LOAD CURRENT

The ADE1202 programmable load current block diagram is shown in Figure 33. The input impedance of the programmable load is given in Table 1. When the programmable load is disabled with the PL_EN register, Bit 15 and Bit 14 = 00, and the external FET is conducting, the load sinks ~100 µA.

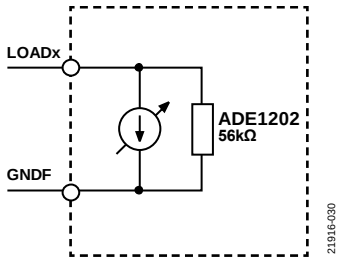


Figure 33. Programmable Load Current Block Diagram

A high voltage digital input is presented to the ADE1202 application circuit, as shown in Figure 23. When the digital input switches on to a high voltage state, the ADE1202 injects a pulsed current load for a user defined period of time based on the PL_HIGH_TIME register, and then switches to a constant current. The pulsed current is sometimes called a wetting current and removes oxidation from the digital input contacts, as well as minimizes the effects of surge and electrical fast transients.

To calculate the value to write to the HIGH_CODE bits (Bits[7:0]) of the PL_HIGH_CODE register to configure the pulsed current, use the following equation:

$$HIGH\_CODE = Pulsed\ Current/0.2 \quad (2)$$

where *Pulsed Current* is the desired current level expressed in mA. The resolution of the pulsed current is 0.2 mA per LSB. The maximum current is $(2^8 - 1) \times 0.2 = 51$ mA.

The recommended range of the pulsed current is between 20 mA and 50 mA, and HIGH_CODE = 100 decimal to 250 decimal. The minimum current is 0.2 mA and HIGH_CODE = 1.

The pulsed current is applied for a time period set in Bits[11:0] (HIGH_TIME) in the PL_HIGH_TIME register.

To determine the value to write to the HIGH_TIME bit field based on the desired period of the pulse, use the following equation:

$$HIGH\_TIME = Pulsed\ Current\ Period/10 \quad (3)$$

where *Pulsed Current Period* is the desired time period expressed in µs. The resolution of the pulsed current period is 10 µs. The maximum period is $(2^{12} - 1) \times 10$ (µs) = 40.95 ms.

After the pulsed current period, the programmable load switches to a constant current level set in the LOW_CODE bits (PL_LOW_CODE register, Bits[5:0]). To determine the value to write to the LOW_CODE bit field, use the following equation:

$$LOW\_CODE = Constant\ Current/0.1 \quad (4)$$

where:
Constant Current is the desired current level expressed in mA. The resolution of the constant current is 0.1 mA per LSB.

The maximum current that can be set is $(2^6 - 1) \times 0.1 = 6.3$ mA.

The user can select between low idle mode and high idle mode to determine when the programmable pulse current is activated.

Low Idle Mode

The user can select the ADC input code where the programmable load pulse current turns on in low idle mode, where PL_MODE = 0 in the PL_CTRL register. This is the default mode of operation.

Figure 34 shows the programmable load current behavior in low idle mode. When the digital input changes from low to high, the pulsed current is generated after the ADC output reaches a rising edge threshold set in the RISE_THR bits of the PL_RISE_THR register, Bits[7:0].

Note that the DOUTx pins must be low for the programmable load pulsed current to be generated. To ensure that a pulsed current is generated, BIN_FILTER_VAL must be ≥3 and RISE_THR must be <BIN_HI_THR.

High Idle Mode

To enable high idle mode, set the PL_MODE bit to 1 in the PL_CTRL register so the programmable load pulse current conducts as soon as the input voltage over the FET is sufficient (a few hundred mV). Figure 35 shows the programmable load current behavior in high idle mode.

Note that the DOUTx pins must be low for the programmable load pulsed current to be generated. To ensure that a pulsed current is generated, BIN_FILTER_VAL must be ≥3.

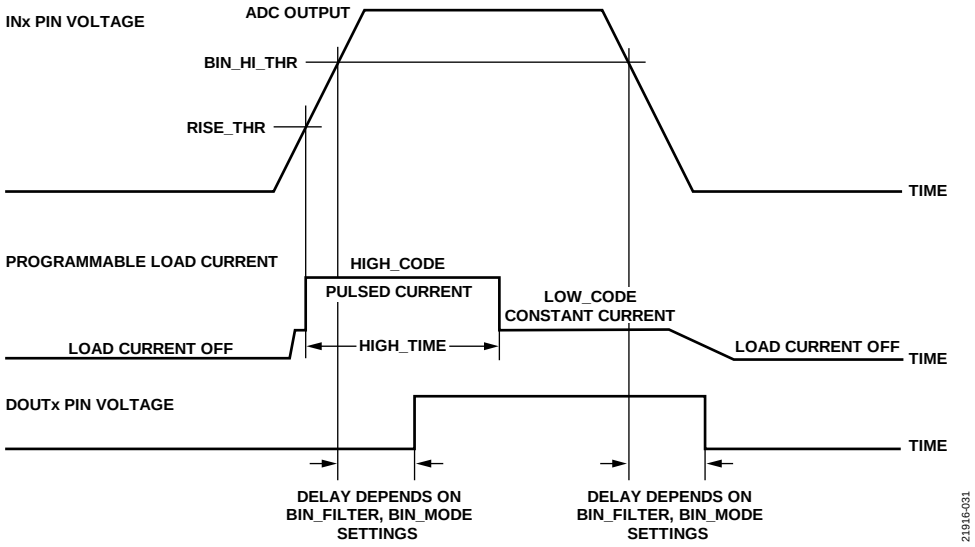


Figure 34. Programmable Load Current Waveform in Low Idle Mode

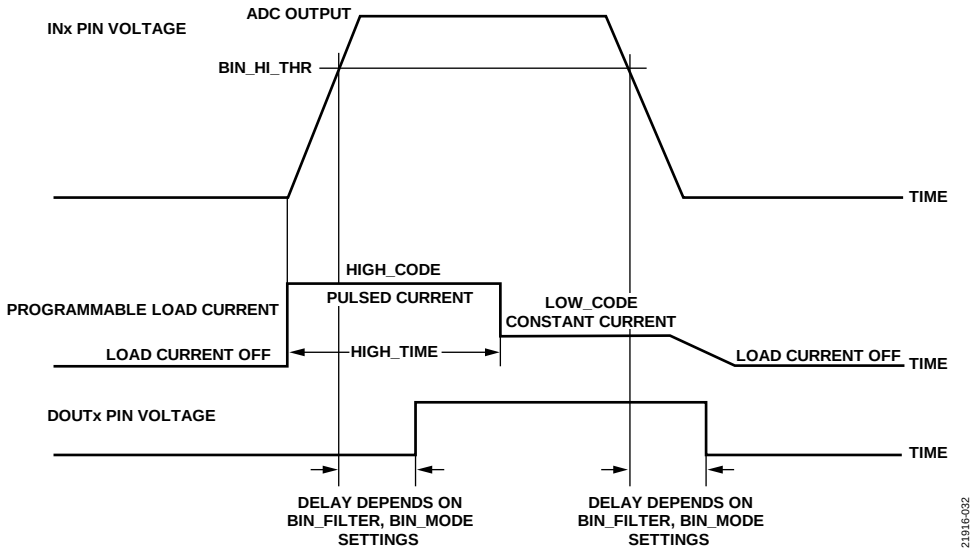


Figure 35. Programmable Load Current Waveform in High Idle Mode

EXTERNAL FET PROTECTION

The external FET protection function monitors the approximate FET energy based on the programmed load current and measured digital input voltage over time. When the accumulation reaches a user programmed limit threshold that is a function of the programmed current load, the pulsed current is turned off for a cool down period.

Threshold Calculation

Calculate the expected ADC code for a given input, ADCx, with the following equation and round to the nearest whole number:

$$ADCx = ((Voltage \times Gain \times Full\ Scale\ ADC\ Codes)/(Voltage\ Divider \times Reference)) \quad (5)$$

where:
Voltage is the input voltage to the ADE1202 application circuit measured in V.
Gain is 1, 2, 5, or 10 according to the setting in the PGA_GAIN register.
Full Scale ADC Codes is the maximum code output by the ADC, which is 255.
*Voltage Divide*r is the application circuit voltage divider ratio.
Reference is the voltage reference value, typically 1.25 V, expressed in V.

Using the safe operating area for the external FET, a threshold, EGY_MTR_THR, can be calculated to prevent energy from the pulsed current from exceeding this threshold. To calculate the threshold, use the following equation:

$$EGY\_MTR\_THR = (SOA \times ADCx)/(Voltage \times Pulsed\ Current \times Rate \times 2^7) \quad (6)$$

where:
SOA is the energy that can be safely dissipated by the FET, expressed in J.
Pulsed Current is the pulsed current setting in the programmable load expressed in A.
Rate is the accumulation rate, 1/100 kHz = 10 µs, expressed in seconds (s).

The expected increase for each pulse is given by the following equation:

$$Single\ Pulse\ Increase = (ADCx \times Pulse\ Current\ Time)/(Rate \times 2^7) \quad (7)$$

When the ADC code is equal to 0xFF in a pulsed current state, the IN1 or IN2 input voltages may be greater than the ADC input voltage range, which can cause the external FET to reach the limit of the safe operating area more quickly. To model this effect, configure the OV_SCALE bits in the EGY_MTR_CTRL register to set an overvoltage scaling factor to speed up the FET energy monitoring accumulation. In this condition, the value of each pulse can be calculated with the following equation:

$$(Overvoltage\ Factor \times Full\ Scale\ ADC\ Codes \times Pulse\ Current\ Time)/(Rate \times 2^7) \quad (8)$$

where *Overvoltage Factor* is configured in the OV_SCALE bits in the EGY_MTR_CTRL register to allow a 1, 4, 8, or 16 scaling factor.

Cool Down Configuration

When the monitored FET energy reaches the user programmed energy limit threshold, the pulsed current is turned off for a cool down period. The cool down period, expressed in seconds, is set in Bits[3:0] (COOLDOWN_SEC) in the EGY_MTR_CTRL register (Address 0x015). If the COOLDOWN_SEC bits are cleared to 0, the cool down functionality is disabled, the load current is not turned off, and the accumulator is forced to 0.

The external FET energy accumulator is decremented outside of the pulsed current period by a quantity set in the COOLDOWN_DECR bits (EGY_MTR_CTRL register, Bits[15:8]). The decrement frequency is set in the COOLDOWN_TIMESTEP bits (EGY_MTR_CTRL register, Bits[5:4]). The frequency can be 10 µs (Bits[5:4] = 00), 20 µs (Bits[5:4] = 01), 40 µs (Bits[5:4] = 10), or 80 µs (Bits[5:4] = 11).

When the ADE1202 is in the cool down period, the accumulator resets to 0. Each channel has a corresponding accumulator, EGY_MTR1 or EGY_MTR2, which allows cool down to be evaluated on each channel individually.

The external FET protection function mechanism is shown in Figure 36.

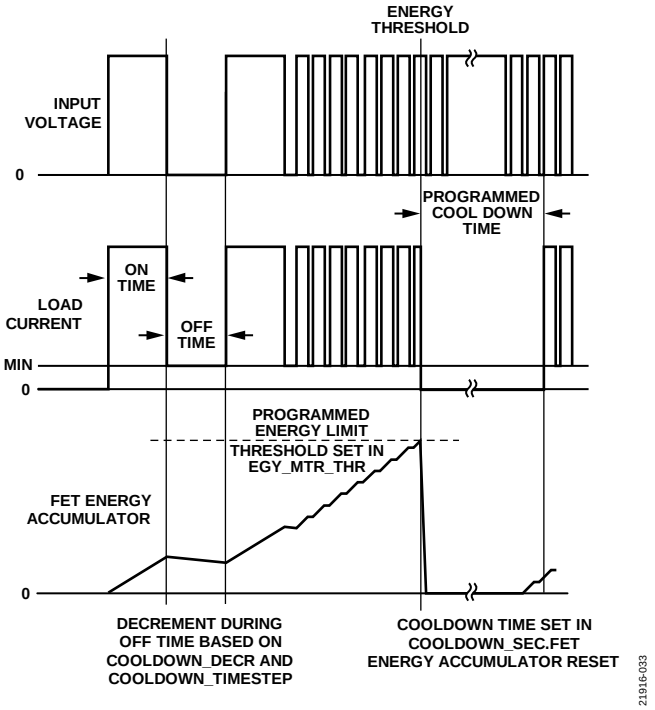


Figure 36. FET Protection Cool Down Feature

GATE DRIVE

The GATE pin is used to drive two external high voltage enhancement mode FETs, Q1 and Q2. After power-up, the GATE pin is biased at $V_{GATENOM}$ to allow Q1 and Q2 to conduct the constant current while protecting the LOADx pins, as shown in Figure 37. Two 10 Ω, external, gate current limiting resistors (R13 and R14), and a 0.1 µF gate capacitor (C5) are required for stability. Table 1 shows the nominal $V_{GATENOM}$ voltage (see Figure 37).

During a pulsed current, $V_{GATENOM}$ is regulated to reduce the voltage on the LOADx pins to minimize on-chip power consumption.

When two FETs are conducting, the corresponding LOADx pin for the FET with the larger gate source voltage (V_{GS}) is at 0.6 V and the other LOADx pin is at a higher voltage, as determined by FET mismatch.

When one FET is conducting, the corresponding LOADx pin is at 2.8 V, or as close as possible based on FET V_{GS}. The LOADx pin voltage is higher with one FET conducting to allow a fast response in case the other FET must turn on.

After a pulsed current period, the GATE voltage is regulated back to $V_{GATENOM}$. The ADE1202 is compatible with FETs with a maximum V_{GS} of 6 V. It is recommended to use the same FET for both channels, and FET to FET mismatch of up to 2 V is supported.

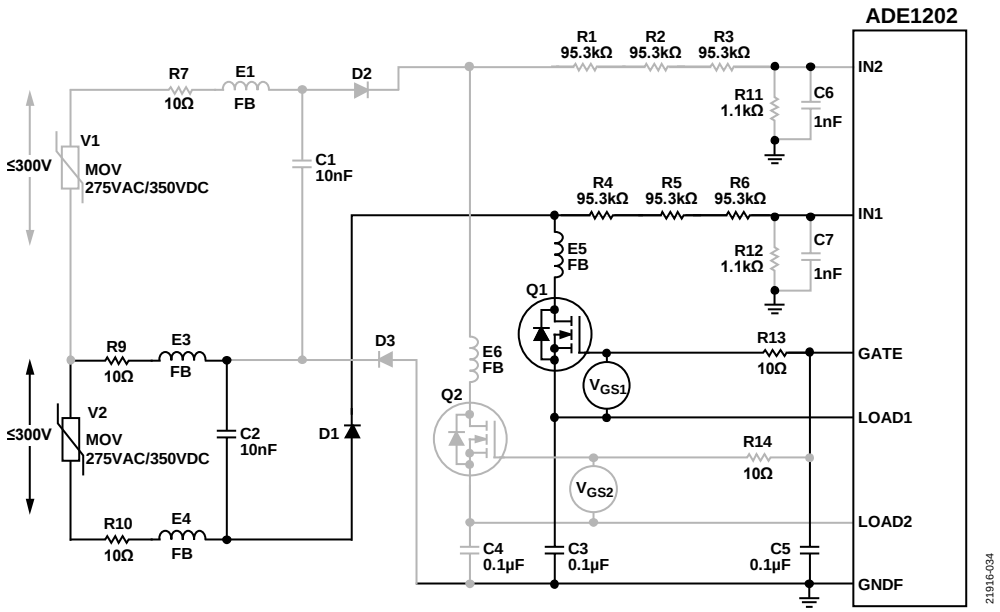


Figure 37. FET Gate Control

THERMAL SHUTDOWN

If the junction temperature of the isolated side exceeds the thermal shutdown value given in Table 1, the programmable load current is disabled. The TSD bit in the INT_STATUS register indicates if the device is in thermal shutdown condition. When the device cools down by the hysteresis value given in Table 1, the programmable load current is reenabled.

INTERRUPT

The interrupt pin, $\overline{\text{IRQ}}$, is multiplexed with the DOUT2/$\overline{\text{IRQ}}$ pin. Use Bit 2 (IRQ_PIN_MODE) in the CTRL register to select the functionality for this pin. If the IRQ_PIN_MODE bit is cleared to 0 (the default) the pin functionality is DOUT2. If the bit is set to 1, the pin functionality is $\overline{\text{IRQ}}$.

When the interrupt pin function, $\overline{\text{IRQ}}$, is selected, the DOUT2/$\overline{\text{IRQ}}$ output switches from being a push/pull output to an open-drain output.

The $\overline{\text{IRQ}}$ pin is managed by a 16-bit interrupt mask register, MASK. To enable an interrupt, the corresponding bit in the MASK register must be set to 1. To disable an interrupt, the bit must be cleared to 0.

INT_STATUS Register

When an interrupt is triggered, the $\overline{\text{IRQ}}$ pin goes low. To determine the source of the interrupt, read the INT_STATUS register to identify which bit(s) are set to 1. To clear the flag(s) in the INT_STATUS register, write to the INT_STATUS register with the corresponding bits set to 1. The $\overline{\text{IRQ}}$ pin remains low until the corresponding INT_STATUS flag is cleared.

By default, all interrupts are disabled with the exception of the RSTDONE interrupt. This interrupt cannot be disabled (masked).

During power-up or software reset, the DOUT2/$\overline{\text{IRQ}}$ pin defaults to DOUT2 functionality. When the power-up or software reset ends, Bit 14 (RSTDONE) in the INT_STATUS register is set to 1.

Note that Bit 15 (DREADY) in the MASK register functions differently than Bits[14:0]. See the SAR ADC section more information on the DREADY function.

STATUS Register

The STATUS register contains status flags that are updated in real time. When the condition related to a flag is triggered, the flag is set to 1. When the condition disappears, the flag is automatically cleared to 0.

The bits in the STATUS register are identical to the bits in the INT_STATUS register with one exception. Bit 14 is RSTBUSY in the STATUS register and RSTDONE in the INT_STATUS register. The RSTBUSY bit is 1 during reset and power-on and becomes 0 when the IC is ready to accept commands.

SPI PROTOCOL OVERVIEW

The compatible SPI consists of four pins: SCLK, MOSI, MISO, and $\overline{\text{CS}}$. The ADE1202 is always an SPI slave. The SPI is compatible with 16-bit read/write operations. The maximum serial clock frequency supported by this interface is 10 MHz.

The $\overline{\text{CS}}$ input pin is the chip select input. Drive the $\overline{\text{CS}}$ pin low for the entire data transfer operation. Bring the $\overline{\text{CS}}$ pin high during a data transfer operation to abort the transfer and place the serial bus in a high impedance state. A new transfer can be initiated by returning the $\overline{\text{CS}}$ pin to low.

Data shifts into the device at the MOSI pin on the falling edge of SCLK, and the ADE1202 samples the data on the rising edge of SCLK. Data shifts out of the ADE1202 at the MISO pin on the falling edge of SCLK, and the host controller samples the data on the rising edge of SCLK. The MSB of the word is shifted in and out first. MISO stays in high impedance when no data is transmitted from the ADE1202.

Figure 38 shows the connection between the ADE1202 SPI and a host controller with a master SPI.

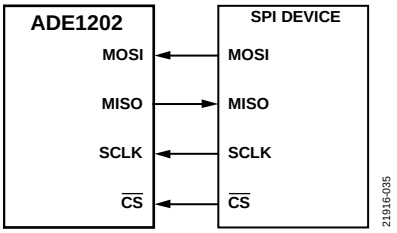


Figure 38. Connecting the SPI to an SPI Device

SPI ADE1202 Addressing

Up to eight ADE1202 devices can be accessed on the same SPI bus. A voltage ladder of up to seven equal resistors ranging from 1 kΩ to 10 kΩ values with 1% tolerance can be used (see Figure 40). With the ADDR pin connected to 3.3 V, the ADE1202 has the chip address of 7. With the ADDR pin connected to ground, the ADE1202 has the chip address of 0. The remaining six ADE1202 devices have the chip addresses in sequence based on the applied voltage of the potential divider. If multichip addressing is not used, connect the ADDR pin to ground.

The chip address is indicated in Bits[2:0] of the 16-bit command header.

Figure 39. SPI Header Word

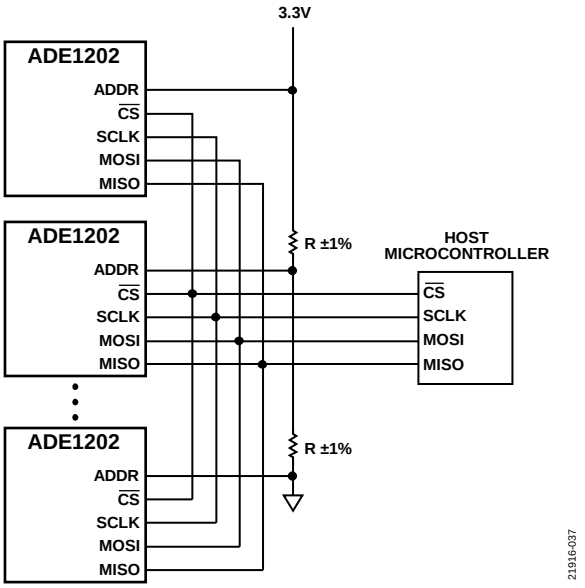


Figure 40. Multichip SPI Addressing Mode

SPI Write Operation

A write operation is initiated when the host controller sets the $\overline{CS}$ pin low and begins sending a 16-bit command word with the register address in Bits[14:4] and Bit 3 of the command header cleared to 0 (see Figure 41).

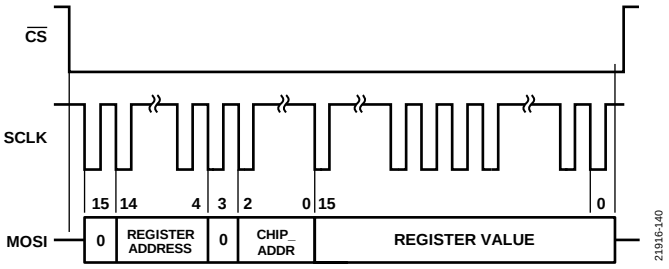


Figure 41. SPI Write Operation

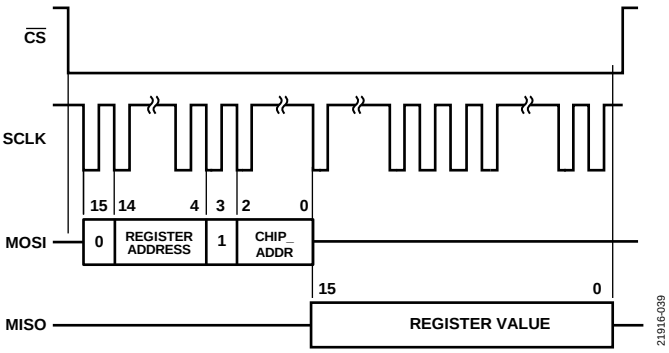


Figure 42. SPI Read Operation

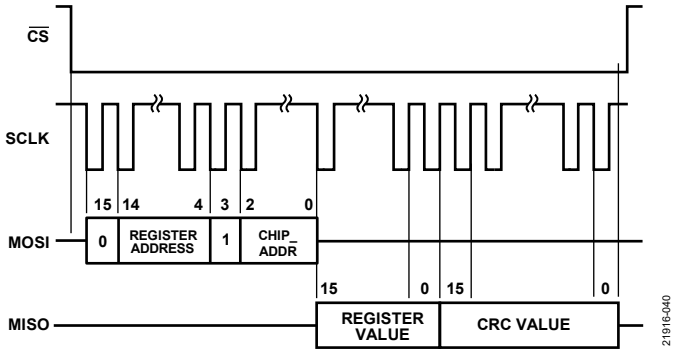


Figure 43. SPI Read Operation with Appended Cyclic Redundancy Check (CRC)

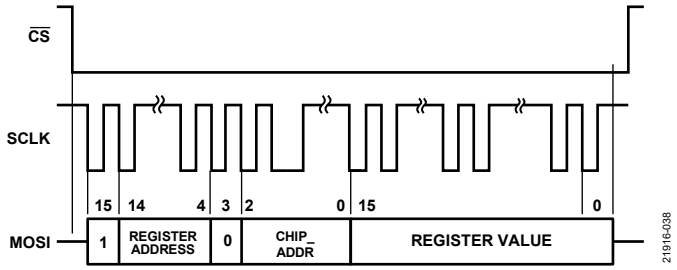


Figure 44. SPI Broadcast Write Operation

Each time a register is written, the register value must be verified by reading it back.

If multiple ADE1202 devices share the same SPI bus (as shown in Figure 38) and the same register in multiple chips must be initialized with an identical value, the broadcast write functionality is available. Set Bit 15 in the SPI header word to 1 to enable a broadcast write, as shown in Figure 44. Bits[2:0] (CHIP_ADDR) of the header word that indicate the chip address on the SPI bus are ignored during a broadcast write.

SPI Read Operation

The registers of the ADE1202 can be read one at a time following the protocol shown in Figure 42.

A read operation is initiated when the host controller sets the $\overline{CS}$ pin low and begins sending a 16-bit command word (see Figure 39). When the ADE1202 receives the last bit of the header word, the device begins to transmit the register contents on the MISO line when the next SCLK high to low transition occurs. The host controller samples the data on the low to high SCLK transition.

For an SPI read operation, Bit 3 of the command header must be set to 1 (see Figure 39).

To ensure the integrity of the SPI read operation, a 16-bit CRC (CRC-16) of the register value sent out on the MOSI pin can be included in the transaction. If enabled, the ADE1202 appends the CRC-16 value during the SPI read operation after the register value (see Figure 43).

If Bit 0 (SPI_CRC_APPEND_EN) in the CTRL register is cleared to 0 (the default value), no CRC value is appended during an SPI read operation. If the bit is set to 1, the CRC-16 value is appended to the register value read during the SPI read operation.

The CRC algorithm is based on the standard CRC-16-CCITT polynomial. The registers are introduced into a linear feedback shift register (LFSR)-based generator one byte at a time, most significant byte first, as shown in Figure 45. Each byte is then used with the MSB first.

Figure 46 shows how the LFSR is used for CRC calculation. The ADE1202 register forms Bits[a_{15}:a_0] used by the LFSR. Bit a_0 is Bit 15 of the register. Bit a_{15} is Bit 0 of the register.

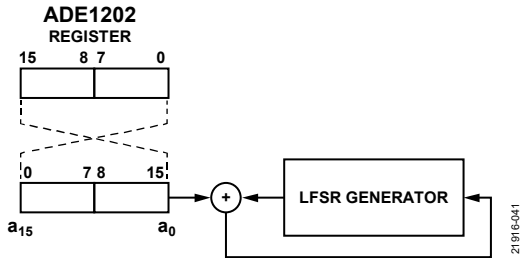


Figure 45. CRC Calculation

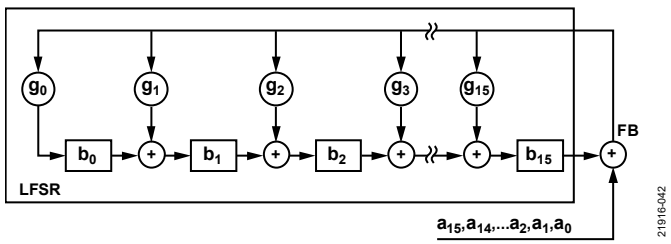


Figure 46. LFSR Generator Used for CRC Calculation

Bits $b_i(0) = 1$, where i = 0, 1, 2, … 15, the initial state of the bits that form the CRC. Bit b_0 is the LSB, and Bit b_{15} is the MSB.

The coefficients g_i, where i = 0, 1, 2, … 15, are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (9)$$

$$g_0 = g_5 = g_{12} = 1 \quad (10)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (11)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (12)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots 15 \quad (13)$$

Equation 11, Equation 12, and Equation 13 must be repeated for j = 1, 2, … 16. The value written into the SPI communication CRC contains Bit $b_i(16)$, where i = 0, 1, … 15.

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

Configuration registers are either user accessible registers (R/W registers listed in Table 17) or internal registers that are not user accessible.

On power-up, the user accessible configuration registers can be written without restriction.

When the registers are configured, write 0xADE1 to the LOCK register to send configuration information from the isolated side to the nonisolated side. This action also disables write access to the configuration registers from the SPI port to protect the integrity of the configuration.

When the protection is enabled, read back the LOCK register to ensure that Bit 0 (LOCK) was set to 1.

When the LOCK register is read, Bit 0 (LOCK) shows the protection status. If the LOCK bit is 0, the protection is disabled. If the LOCK bit is 1, the protection is enabled.

The lock function does not affect the ADDR_RELOAD bit, the LOCK register, and the INT_STATUS register, which can all be written when LOCK = 1.

To disable the register protection, write 0xADE0 to the LOCK register.

To change any configuration registers, disable the protection, change the value of the register, and then reenable the protection.

VERSION

The REVID bits (Bits[8:5]) in the CTRL register identify the version of the IC.

INSULATION WEAR OUT

The lifetime of insulation caused by wear out is determined by the isolation thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress because this value reflects isolation from the line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier, as shown in Equation 14. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 15. For insulation wear out with the polyimide materials used in the ADE1202, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (14)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (15)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 47 and the following equations.

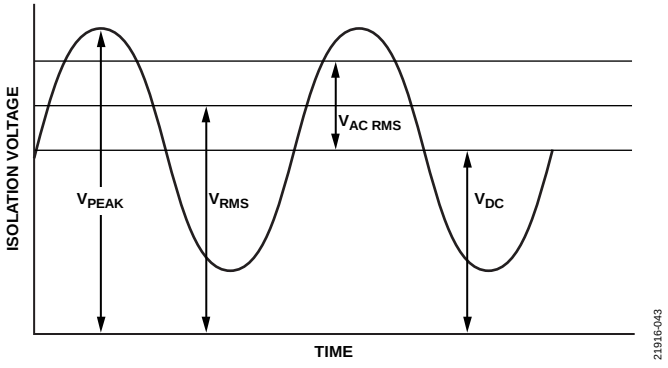


Figure 47. Critical Voltage Example

Calculate the working voltage across the barrier from Equation 16 with the following equations:

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (16)$$

$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (17)$$

In this example, V_{RMS} = 466 V.

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 18.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^{\ 2} - V_{DC}^{\ 2}} \quad (18)$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2} \quad (19)$$

In this example, $V_{AC\ RMS}$ = 240 V rms.

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 12 for the expected lifetime, is less than a 60 Hz sine wave, and is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 12 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

LAYOUT GUIDELINES

Figure 23 shows the schematic of the typical ADE1202 application circuit.

A 4-layer PCB is recommended for the application circuit. Figure 48 shows the recommended layout to interface two digital input channels given on P0 and P1 with one ADE1202.

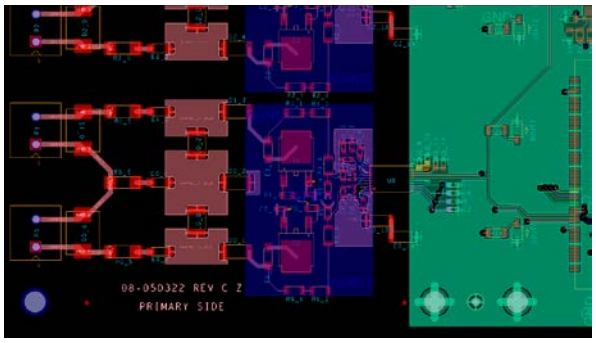


Figure 48. ADE1202 Circuit Board, Top Layer

Figure 49 shows a close up of the Figure 48 layout, focusing on the critical areas around the ADE1202.

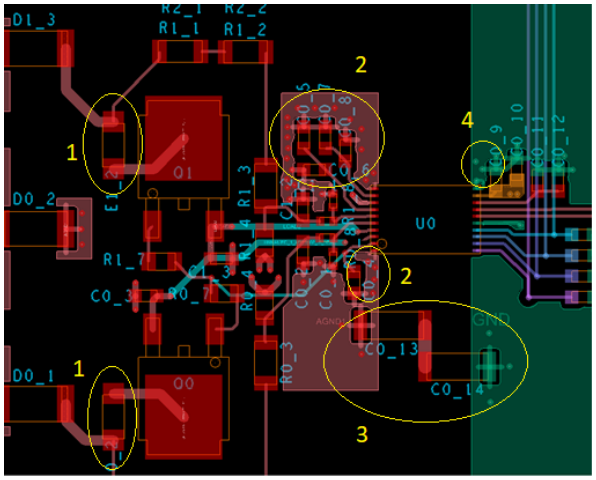


Figure 49. Close Up of the ADE1202 Support Circuitry

FERRITE BEAD

A ferrite bead is placed on the drain of each FET to prevent parasitics in the application circuit from resonating with the FET at high frequencies (hundreds of MHz).

Place a ferrite bead near the drain of each FET (see the yellow Circle 1 labels in Figure 49).

DECOUPLING AND GROUND PLANE CONNECTION

A low inductance path to the ground plane is required. It is recommended to use multiple vias to lower the inductance and provide multiple connections to the GNDF ground pins, Pin 1 and Pin 10.

When placing the decoupling capacitors, ensure that the smaller capacitor, 0.1 µF, is placed as close as possible to the VDDI pin and GNDF pin (Pin 10) to provide a low inductance from the pin to the capacitor, and from the capacitor to ground.

Figure 50 and Figure 51 show close ups of the recommended layout around the ADE1202 Pin 1 and Pin 10, which are indicated by the yellow Circle 2 labels in Figure 49.

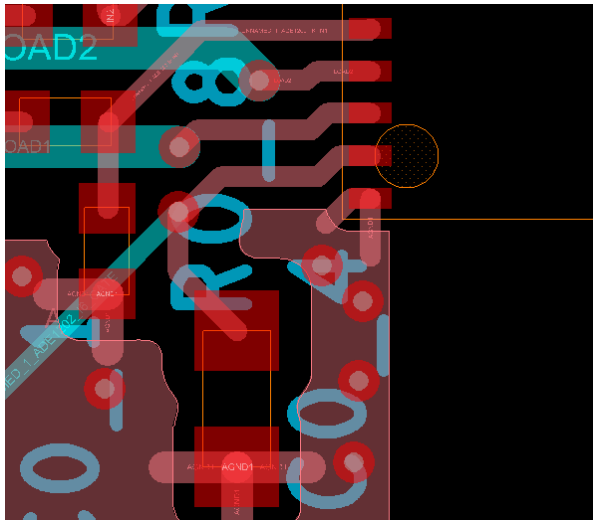


Figure 50. ADE1202 Pin 1 Close Up

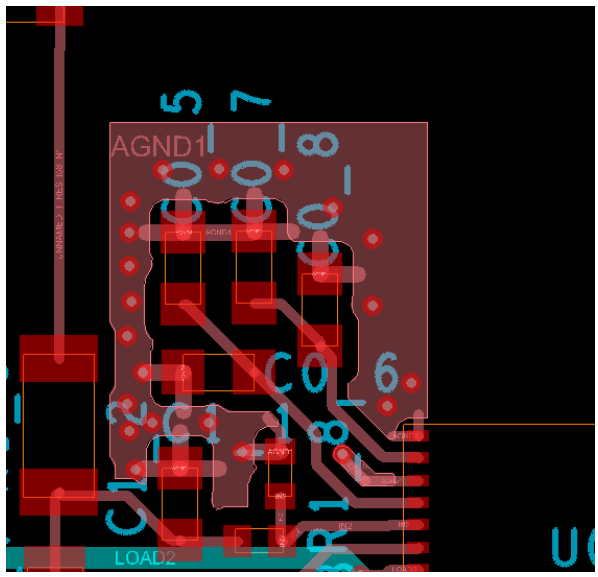


Figure 51. ADE1202 Pin 10 Close Up

Similar rules apply for decoupling on the isolated side for the GND and VDD supplies on Pin 11 and Pin 12 (see the yellow Circle 4 label in Figure 49).

ELECTOMAGNETIC INTERFACE (EMI) CAPACITOR

High voltage capacitors are recommended to improve emissions and immunity to conducted disturbances.

These capacitors must be connected between the two ground planes (GND and GNDF) through multiple vias, as shown in Figure 52 (see the yellow Circle 3 label in Figure 49).

Take care to meet the application creepage and clearance requirements because the distance between the ground planes and the copper on the capacitor footprint is lower than the creepage and clearance of the ADE1202. Through hole capacitors are not recommended.

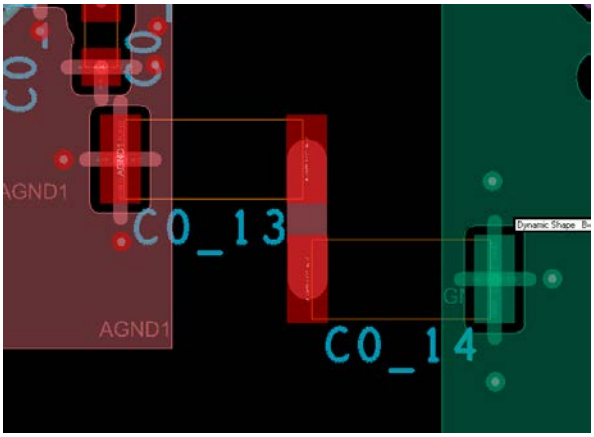


Figure 52. EMI Capacitor

APPLICATIONS INFORMATION

Table 16 lists the external components in the recommended ADE1202 application circuit, as shown in Figure 23.

Table 16. External Components

Component	Value	Recommended Component		Notes/Comments
		Manufacturer	Manufacturer Part Number[1]	
Capacitors				
Decoupling for VDDL, VDDI, VDD, VLDO	1 µF 0.1 µF	AVX AVX	0603YC105KAT2A 06035C104KAT2A	X7R, it is recommended to decouple each voltage rail with 1 µF and 0.1 µF
C1, C2	10 nF	TDK	CGA8L4C0G2J103J160KA	630 V high voltage capacitors, shunt high frequency disturbance from ADE1202 input
C3, C4	1000 pF	Murata	GRM188R71H102KA01D	50 V, ceramic X7R, required for proper function of the programmable load circuit of ADE1202
C6, C7	1 nF	TDK	C1608C0G2A102J	Creates low pass filter with R11 and R12
C13, C14	10 pF	TDK	C4520C0G3F100F085KA	3 kV, SMD, EMI capacitor, may be required to reduce radiated emissions
Resistors				
R1 to R6	95.3 kΩ	Panasonic	ERJ-8ENF9532V	1% 1206, forms part of the voltage divider, creepage and clearance requirements dictate the size of these components
R7, R8, R9	10 Ω	Vishay	SMM02070C1009FBP00	1%, 1 W, automotive grade metal electrode leadless face (MELF), serve as current limiting resistors and are required for surge and EMC withstand
R10, R11	1.1 kΩ	Panasonic	ERJ-6ENF1101V	1%, 0805, forms part of the voltage divider
R12, R13	10 Ω	Vishay	Y162910R0000B9R	0.1% Z foil, current limiting resistors
Other Components				
External FET (Q1, Q2)		Vishay	SIHFRC20TR-GE3	Pass device for programmable current, the operating point must fit within SOA under all conditions, maximum V_{GS} of 6 V.
Diode (D1, D2, D3)		Vishay	GL41M-E3/96	1 kV, 1 A, required for half wave rectification
Ferrite Beads (E1, E3, E4)		Murata	BLM31PG601SN1L	Active from 10 MHz to 300 MHz, improves radiated emissions and RF immunity
Ferrite Beads (E5, E6)		Murata	BLM31PG601SN1L	Active from 10 MHz to 300 MHz, aids in preventing FET parasitic oscillation
Metal Oxide Varistor (MOV) (V1, V2)	275 V ac/ 350 V dc	Kemet	VP3225K401R275	Provide transient voltage suppression

[1] Use recommended components or ones that are similar.

REGISTER MAP

Table 17. ADE1202 Address Map Register Summary

Address	Name	Description	Reset	Access
0x000	LOCK	Lock register	0x0001	R/W
0x001	CTRL	Control register	0x1080	R/W
0x002	BIN_CTRL	Binary channel control register	0x3610	R/W
0x003	BIN_THR	Binary channel threshold level register	0x5AAA	R/W
0x004	WARNA_THR	WARNAx channel threshold level register	0xCCCC	R/W
0x005	WARNB_THR	WARNBx channel threshold level register	0x5A88	R/W
0x006	WARNC_THR	WARNCx channel threshold level register	0x2D2D	R/W
0x007	BIN_FILTER	Binary channel configuration register	0x0096	R/W
0x008	WARNA_FILTER	WARNAx datapath configuration register	0x80FA	R/W
0x009	WARNB_FILTER	WARNBx datapath configuration register	0x80FA	R/W
0x00A	WARNC_FILTER	WARNCx datapath configuration register	0x80FA	R/W
0x00B	MASK	Interrupt mask register	0x4000	R/W
0x00C	INT_STATUS	Interrupt status register	0x0000	RW1C
0x00D	STATUS	Status register	0x4000	R
0x00E	ADC	ADC register	0x0000	R
0x00F	ADCDEC	ADC decimated register	0x0000	R
0x010	PL_CTRL	Programmable load control register	0x0000	R/W
0x011	PL_RISE_THR	Programmable load rise threshold register	0x001E	R/W
0x012	PL_LOW_CODE	Programmable load low code register	0x001E	R/W
0x013	PL_HIGH_CODE	Programmable load high code register	0x00C8	R/W
0x014	PL_HIGH_TIME	Programmable load high current period register	0x012C	R/W
0x015	EGY_MTR_CTRL	Energy meter control register	0x0505	R/W
0x016	EGY_MTR_THR	Energy meter max threshold register	0x9BA3	R/W
0x017	EGY_MTR1	Energy meter Channel 1 accumulator register	0x0000	R
0x018	EGY_MTR2	Energy meter Channel 2 accumulator register	0x0000	R
0x200	PL_EN	Programmable load enable register	0x0000	R/W
0x201	PGA_GAIN	PGA gain register	0x0000	R/W

REGISTER DETAILS

LOCK REGISTER

Address: 0x000, Reset: 0x0001, Name: LOCK

The user must write to the LOCK register to unlock the device before they can successfully write to any configuration register. The user can always read registers even when the device is locked.

Table 18. Bit Descriptions for LOCK

Bits	Bit Name	Description	Reset	Access
[15:4]	LOCK_KEY	Lock Key. To reset or set the LOCK bit, write the LOCK_KEY = 0xADE. To unlock the device, write 0xADE0 to the LOCK register. To lock the device, write 0xADE1 to the LOCK register.	0x0	W
[3:1]	RESERVED	Reserved.	0x0	R
0	LOCK	Lock Bit. After reset, the device is locked with the LOCK bit set to 1. To configure the device, write this bit to 0 and then write the desired configuration registers. After writing 1 to the LOCK bit, normal operation resumes in about 100 µs. The lock function does not affect the ADDR_RELOAD bit, the LOCK register, and the INT_STATUS register, which can all be written when LOCK = 1.	0x1	R/W

CONTROL REGISTER

Address: 0x001, Reset: 0x1080, Name: CTRL

The control register allows the user to change several operating modes and also read model and revision information.

Table 19. Bit Descriptions for CTRL

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	W
[13:12]	MODEL	Model Identifier. 0: reserved. 1: device is an ADE1202.	0x0	R
[11:9]	CHIP_ADDR	Chip Address. The CHIP_ADDR bit field is the chip address used by the SPI. The bit field value is determined based on the voltage on the ADDR pin at power-up.	0x0	R
[8:5]	REVID	Version Identifier. The current revision of the integrated circuit is 0x4.	0x4	R
4	SW_RST	Software Reset. Write a 1 to the SW_RST bit to reset the device.	0x0	W
3	ADDR_RELOAD	Address Reload. Write a 1 to this bit to force the chip address to be decoded and latched from the voltage on the ADDR pin.	0x0	W
2	IRQ_PIN_MODE	IRQ/DOUT2 Pin Mode. 0: the pin is assigned to DOUT2 and is in push/pull mode by default. 1: the pin is assigned to IRQ and is in open-drain mode.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	SPI_CRC_APPEND_EN	SPI CRC Append Enable. If this bit is set when the user performs an SPI read and keeps clocking for 16 cycles, a 16-bit CRC is appended to the read operation.	0x0	R/W

BINARY CHANNEL CONTROL REGISTER

Address: 0x002, Reset: 0x3610, Name: BIN_CTRL

Binary channel and warning controls for decimation and filter modes.

Table 20. Bit Descriptions for BIN_CTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	LOAD_STANDBY_MODE	Load Standby Mode. In load standby mode the binary channel monitors the load standby current instead of the ADC voltage values.	0x0	R/W
[13:12]	WARNC_MODE	Comparator Mode. 0: hysteretic mode. When the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. 1: midrange mode. When the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. 10: GT. When the ADC output is greater than the high threshold level, the comparator output is set high. 11: LT mode. When the ADC output is lower than or equal to the high threshold level, the comparator output is set high.	0x3	R/W
[11:10]	WARNB_MODE	Comparator Mode. 0: hysteretic mode. When the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. 1: midrange mode. When the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. 10: GT mode. When the ADC output is greater than the high threshold level, the comparator output is set high. 11: LT mode. When the ADC output is lower than or equal to the high threshold level, the comparator output is set high.	0x1	R/W
[9:8]	WARNA_MODE	Comparator Mode. 0: hysteretic mode. When the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. 1: midrange mode. When the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. 10: GT mode. When the ADC output is greater than the high threshold level, the comparator output is set high. 11: LT mode. When the ADC output is lower than or equal to the high threshold level, the comparator output is set high.	0x2	R/W
[7:6]	BIN_MODE	Comparator Mode. 0: hysteretic mode. When the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. 1: midrange mode. When the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. 10: GT mode. When the ADC output is greater than the high threshold level, the comparator output is set high. 11: LT mode. When the ADC output is lower than or equal to the high threshold level, the comparator output is set high.	0x0	R/W
[5:4]	INVALID_MODE	Invalid Mode. This bit field selects the value driven onto DOUTx in invalid mode. 00: DOUTx equals the FORCEVAL bit value. 01: DOUTx equals the binary filter output. 10: DOUTx toggles value on entering invalid mode. 11: DOUTx holds current value.	0x1	R/W
3	FORCEVAL	DOUTx Value During Invalid Mode.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[2:1]	DECRATE	Decimation Rate. The decimation rate used when decimation is enabled. 0: decimation filter is bypassed. 1: decimation rate equals 2. 10: decimation rate equals 4. 11: decimation rate equals 8.	0x0	R/W
0	DECIMATE	Enable Decimation. If this bit is set, the ADC data is decimated according to the DECRATE bit field setting. The decimated samples can be read back from the ADCDEC register.	0x0	R/W

BINARY CHANNEL THRESHOLD LEVEL REGISTER

Address: 0x003, Reset: 0x5AAA, Name: BIN_THR

Binary channel high and low threshold values.

Table 21. Bit Descriptions for BIN_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	BIN_LO_THR	Low Threshold Level. If the ADC is ≤ low threshold, the comparator output is reset.	0x5A	R/W
[7:0]	BIN_HI_THR	High Threshold Level. If the ADC is > high threshold, the comparator output is set.	0xAA	R/W

WARNAx CHANNEL THRESHOLD LEVEL REGISTER

Address: 0x004, Reset: 0xCCCC, Name: WARNA_THR

Warning A high and low threshold values.

Table 22. Bit Descriptions for WARNA_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNA_LO_THR	Low Threshold Level. If the ADC is ≤ low threshold, the comparator output is reset.	0xCC	R/W
[7:0]	WARNA_HI_THR	High Threshold Level. If the ADC is > high threshold, the comparator output is set.	0xCC	R/W

WARNBx CHANNEL THRESHOLD LEVEL REGISTER

Address: 0x005, Reset: 0x5A88, Name: WARNB_THR

Warning B high and low threshold values.

Table 23. Bit Descriptions for WARNB_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNB_LO_THR	Low Threshold Level. If the ADC is ≤ low threshold, the comparator output is reset.	0x5A	R/W
[7:0]	WARNB_HI_THR	High Threshold Level. If the ADC is > high threshold, the comparator output is set.	0x88	R/W

WARNCx CHANNEL THRESHOLD LEVEL REGISTER

Address: 0x006, Reset: 0x2D2D, Name: WARNC_THR

Warning C high and low threshold values.

Table 24. Bit Descriptions for WARNC_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNC_LO_THR	Low Threshold Level. If the ADC is ≤ low threshold, the comparator output is reset.	0x2D	R/W
[7:0]	WARNC_HI_THR	High Threshold Level. If the ADC is > high threshold, the comparator output is set.	0x2D	R/W

BINARY CHANNEL CONFIGURATION REGISTER

Address: 0x007, Reset: 0x0096, Name: BIN_FILTER

Binary channel configuration register.

Table 25. Bit Descriptions for BIN_FILTER

Bits	Bit Name	Description	Reset	Access
15	BIN_EN	DOUTx Datapath Enable. When this bit is zero, the comparator output is forced low. Note that this bit defaults to zero so that the datapath is disabled.	0x0	R/W
14	BIN_UPDWN	When set, the debounce filter is in up/down mode. By default the mode is up/clear mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	BIN_FILTER_VAL	Filter Length. The filter length is in 20 µs increments. Any input glitch less than the filter length is rejected such that the output does not change. If the filter length is zero, the filter is bypassed so the output equals the input with no latency.	0x96	R/W

WARNAx DATAPATH CONFIGURATION REGISTER

Address: 0x008, Reset: 0x80FA, Name: WARNA_FILTER

Warning A datapath configuration register.

Table 26. Bit Descriptions for WARNA_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNA_EN	Filter Comparator Enable.	0x1	R/W
14	WARNA_UPDWN	Filter Up/Down Mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNA_FILTER_VAL	Filter Length. Filter length is in 20 µs increments. Any input glitch less than the filter length is rejected such that the output does not change. If the filter length is zero, the filter is bypassed so the output equals the input with no latency.	0xFA	R/W

WARNBx DATAPATH CONFIGURATION REGISTER

Address: 0x009, Reset: 0x80FA, Name: WARNB_FILTER

Warning B datapath configuration register.

Table 27. Bit Descriptions for WARNB_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNB_EN	Filter Comparator Enable.	0x1	R/W
14	WARNB_UPDWN	Filter Up/Down Mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNB_FILTER_VAL	Filter Length. The filter length is in 20 µs increments. Any input glitch less than the filter length is rejected such that the output does not change. If the filter length is zero, the filter is bypassed so the output equals the input with no latency.	0xFA	R/W

WARNCx DATAPATH CONFIGURATION REGISTER

Address: 0x00A, Reset: 0x80FA, Name: WARNC_FILTER

Warning C datapath configuration register.

Table 28. Bit Descriptions for WARNC_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNC_EN	Filter Comparator Enable.	0x1	R/W
14	WARNC_UPDWN	Filter Up/Down Mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNC_FILTER_VAL	Filter Length. The filter length is in 20 µs increments. Any input glitch less than the filter length is rejected such that the output does not change. If the filter length is zero, the filter is bypassed so the output equals the input with no latency.	0xFA	R/W

INTERRUPT MASK REGISTER

Address: 0x00B, Reset: 0x4000, Name: MASK

If a bit in the MASK register is set, the associated status flag generates an interrupt, with the exception of Bit 15, DREADY, as described in Table 29.

Table 29. Bit Descriptions for MASK

Bits	Bit Name	Description	Reset	Access
15	DREADY	ADC Waveform Sample Interrupt Enable. Set this bit to 1 to enable 100 kHz interrupts synchronized when ADC samples are ready. When this bit is enabled, all other interrupts must be disabled with MASK register, Bits[14:0] equal to zero.	0x0	R/W
14	RSTDONE	Indicates that the device has reset and is ready to be programmed or begin default normal operation.	0x1	R/W
13	BUSY	Internal Communications Busy.	0x0	R/W
12	COOLDOWN2	Channel 2 Cool Down Mode Interrupt Enable. Set this bit to 1 to get an indication when channel 2 is in cool down mode to keep the device within a safe operating mode as configured by the internal FET power meter.	0x0	R/W
11	COOLDOWN1	Channel 1 Cool Down Mode Interrupt Enable. Set this bit to 1 to get an indication when channel 1 is in cool down mode to keep the device within a safe operating mode as configured by the internal FET power meter.	0x0	R/W
10	TSD	Programmable Load Thermal Shutdown Interrupt Enable. Set this bit to 1 to get an indication when the programmable load has been disabled due to thermal protection.	0x0	R/W
9	COMFLT	Isolated Communication Error Interrupt Enable. Set this bit to 1 to get an indication when there is an error in the internal data communicated between the isolated and nonisolated sides of the device. The device deals with retransmitting packets. If this error persists after writing a 1 to the COMFLT bit in the INT_STATUS register, then reconfigure the register settings in the device.	0x0	R/W
8	MEMFLT	Memory Fault Interrupt Enable. Set this bit to 1 to get an indication when there is a mismatch between the register values on the isolated and nonisolated sides of the device, indicating the registers must be reconfigured.	0x0	R/W
7	WARNC2	WARNC2 Interrupt Enable. Set this bit to 1 to get an indication when the WARNCx comparator output goes from logic low to logic high for the Channel 2 input.	0x0	R/W
6	WARNB2	WARNB2 Interrupt Enable. Set this bit to 1 to get an indication when the WARNBx comparator output goes from logic low to logic high for the Channel 2 input.	0x0	R/W
5	WARNA2	WARNA2 Interrupt Enable. Set this bit to 1 to get an indication when the WARNAx comparator output goes from logic low to logic high for the Channel 2 input.	0x0	R/W
4	DOUT2	DOUT2 Interrupt Enable. Set this bit to 1 to get an indication when the DOUT2 output pin goes from logic low to logic high.	0x0	R/W
3	WARNC1	WARNC1 Interrupt Enable. Set this bit to 1 to get an indication when the WARNCx comparator output goes from logic low to logic high.	0x0	R/W
2	WARNB1	WARNB1 Interrupt Enable. Set this bit to 1 to get an indication when the WARNBx comparator output goes from logic low to logic high.	0x0	R/W
1	WARNA1	WARNA1 Interrupt Enable. Set this bit to 1 to get an indication when the WARNAx comparator output goes from logic low to logic high.	0x0	R/W
0	DOUT1	DOUT1 Interrupt Enable. Set this bit to 1 to get an indication when the DOUT1 pin changes from logic low to logic high.	0x0	R/W

INTERRUPT STATUS REGISTER

Address: 0x00C, Reset: 0x0000, Name: INT_STATUS

The interrupt status register indicates which events capable of generating an interrupt have occurred. Write a 1 to the desired bit position to acknowledge the event and then clear the bit. This register can be written while the device is locked.

Table 30. Bit Descriptions for INT_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	RSTDONE	Indicates that the device has reset and is ready to be programmed or begin default normal operation.	0x0	RW1C
13	BUSY	Internal Communications Busy.	0x0	RW1C
12	COOLDOWN2	Channel 2 is in cool down mode.	0x0	RW1C

Bits	Bit Name	Description	Reset	Access
11	COOLDOWN1	Channel 1 is in cool down mode.	0x0	RW1C
10	TSD	Thermal Shutdown Detected.	0x0	RW1C
9	COMFLT	Communication Fault.	0x0	RW1C
8	MEMFLT	Memory Fault. When a memory fault is detected, the user can reconfigure the device.	0x0	RW1C
7	WARNC2	Warning C from Channel 2.	0x0	RW1C
6	WARNB2	Warning B from Channel 2.	0x0	RW1C
5	WARNA2	Warning A from Channel 2.	0x0	RW1C
4	DOUT2	DOUT2.	0x0	RW1C
3	WARNC1	Warning C from Channel 1.	0x0	RW1C
2	WARNB1	Warning B from Channel 1.	0x0	RW1C
1	WARNA1	Warning A from Channel 1.	0x0	RW1C
0	DOUT1	DOUT1.	0x0	RW1C

STATUS REGISTER

Address: 0x00D, Reset: 0x4000, Name: STATUS

The bits in this register are not latched and can be polled to determine the current status of the desired event.

Table 31. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	RSTBUSY	RSTBUSY goes from 0 to 1 to indicate that the device has reset and is ready to be programmed or begin default normal operation. Because this bit is active low, the user can distinguish between a bad read (0xFFFF) and an initialized device.	0x1	R
13	BUSY	Internal Communications Busy.	0x0	R
12	COOLDOWN2	Channel 2 is in cool down mode.	0x0	R
11	COOLDOWN1	Channel 1 is in cool down mode.	0x0	R
10	TSD	Thermal Shutdown Detected.	0x0	R
9	COMFLT	Communication Fault.	0x0	R
8	MEMFLT	Memory Fault. When a memory fault is detected, the user can reconfigure the device.	0x0	R
7	WARNC2	Warning C from Channel 2.	0x0	R
6	WARNB2	Warning B from Channel 2.	0x0	R
5	WARNA2	Warning A from Channel 2.	0x0	R
4	DOUT2	DOUT2.	0x0	R
3	WARNC1	Warning C from Channel 1.	0x0	R
2	WARNB1	Warning B from Channel 1.	0x0	R
1	WARNA1	Warning A from Channel 1.	0x0	R
0	DOUT1	DOUT1.	0x0	R

ADC REGISTER

Address: 0x00E, Reset: 0x0000, Name: ADC

ADC sample updates at 100 kHz, multiplexed into two channels updated at 50 kHz.

Table 32. Bit Descriptions for ADC

Bits	Bit Name	Description	Reset	Access
[15:8]	ADC2	ADC Channel 2.	0x0	R
[7:0]	ADC1	ADC Channel 1.	0x0	R

ADC DECIMATED REGISTER

Address: 0x00F, Reset: 0x0000, Name: ADCDEC

Decimated ADC sample(s).

Table 33. Bit Descriptions for ADCDEC

Bits	Bit Name	Description	Reset	Access
[15:8]	ADCDEC2	ADC Channel 2 Decimated. The sample is decimated at the rate determined by the DECRATE bit field.	0x0	R
[7:0]	ADCDEC1	ADC Channel 1 Decimated. The sample is decimated at the rate determined by the DECRATE bit field.	0x0	R

PROGRAMMABLE LOAD CONTROL REGISTER

Address: 0x010, Reset: 0x0000, Name: PL_CTRL

Configures the programmable load into low idle mode or high idle mode.

Table 34. Bit Descriptions for PL_CTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	PL_MODE	Programmable Load Mode. 0: low idle state. In low idle state, the programmable load current is configured for PL_LOW_CODE when the channel ADC code is greater than zero but less than the RISE_THR bit field. When the channel ADC value rises above the PL_RISE_THR, the load current is set to PL_HIGH_CODE. 1: high idle state. In high idle state, the programmable load current is set to PL_HIGH_CODE when the channel ADC code is higher than zero. The programmed load current flows as soon as there is enough voltage headroom on the respective pin, the LOAD1 pin for Channel 1 or the LOAD2 pin for Channel 2.	0x0	R/W

PROGRAMMABLE LOAD RISE THRESHOLD REGISTER

Address: 0x011, Reset: 0x001E, Name: PL_RISE_THR

Sets programmable load rising edge ADC sample threshold.

Table 35. Bit Descriptions for PL_RISE_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	RISE_THR	Rising Edge Threshold. When configured in low idle mode, with PL_MODE = 0, when the ADC value is greater than RISE_THR, the corresponding LOAD1 pin for Channel 1 or LOAD2 pin for Channel 2) is configured to sink a high current (PL_HIGH_CODE). The minimum value that can be written is 0x01 and the maximum value is 0xFE. These values are enforced by the hardware such that a write of 0x00 becomes 0x01 and 0xFF becomes 0xFE.	0x1E	R/W

PROGRAMMABLE LOAD LOW CODE REGISTER

Address: 0x012, Reset: 0x001E, Name: PL_LOW_CODE

Programmable load low code.

Table 36. Bit Descriptions for PL_LOW_CODE

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	LOW_CODE	Programmable Load Low Code. Minimum low current value is in units of 100 µA. The minimum value is 0x1. If 0x0 is written, LOW_CODE = 0x1.	0x1E	R/W

PROGRAMMABLE LOAD HIGH CODE REGISTER

Address: 0x013, Reset: 0x00C8, Name: PL_HIGH_CODE

Programmable load high code.

Table 37. Bit Descriptions for PL_HIGH_CODE

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	HIGH_CODE	Programmable Load High Code in Units of 200 µA. The minimum value that can be written is 0x1.	0xC8	R/W

PROGRAMMABLE LOAD HIGH CURRENT PERIOD REGISTER

Address: 0x014, Reset: 0x012C, Name: PL_HIGH_TIME

High current timer duration.

Table 38. Bit Descriptions for PL_HIGH_TIME

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	HIGH_TIME	Programmable Load High Current Period. When the programmable load goes into the high state, it pulls down the high current for the HIGH_TIME period, which is in units of 10 µs. The minimum HIGH_TIME is 10 µs. If 0 is written, HIGH_TIME = 1.	0x12C	R/W

ENERGY METER CONTROL REGISTER

Address: 0x015, Reset: 0x0505, Name: EGY_MTR_CTRL

Energy meter control register.

Table 39. Bit Descriptions for EGY_MTR_CTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	COOLDOWN_DECR	Cool Down Decrement. When the pulse current is turned off, the FET power accumulator is decremented by the COOLDOWN_DECR value every COOLDOWN_TIMESTEP.	0x5	R/W
[7:6]	OV_SCALE	Overvoltage Scale Factor. Applied when the ADC value is 0xFF. 0: multiply by 1. 1: multiply by 4. 10: multiply by 8. 11: multiply by 16.	0x0	R/W
[5:4]	COOLDOWN_TIMESTEP	Cool Down Timestep. When the pulse current is turned off, the FET power accumulator is decremented by the COOLDOWN_DECR value every COOLDOWN_TIMESTEP. 0: 10 µs. 1: 20 µs. 10: 40 µs. 11: 80 µs.	0x0	R/W
[3:0]	COOLDOWN_SEC	Cool Down Period. Cool down period is in seconds. A value of 0 disables the cool down function.	0x5	R/W

ENERGY METER MAXIMUM THRESHOLD REGISTER

Address: 0x016, Reset: 0x9BA3, Name: EGY_MTR_THR

Energy meter maximum energy threshold.

Table 40. Bit Descriptions for EGY_MTR_THR

Bits	Bit Name	Description	Reset	Access
[15:0]	MAX_EGY_THR	Maximum Energy Threshold. When the MAX_EGY_THR is exceeded, the device enters cool down mode. The threshold is scaled by 128. The energy meter accumulates the overscaled ADC values every 10 µs when the device is not in cool down mode.	0x9BA3	R/W

ENERGY METER CHANNEL 1 ACCUMULATOR REGISTER

Address: 0x017, Reset: 0x0000, Name: EGY_MTR1

Energy meter Channel 1.

Table 41. Bit Descriptions for EGY_MTR1

Bits	Bit Name	Description	Reset	Access
[15:0]	EGY_MTR1	Channel 1 Energy Meter. The current accumulated value.	0x0	R

ENERGY METER CHANNEL 2 ACCUMULATOR REGISTER

Address: 0x018, Reset: 0x0000, Name: EGY_MTR2

Energy meter Channel 1.

Table 42. Bit Descriptions for EGY_MTR2

Bits	Bit Name	Description	Reset	Access
[15:0]	EGY_MTR2	Channel 2 Energy Meter. The current accumulated value.	0x0	R

PROGRAMMABLE LOAD ENABLE REGISTER

Address: 0x200, Reset: 0x0000, Name: PL_EN

The programmable load enable.

Table 43. Bit Descriptions for PL_EN

Bits	Bit Name	Description	Reset	Access
15	EN2	Programmable Load Channel 2 Enable. Disable after power-on reset.	0x0	R/W
14	EN1	Programmable Load Channel 1 Enable. Disabled after power-on reset.	0x0	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R

PGA GAIN REGISTER

Address: 0x201, Reset: 0x0000, Name: PGA_GAIN

Gain value, as shown in Table 44.

Table 44. Bit Descriptions for PGA_GAIN

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	PGA_GAIN	PGA Gain, 2 Bits Decoded to a 4-Bit Thermometer Value. Supports the following four gain values: 0: gain equals 1. 1: gain equals 2. 10: gain equals 5. 11: gain equals 10.	0x0	R/W

OUTLINE DIMENSIONS

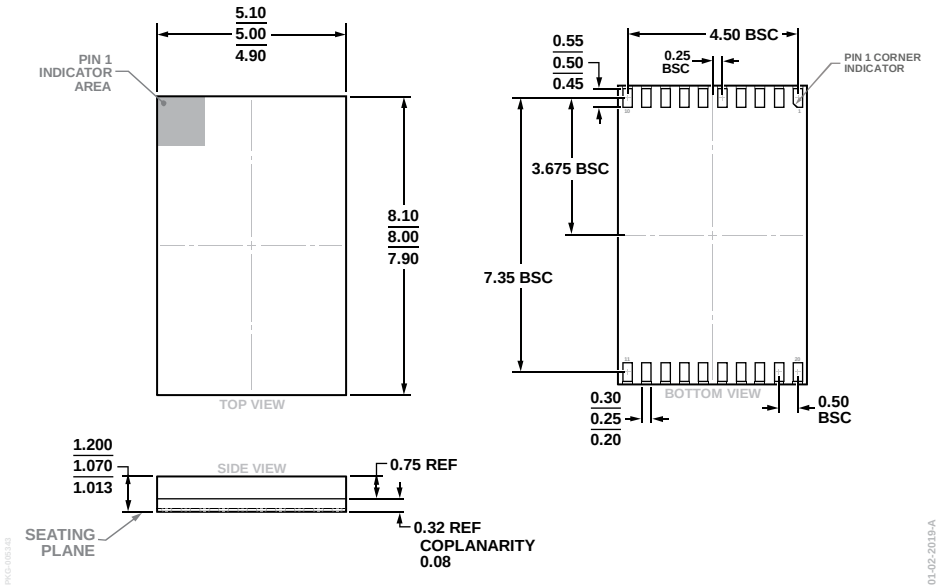


Figure 53. 20-Lead Land Grid Array [LGA]
(CC-20-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1,2]	Temperature Range	Package Description	Package Option
ADE1202ACCZ	−40°C to +125°C	20-Lead Land Grid Array [LGA]	CC-20-5
ADE1202ACCZ-RL	−40°C to +125°C	20-Lead Land Grid Array [LGA]	CC-20-5
EVAL-ADE1202EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-SDP-CB1Z is the controller board that manages the EVAL-ADE1202EBZ evaluation board. Both boards must be ordered together.