

# ESDM1131

## 3.3 V ESD Protection Diodes

### Micro-packaged Diodes for ESD Protection

The ESD1131 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

#### Features

- Low Capacitance (4 pF, I/O to GND)
- Small Body Outline Dimensions
  - ◆ 01005 Size: 0.445 x 0.240 mm
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_J$	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{\text{stg}}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	$T_L$	260	$^\circ\text{C}$
IEC 61000-4-2 Contact (ESD)	ESD	$\pm 16$	kV
IEC 61000-4-2 Air (ESD)	ESD	$\pm 16$	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



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#### MARKING DIAGRAM

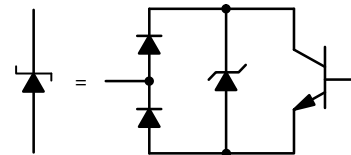
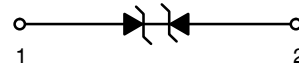


X4DFN2  
CASE 718AA



A = Specific Device Code

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# ESDM1131

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	I/O Pin to GND			3.3	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ , I/O Pin to GND	4.0	5.0	6.0	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3\text{ V}$ , I/O Pin to GND			0.1	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP} = 4\text{ A}$ , (8x20 $\mu\text{s}$ pulse)		5.6		V
Clamping Voltage TLP (Note 1)	$V_C$	$I_{PP} = 8\text{ A}$ } IEC 61000-4-2 Level 2 equivalent ( $\pm 4\text{ kV}$ Contact, $\pm 4\text{ kV}$ Air)		5.5		V
		$I_{PP} = 16\text{ A}$ } IEC 61000-4-2 Level 2 equivalent ( $\pm 8\text{ kV}$ Contact, $\pm 15\text{ kV}$ Air)		7.0		
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$		4.0		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 4\text{ ns}$ , averaging window;  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ .

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
ESDM1131MX4T5G	X4DFN2 (Pb-Free)	10,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

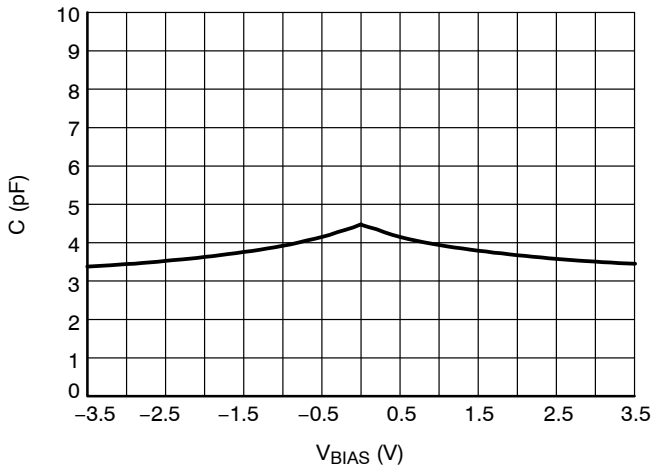


Figure 1. CV Characteristics

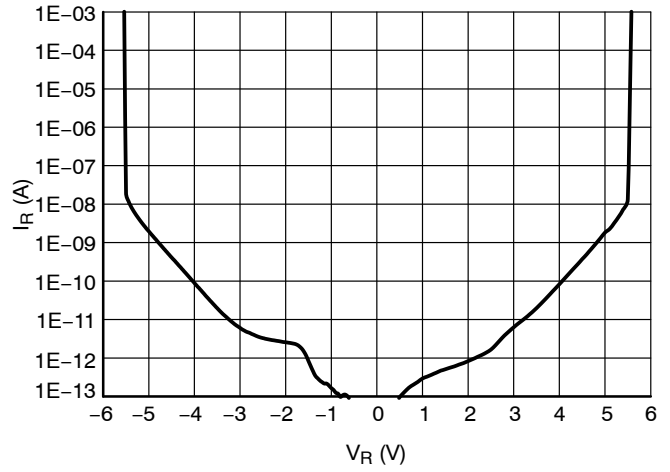


Figure 2. Reverse Leakage Current

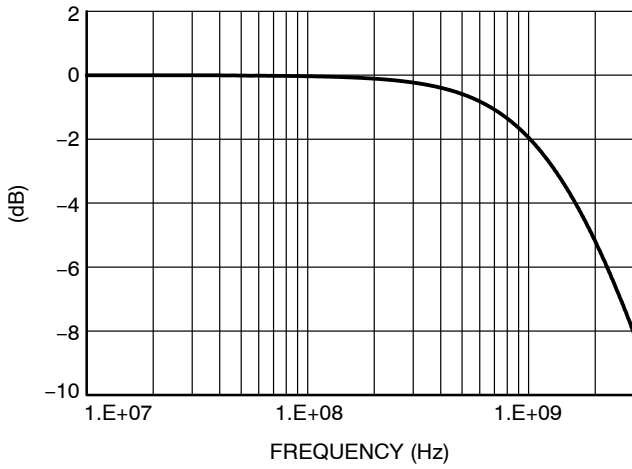


Figure 3. S21 Insertion Loss

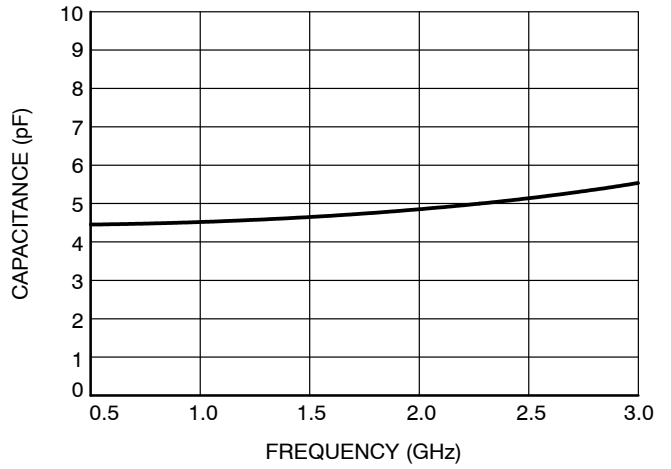


Figure 4. Capacitance over Frequency

# ESDM1131

## TYPICAL CHARACTERISTICS

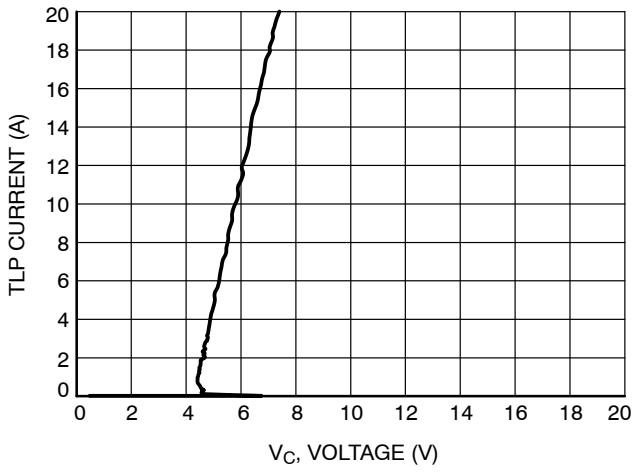


Figure 5. Positive TLP I-V Curve

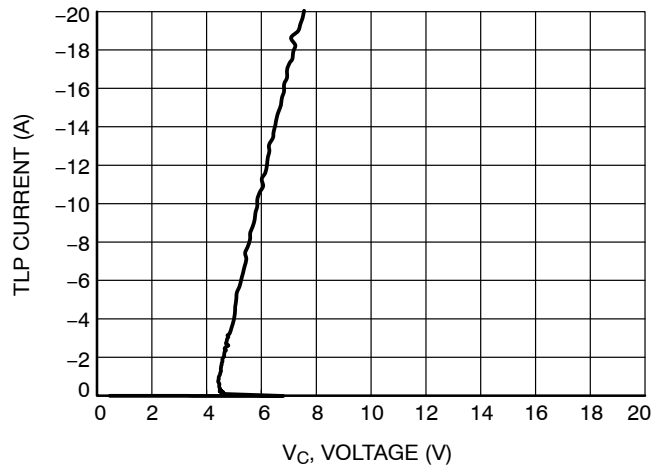


Figure 6. Negative TLP I-V Curve

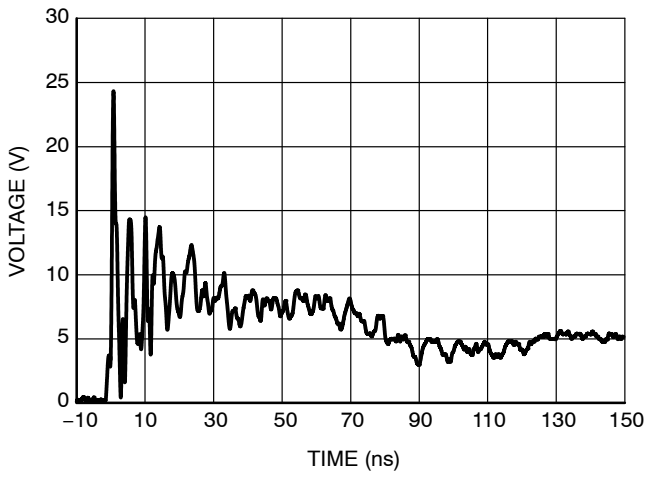


Figure 7. Positive 8 kV ESD Contact Discharge

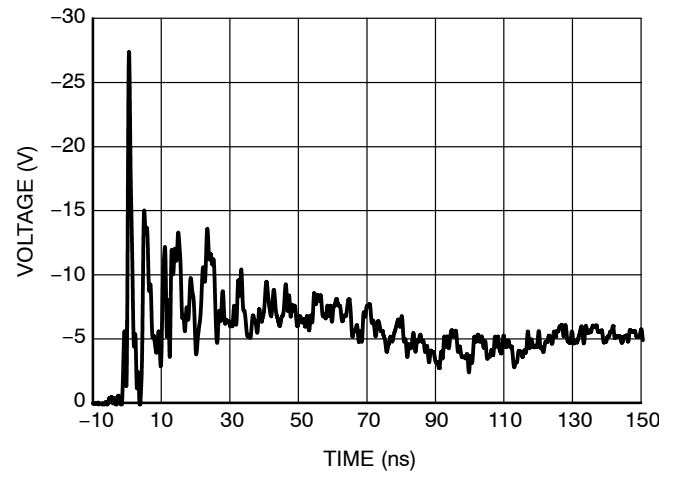


Figure 8. Negative 8 kV ESD Contact Discharge

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 9. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 10. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 11 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.



Figure 10. Simplified Schematic of a Typical TLP System

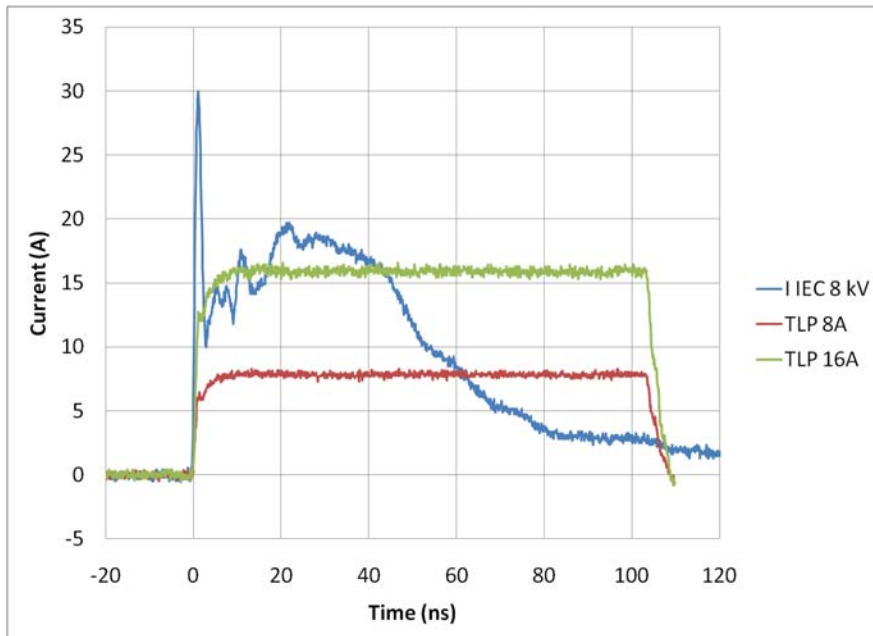


Figure 11. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

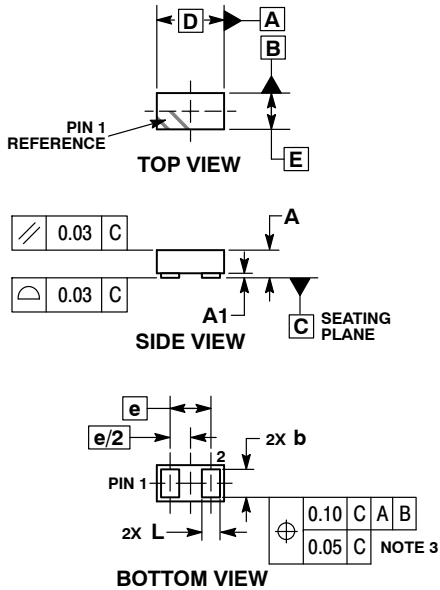
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SCALE 10:1

**X4DFN2, 0.445x0.24, 0.27P**  
**CASE 718AA**  
**ISSUE A**

DATE 21 MAR 2017

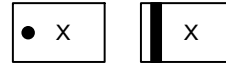


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.15	0.18	0.21
A1	---	---	0.03
b	0.170	0.185	0.200
D	0.415	0.445	0.475
E	0.210	0.240	0.270
e	0.270 BSC		
L	0.105	0.120	0.135

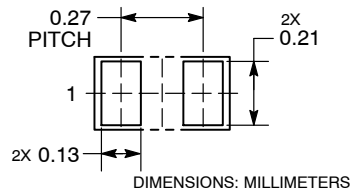
**GENERIC MARKING DIAGRAMS\***



X = Specific Device Code

\*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

**RECOMMENDED MOUNTING FOOTPRINT\***



See Application Note AND8398/D for more mounting details  
 \*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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