

P-Channel Power MOSFET

-40V, -51A, 16mΩ

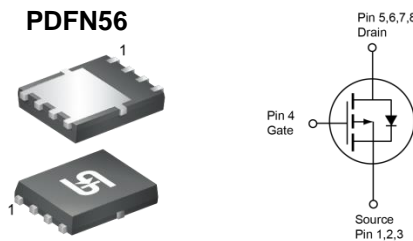
FEATURES

- AEC-Q101 Rev-D Qualified
- Logic level
- 100% UIS and R_g tested
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

PRODUCT SUMMARY		
PARAMETER	VALUE	UNIT
V_{DS}	-40	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	16
	$V_{GS} = -4.5V$	22
Q_g	23	nC

APPLICATIONS

- 12V Battery System for Automotive
- Battery Management System
- Infotainment



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	-51
		$T_A = 25^\circ\text{C}$	-10
Pulsed Drain Current	I_{DM}	-204	A
Single Pulse Avalanche Current ^(Note 2)	I_{AS}	-27	A
Single Pulse Avalanche Energy ^(Note 2)	E_{AS}	109	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	69
		$T_C = 125^\circ\text{C}$	14
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	2.6
		$T_A = 125^\circ\text{C}$	0.5
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	BV_{DSS}	-40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	$V_{GS(TH)}$	-1	-1.5	-2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = -40\text{V}$	I_{DSS}	--	--	-1	μA
	$V_{GS} = 0\text{V}, V_{DS} = -40\text{V}$ $T_J = 150^\circ\text{C}$		--	--	-100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = -10\text{V}, I_D = -10\text{A}$	$R_{DS(on)}$	--	9.9	16	m Ω
	$V_{GS} = -10\text{V}, I_D = -10\text{A},$ $T_J = 150^\circ\text{C}$		--	16.8	27.2	
	$V_{GS} = -4.5\text{V}, I_D = -8\text{A}$		--	13.5	22	
Forward Transconductance (Note 3)	$V_{DS} = -5\text{V}, I_D = -10\text{A}$	g_{fs}	--	31	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = -10\text{V}, I_D = -10\text{A},$ $V_{DS} = -20\text{V}$	Q_g	--	48	--	nC
Total Gate Charge	$V_{GS} = -4.5\text{V}, I_D = -8\text{A},$ $V_{DS} = -20\text{V}$	Q_g	--	23	--	
Gate-Source Charge		Q_{gs}	--	7	--	
Gate-Drain Charge		Q_{gd}	--	9	--	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = -20\text{V},$ $f = 1\text{MHz}$	C_{iss}	--	2712	--	pF
Output Capacitance		C_{oss}	--	270	--	
Reverse Transfer Capacitance		C_{rss}	--	150	--	
Gate Resistance	$f = 1\text{MHz}$	R_g	1.9	6.2	12.4	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = -10\text{V}, V_{DS} = -20\text{V},$ $I_D = -10\text{A}, R_G = 2\Omega$	$t_{d(on)}$	--	6.8	--	ns
Rise Time		t_r	--	2.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	63	--	
Fall Time		t_f	--	32	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = -10\text{A}$	V_{SD}	--	--	-1.2	V
Reverse Recovery Time	$I_S = -10\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	19	--	ns
Reverse Recovery Charge		Q_{rr}	--	11	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}, V_{GS} = -10\text{V}, V_{DD} = -25\text{V}, R_G = 25\Omega, I_{AS} = -27\text{A}$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

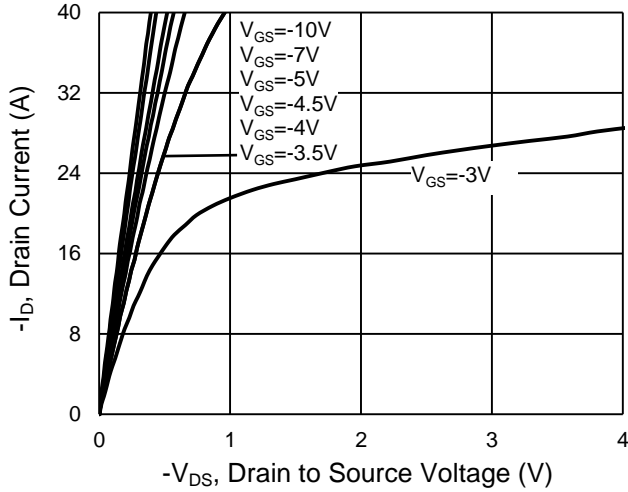
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM160P04LCRH RLG	PDFN56	2,500pcs / 13" Reel

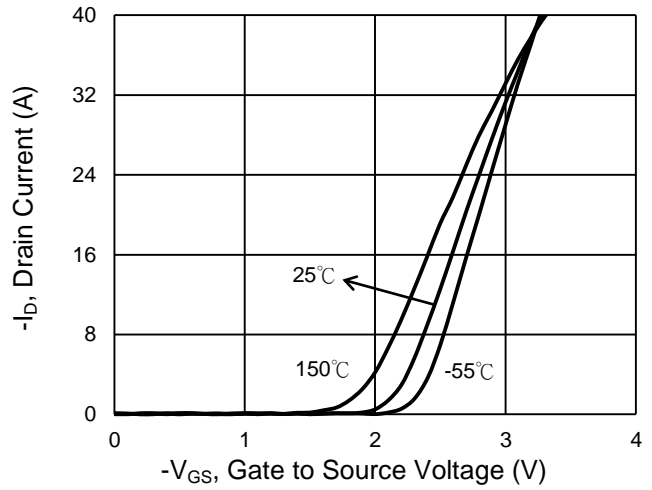
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

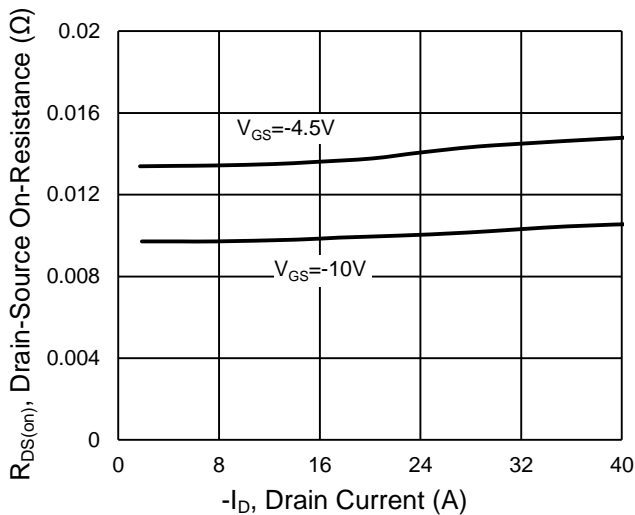
Output Characteristics



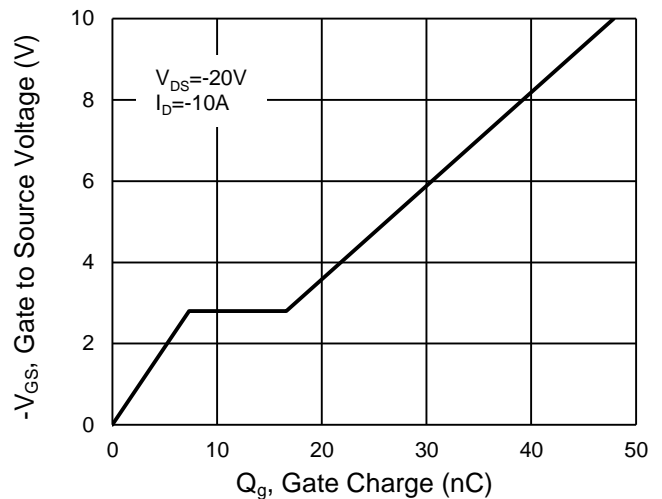
Transfer Characteristics



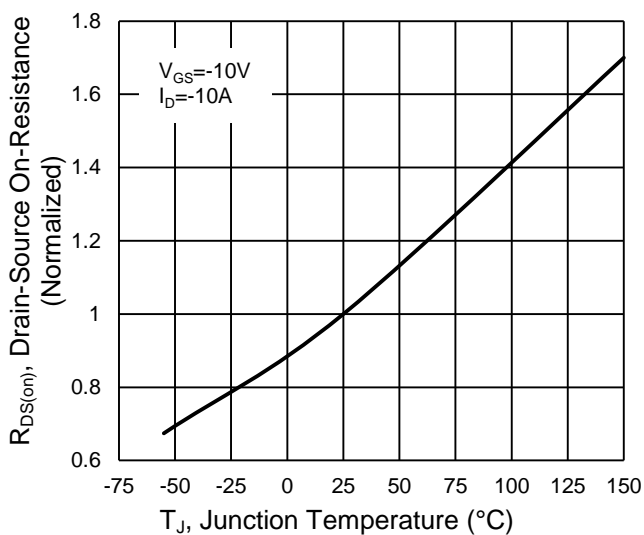
On-Resistance vs. Drain Current



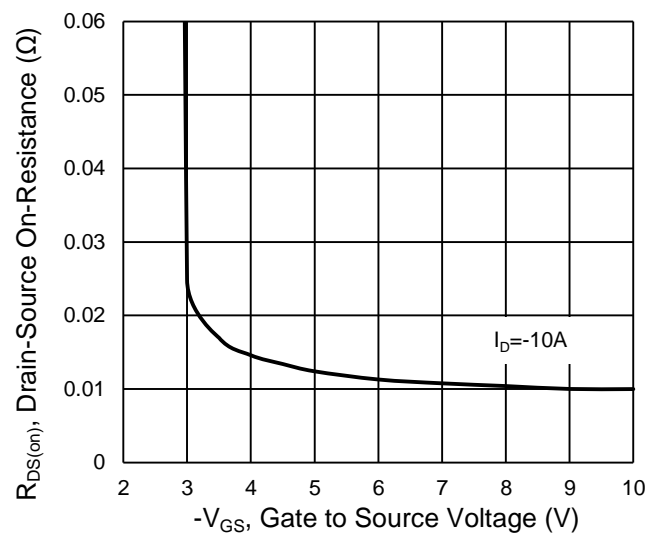
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



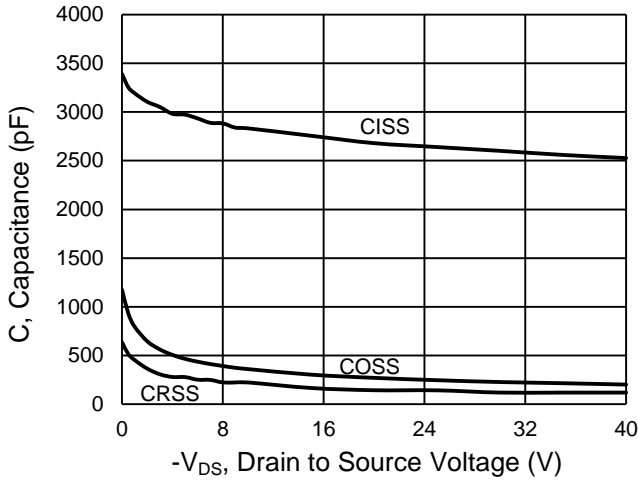
On-Resistance vs. Gate-Source Voltage



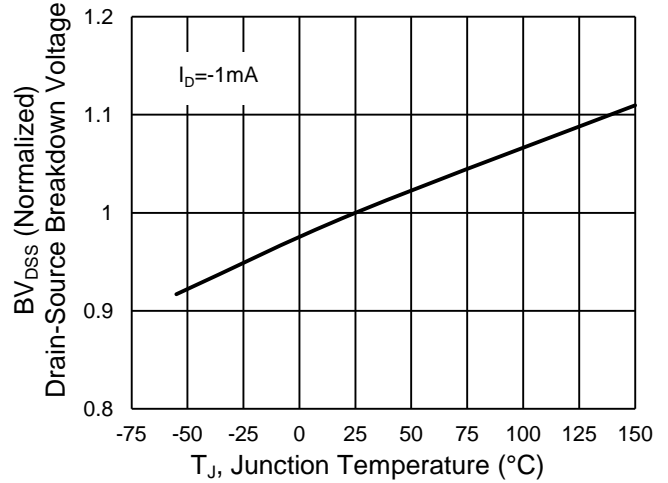
CHARACTERISTICS CURVES

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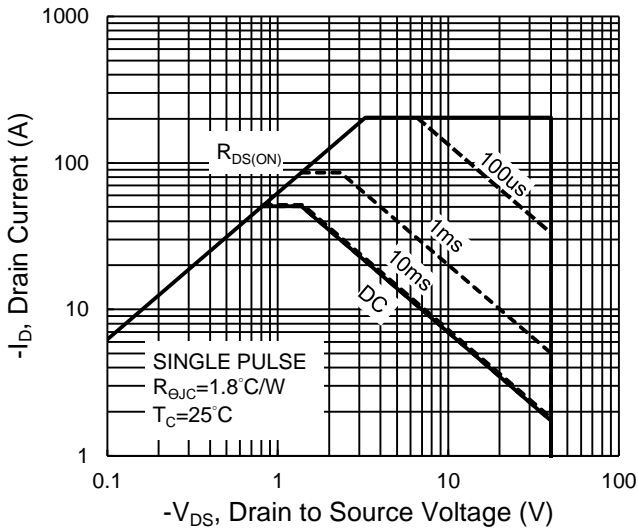
Capacitance vs. Drain-Source Voltage



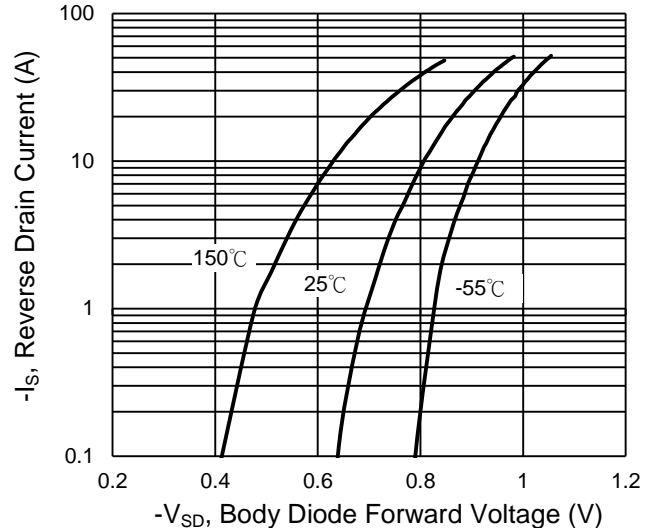
BV_{DSS} vs. Junction Temperature



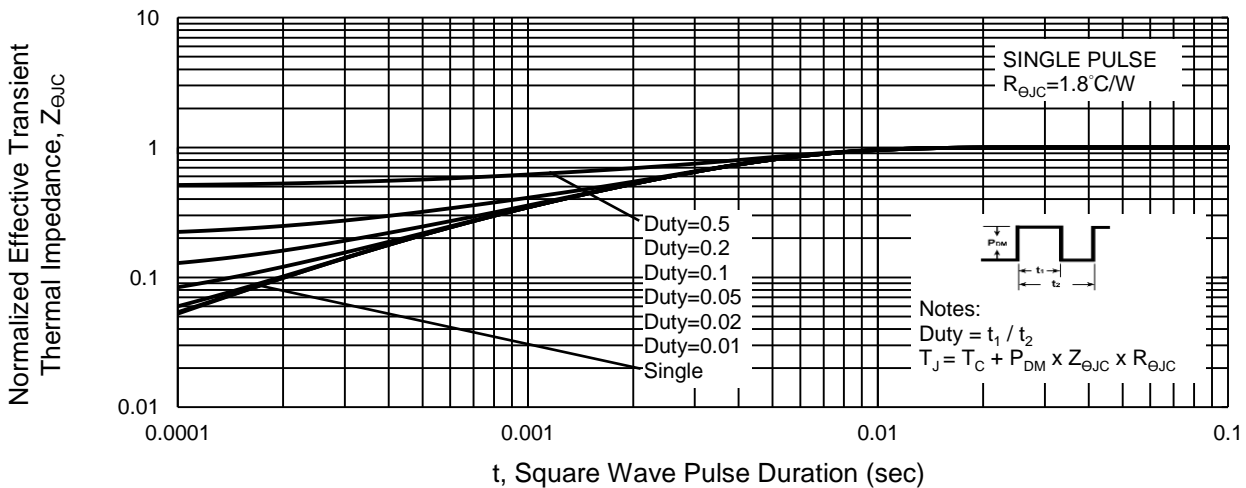
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

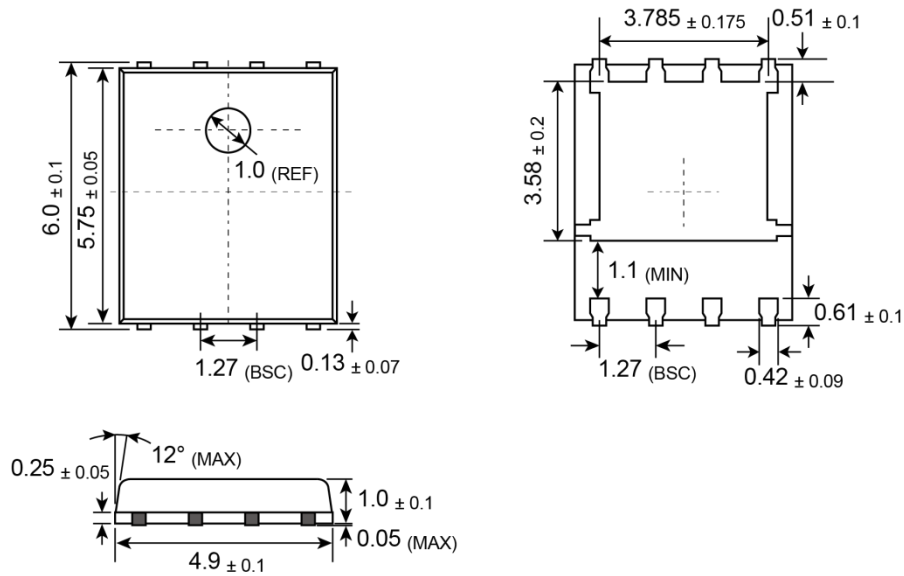


Normalized Thermal Transient Impedance, Junction-to-Case

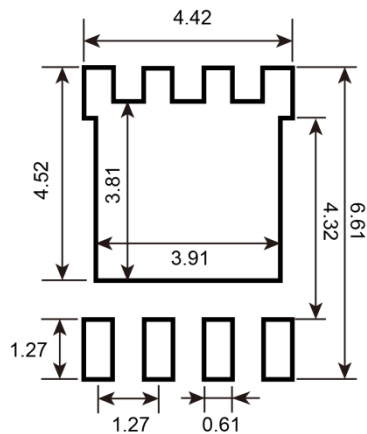


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code
- = AEC-Q101 Qualified

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