KAF-1001

1024 (H) x 1024 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−1001 Image Sensor is a high-performance charge-coupled device (CCD) designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Selectable on-chip output amplifiers allow operation to be optimized for different imaging needs: Low Noise (when using the high-sensitivity output) or Maximum Dynamic Range (when using the low-sensitivity output).

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Pixel Count	1024 (H) × 1024 (V)
Pixel Size	24 μm (H) × 24 μm (V)
Active Image Size	24.6 mm (H) × 24.6 mm (V) 34.8 mm (Diagonal) APS−H Optical Format
Chip Size	28.6 mm (H) × 25.5 mm (V)
Optical Fill-Factor	100%
Saturation Signal High Sensitivity Output High Dynamic Range	 240,000 electrons 650,000 electrons
Output Sensitivity High Sensitivity Output High Dynamic Range	 11 μV/electron 2 μV/electron
Readout Noise (1 MHz)	15 electrons rms
Dark Current (25°C, Accumulation Mode)	< 30 pA/cm^2
Dark Current Doubling Rate	5−6°C
Dynamic Range (Sat Sig/Dar Noise) High Sensitivity Output High Dynamic Range	 83 dB 97 dB
Quantum Efficiency (450, 550, 650 nm)	40%, 55%, 65%
Maximum Data Rate High Sensitivity Output High Dynamic Range	 5 MHz 2 MHz
Transfer Efficiency (2 MHz, to −40°C)	> 0.99997
Package	CERDIP Package (Sidebrazed)
Cover Glass	Clear

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

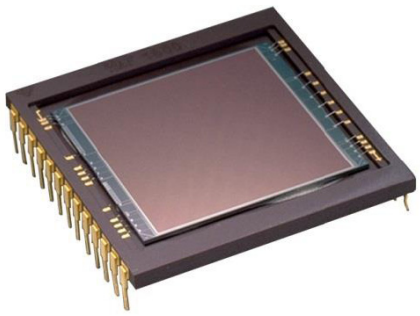


Figure 1. KAF−1001 CCD Image Sensor

Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity
- 100% Fill Factor
- Low Dark Current
- Single Readout Register
- User-selectable Outputs Allow either Low Noise or High Dynamic Range Operation

Applications

- Scientific
- Medical

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−1001 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−1001−AAA−CP−B1	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 1	KAF−1001−AAA Serial Number
KAF−1001−AAA−CP−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF−1001−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	
KAF−1001−AAA−CB−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	
KAF−1001−AAA−CB−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Grade 2	

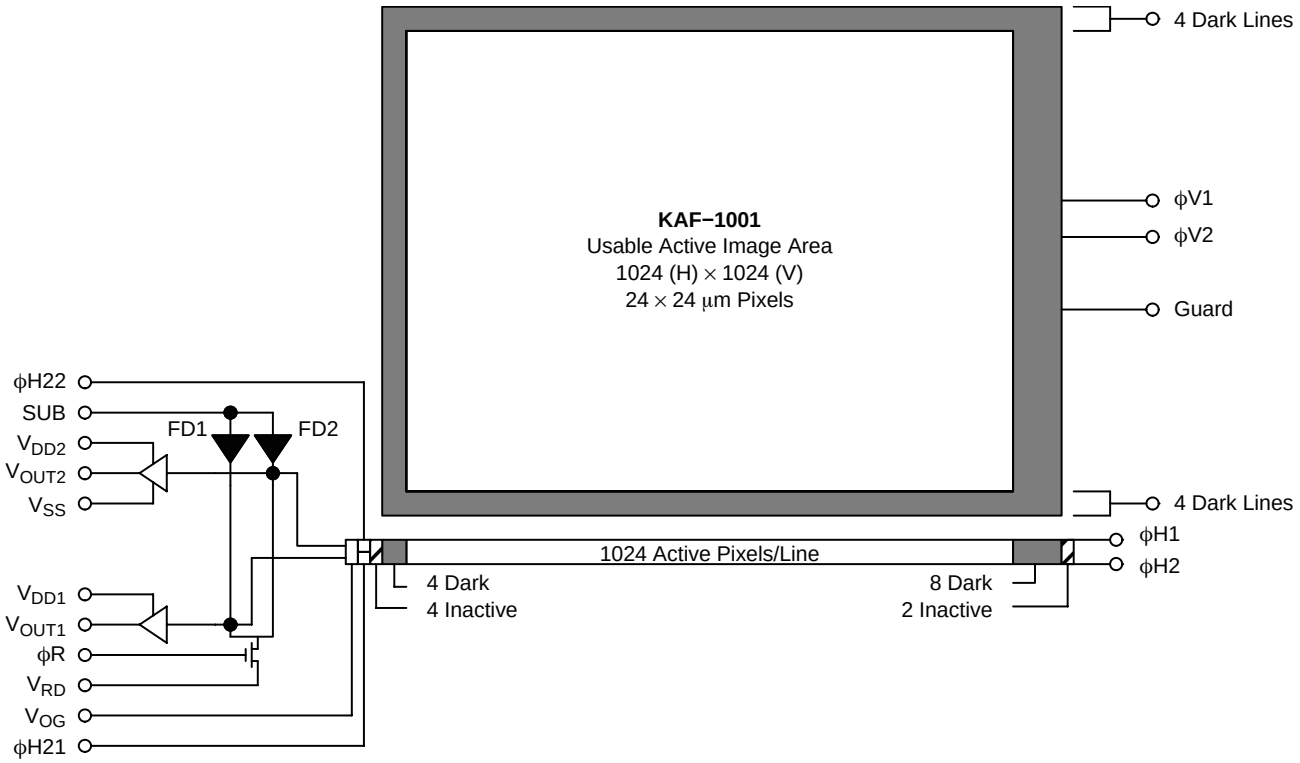
Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KEK−4H0080−KAF−1001−12−5	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture



NOTE: Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

Figure 2. Block Diagram

Refer to the block diagram in Figure 2. The KAF−1001 consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate true two-phase buried channel technology. The vertical register consists of 24 μm × 24 μm photo-capacitor sensing elements (pixels) which also serves as the transport mechanism. The pixels are arranged in a 1024 (H) × 1024 (V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. Because there is no storage array, this device must be synchronized with strobe illumination or shuttered during readout.

Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (V_{OUT1}), tie ϕH22 to a negative voltage to block charge transfer, and tie ϕH21 to ϕH2 to transfer charge. To use the high sensitivity two-stage output (V_{OUT2}), tie ϕH21 to a negative voltage and ϕH22 to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd} = \Delta Q/C_{fd}$. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

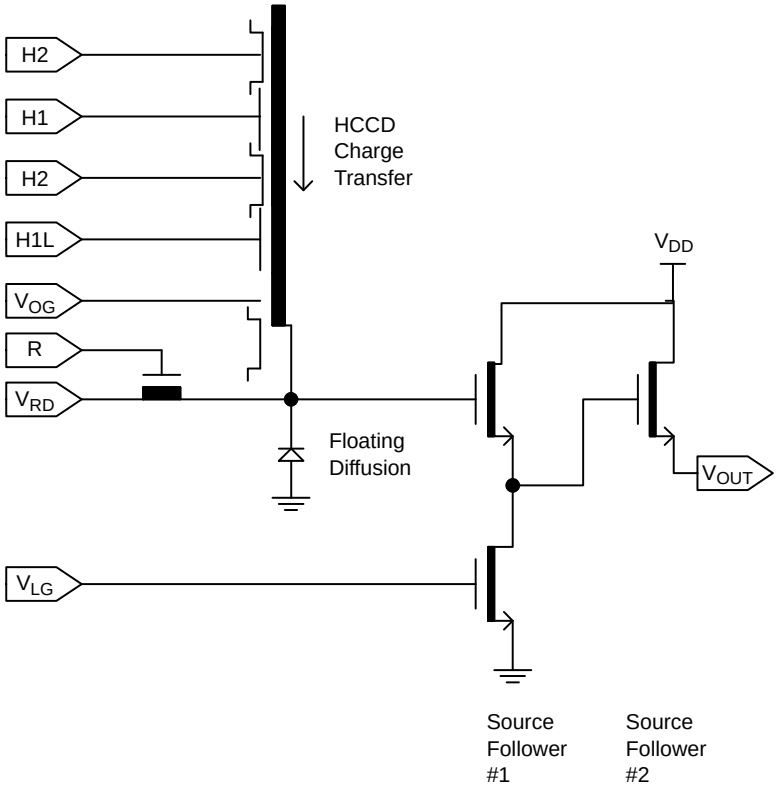


Figure 3. Output Schematic

Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will ‘bloom’ into vertically adjacent pixels.

Charge Transport

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. ‘Lines’ of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate.

ϕV1 and ϕV2 now reverse their polarity causing the charge packets to ‘spill’ forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which controls the output amplifier. The cycle repeats until all lines are read.

Physical Description

Pin Description and Device Orientation

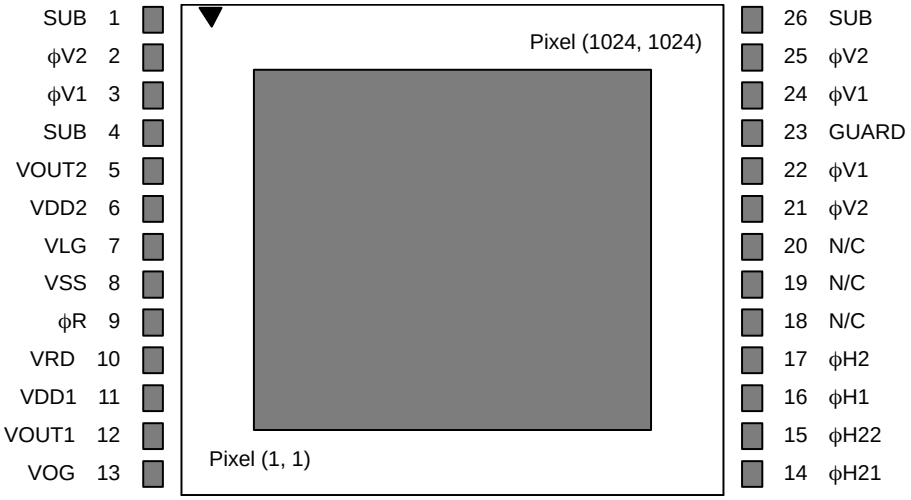


Figure 4. Pinout Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	SUB	Substrate
2	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
3	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
4	SUB	Substrate
5	VOUT2	Video Output from High Sensitivity Two-Stage Amplifier
6	VDD2	High Sensitivity Two-Stage Amplifier Supply
7	VLG	First Stage Load Transistor Gate for Two-Stage Amplifier
8	VSS	Output Amplifier Return
9	ϕR	Reset Clock
10	VRD	Reset Drain
11	VDD1	High Dynamic Range Single-Stage Amplifier Supply
12	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier
13	VOG	Output Gate
14	ϕH21	Last Horizontal (Serial) CCD Phase − Split Gate
15	ϕH22	Last Horizontal (Serial) CCD Phase − Split Gate
16	ϕH1	Horizontal (Serial) CCD Clock − Phase 1
17	ϕH2	Horizontal (Serial) CCD Clock − Phase 2
18	N/C	No Connection
19	N/C	No Connection
20	N/C	No Connection
21	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
22	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
23	GUARD	Guard Ring
24	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
25	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
26	SUB	Substrate

1. Pins 3, 22, and 24 must be connected together − only one Phase 1 clock driver is required.
2. Pins 2, 21, and 25 must be connected together − only one Phase 2 clock driver is required.

IMAGING PERFORMANCE

Typical Operational Conditions

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons: to convert to voltage, multiply by the amplifier sensitivity.

Specifications

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
ELECTRO-OPTICAL							
Optical Fill Factor	FF	−	100	−	%		
Photoresponse Non-uniformity	PRNU	−	−	5	% rms	Full Array	Die[10]
Quantum Efficiency (450, 550, 650 nm)	QE	−	−	−			Design[11]
CCD PARAMETERS COMMON TO BOTH OUTPUTS							
Sat. Signal − V_{CCD} Register	Ne^-_{SAT}	450	500	−	ke^-	2	Design[11]
Dark Current	J_D	− −	15.3 550	30 1,080	pA/cm^2 e^-/pix/sec	25°C (Mean of All Pixels)	Die[10]
Dark Current Doubling Temp	DCDR	5	6	7	°C		Design[11]
Dark Signal Non-uniformity	DSNU	−	−	1,080	e^-/pix/sec	4	Die[10]
Charge Transfer Efficiency	CTE	−	0.99997	−		5	Die[10]
V-H CCD Transfer Time	t_{VH}	−	32	−	μs	6, 7	Design[11]
Blooming Suppression	B_S	−	None	−			
CCD PARAMETERS SPECIFIC TO HIGH OUTPUT AMPLIFIER							
Output Sensitivity	V_{OUT}/Ne^-	9	11	−	$μV/e^-$		Design[11]
Sat. Signal	Ne^-_{SAT}	180	200	240	ke^-	1	Design[11]
Total Sensor Noise	ne^-_{TOTAL}	−	13	20	e^- rms	8	Design[11]
Horizontal CCD Frequency	f_H	−	2	5	MHz	6	Design[11]
Dynamic Range	DR	79	83	−	dB	9	Design[11]
CCD PARAMETERS SPECIFIC TO LOW GAIN (HIGH DYNAMIC RANGE) OUTPUT AMPLIFIER							
Output Sensitivity	V_{OUT}/Ne^-	1.7	2		$μV/e^-$		Die[10]
Sat. Signal	Ne^-_{SAT}	1,400	1,500	1,800	ke^-	3	Design[11]
Total Sensor Noise	ne^-_{TOTAL}	−	22	30	e^- rms	8	Die[10]
Horizontal CCD Frequency	f_H	−	0.5	2	MHz	6	Design[11]
Dynamic Range	DR	93	97	−	dB	9	Design[11]

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register.
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 64 sub arrays (128 × 128) exceed the maximum dark current specification.
5. For 2 MHz data rate and T = 30°C to −40°C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
7. Time between the rising edge of ϕV1 and the first falling edge of ϕH1.
8. At $T_{INTEGRATION}$ = 0; data rate = 1 MHz; temperature = −30°C.
9. Uses 20LOG (Ne^-_{SAT} / ne^-_{TOTAL}) where Ne^-_{SAT} refers to the amplifier saturation signal.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

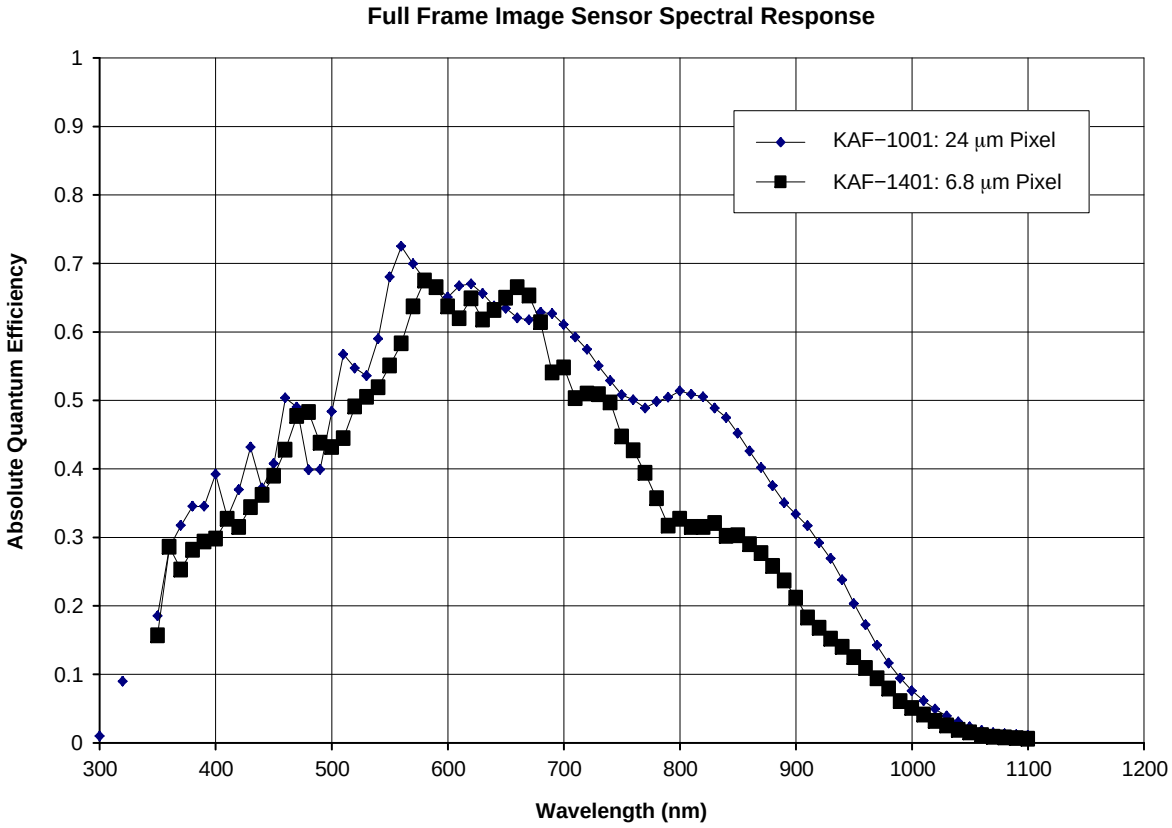


Figure 5. Typical Spectral Response

Figure 5 shows a representative spectral response of front side illuminated transparent gate full frame image sensors. The KAF−1001 with 24 μm pixels has higher response than the 6.8 μm pixel sensor at wavelengths greater than 750 nm because it is constructed on a lower resistivity silicon substrate. The resulting collection volume of each pixel more efficiently collects signal generated deeper within the silicon.

Most of the two phase CCD pixels are designed so that each of the electrodes occupies half of the pixel area. The KAF−1001 was not designed this way but instead is designed with the transparent electrode occupying greater than half the pixel area. This further improves the benefits of the transparent gate.

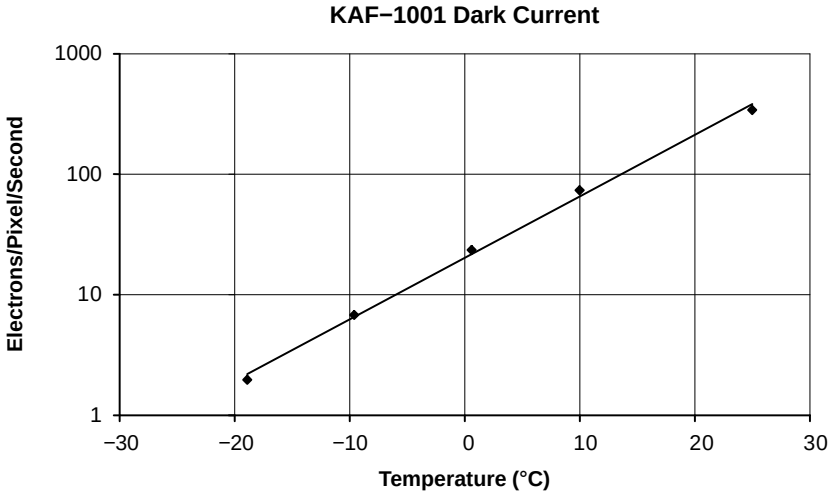


Figure 6. Dark Current as a Function of Temperature

DEFECT DEFINITIONS

Table 6. SPECIFICATIONS

Grade	Point Defect	Cluster Defect	Column Defect
C1	20	2	0
C2	40	10	2

Point Defects

Dark: A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel whose dark current exceeds 4,500 e^-/pix/sec at 25°C.

Cluster Defect

A grouping of not more than 5 adjacent point defects.

Column Defect

A grouping point defects along a single column (Dark column).

A column that contains a pixel whose dark current exceeds 150,000 e^-/pix/sec at 25°C (Bright column).

A column that does not exhibit the minimum charge capacity specification (Low Charge capacity).

A column that loses > 500 electrons when the array is illuminated to a signal level of 2,000 e^-/pix (Trap like defects).

Neighboring Pixels

The surrounding 128 × 128 pixels or ±64 columns/rows.

Defect Separation

Defects are separated by no less than 3 pixels in any one direction.

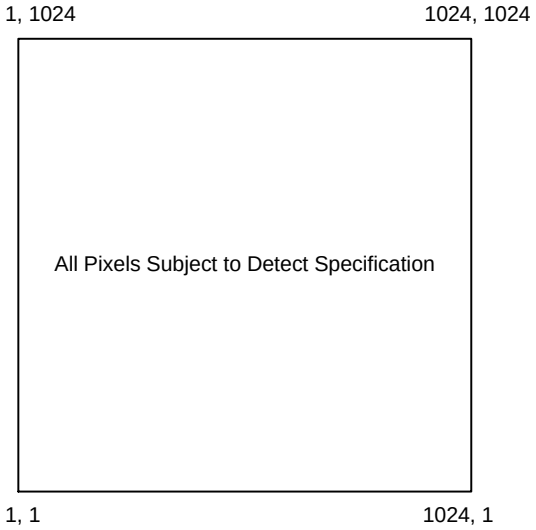


Figure 7. Active Pixel Region

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−100	+80	°C	At Device
Operating Temperature	T_{OP}	−50	+50	°C	At Device
Voltage	All Clocks	−16	+16	V	V_{SUB} = 0 V
Voltage	OG	0	+8	V	V_{SUB} = 0 V
Voltage	V_{RD}, V_{SS}, V_{DD}, GUARD	0	+20	V	V_{SUB} = 0 V
Current	Output Bias Current (I_{DD})	−	10	mA	
Capacitance	Output Load Capacitance (C_{LOAD})	−	10	pF	
Frequency/Time	ϕV1, ϕV2 Pulse Width	8	−	μs	
Frequency/Time	ϕH1, ϕH2	−	5	MHz	
Frequency/Time	ϕR Pulse Width	20	−	ns	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance	Notes
Substrate	V_{SUB}	0.0	0.0	0.0	V	Common	
Output Amplifier Supply	V_{DD}	15.0	17.0	17.5	V	5 pF, 2 kΩ	1
Output Amplifier Return	V_{SS}	1.4	2.0	2.1	V	5 pF, 2 kΩ	
Reset Drain	V_{RD}	11.5	12.0	12.5	V	5 pF, 1 MΩ	
Output Gate	OG	3.0	4.0	4.5	V	5 pF, 10 MΩ	
Guard Ring	GUARD	7.0	10.0	15.0	V	350 pF, 10 MΩ	
Load Gate	V_{LG}	V_{SS} − 0.5	V_{SS}	V_{SS} + 1.0	V		

1. V_{DD} = 17 V for applications where the expected output voltage > 2.0 V. For applications where the expected useable output voltage is < 2 V, V_{DD} can be reduced to 15 V.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical CCD Clock − Phase 1	ϕV1	Low	−10.25	−10.0	−9.8	V	200 nF, 10 MΩ
Vertical CCD Clock − Phase 1	ϕV1	High	0.0	0.0	1.0	V	
Vertical CCD Clock − Phase 2	ϕV2	Low	−10.25	−10.0	−9.8	V	200 nF, 10 MΩ
Vertical CCD Clock − Phase 2	ϕV2	High	0.0	0.0	1.0	V	$C_{\phi V1-V2}$ = 100 nF
Horizontal CCD Clock − Phase 1	ϕH1	Low	−2.2	−2.0	−1.8	V	400 pF, 10 MΩ
Horizontal CCD Clock − Phase 1	ϕH1	High	7.8	8.0	8.2	V	
Horizontal CCD Clock − Phase 2	ϕH2	Low	−2.2	−2.0	−1.8	V	250 pF, 10 MΩ
Horizontal CCD Clock − Phase 2	ϕH2	High	7.8	8.0	8.2	V	$C_{\phi H1-H2}$ = 200 nF
Reset Clock	ϕR	Low	2.0	3.0	3.5	V	10 pF, 10 MΩ
Reset Clock	ϕR	High	9.5	10.0	11.0	V	

Description	Symbol	Level	Using the High Gain Output (V_{OUT2})			Using the High Dynamic Range Output (V_{OUT1})			Units	Pin Impedance
			Min.	Nom.	Max.	Min.	Nom.	Max.		
Horizontal Clock − Phase 1	ϕH21	Low	−4	ϕH2 Low	ϕH2 Low	−	ϕH2	−	V	10 pF, 10 MΩ
Horizontal Clock − Phase 1	ϕH21	High	−4	ϕH2 Low	ϕH2 Low	−	ϕH2	−	V	
Horizontal Clock − Phase 2	ϕH22	Low	−	ϕH2	−	−	ϕH2 Low	ϕH2 Low	V	10 pF, 10 MΩ
Horizontal Clock − Phase 2	ϕH22	High	−	ϕH2	−	−	ϕH2 Low	ϕH2 Low	V	

1. When using V_{OUT1}, ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using V_{OUT2}, ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.
2. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MΩ are expected resistances. These pins are only verified to 1 MΩ.
3. ϕV1, 2 capacitances are accumulated gate oxide capacitance, and are an over-estimate of the capacitance.
4. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult ON Semiconductor in those situations in which operating conditions meet or exceed minimum or maximum levels.

TIMING

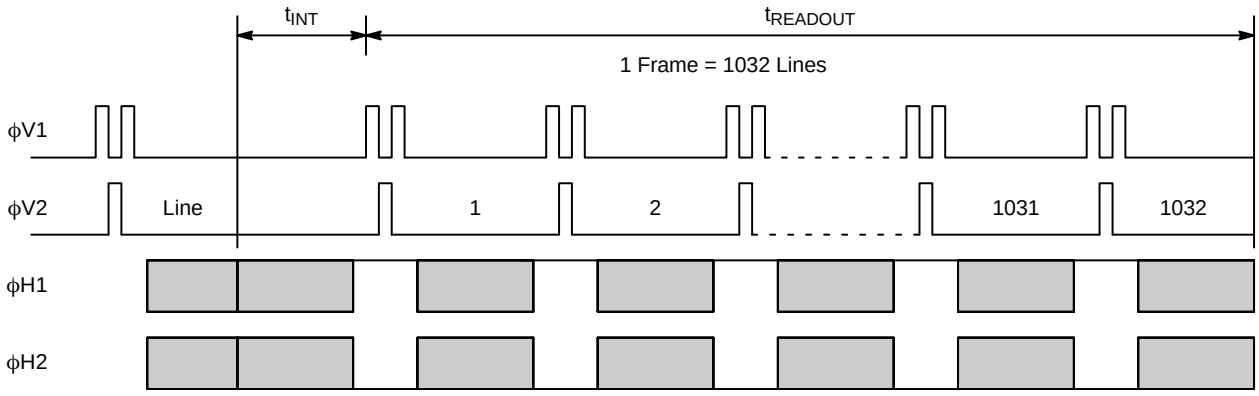
Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H	−	4	5	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V	−	100	125	kHz	1, 2, 3
Pixel Period (1 Count)	t_{PIX}	200	250	−	ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	500	1,000	−	ns	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5	−	μs	2
Reset Clock Pulse Width	$t_{\phi R}$	20	60	−	ns	4
Readout Time	$t_{READOUT}$	226	286	−	ms	5
Integration Time	t_{INT}	−	−	−		6
Line Time	t_{LINE}	219	277	−	μs	7

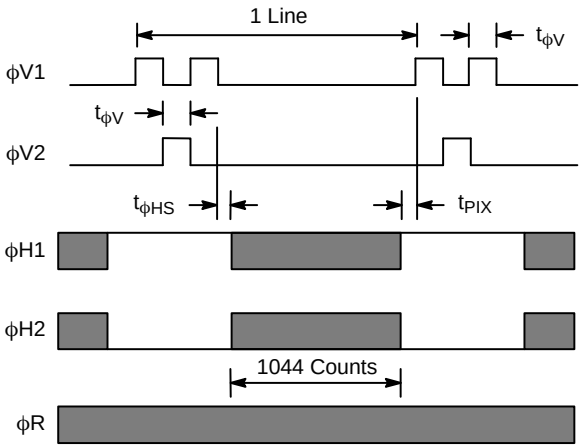
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5−10% of clock period. Crossover of register clocks should be between 40−60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{READOUT} = (1032 * t_{LINE})$
6. Integration time (t_{INT}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{LINE} = (3 * t_{\phi V}) + t_{\phi HS} + (1044* t_{PIX}) + t_{PIX}$

Normal Readout

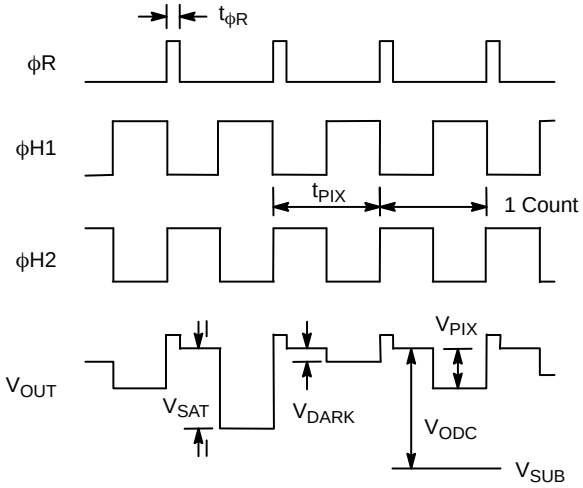
Frame Timing Detail



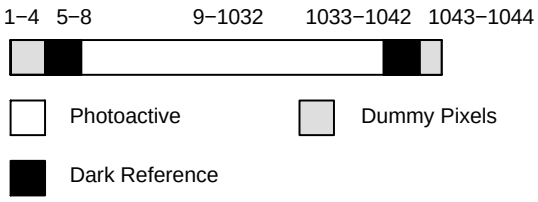
Line Timing Detail



Pixel Timing Detail



Line Content



V_{SAT}	Saturated pixel video output signal
V_{DARK}	Video output signal in no-light situation, not zero due to J_{DARK}
V_{PIX}	Pixel video output signal level, more electrons = more negative
V_{ODC}	Video level offset with respect to V_{SUB}*
V_{SUB}	Analog ground

* See Image Acquisition section.

Figure 8. Timing Diagram

NOTE: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult ON Semiconductor in those situations that require special consideration.

STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−100	+80	°C	At Device
Operating Temperature	T_{OP}	−50	90	°C	

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

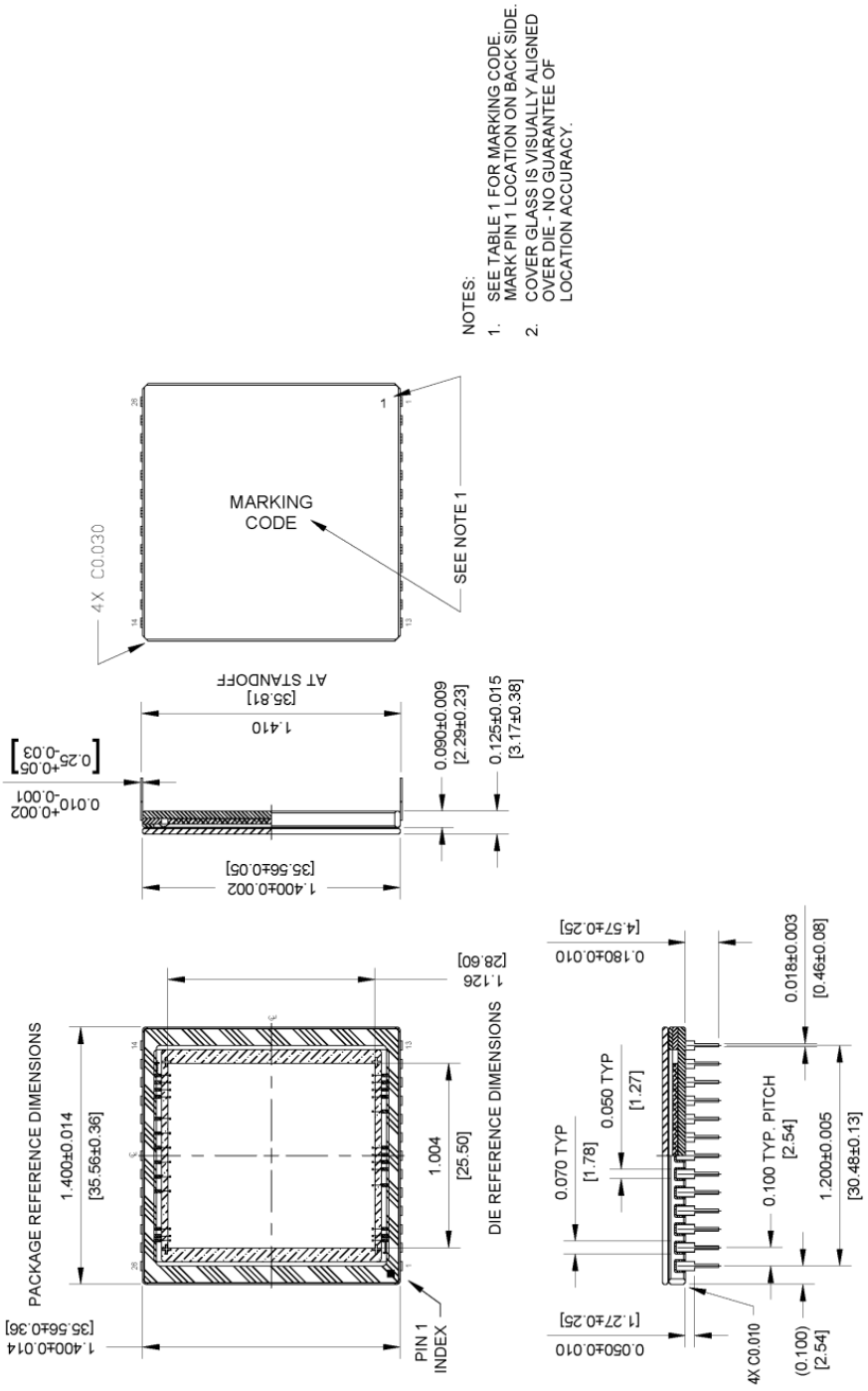


Figure 9. Completed Assembly (1 of 2)

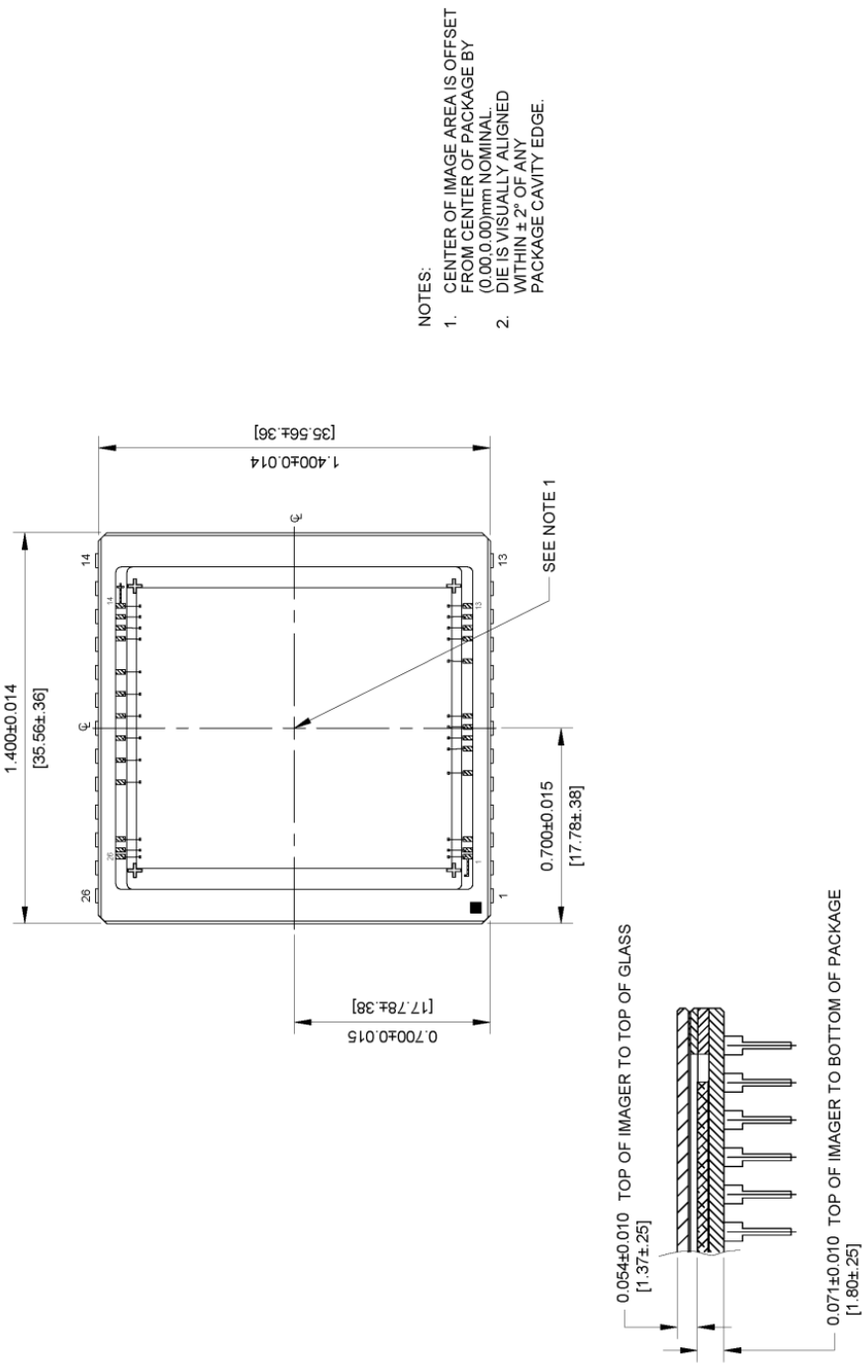


Figure 10. Completed Assembly (2 of 2)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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