User's Guide TPS38700Q1EVM Voltage Sequencer

TEXAS INSTRUMENTS

ABSTRACT

This user guide describes the operational use of the TPS38700Q1EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer. This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TPS38700Q1EVM is an evaluation module (EVM) for the TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer. Test points are provided to give the user additional access, if needed, for oscilloscope or multi-meter measurements.

The TPS38700Q1EVM comes pre-populated with TPS38700C03ARGERQ1. This option offers NEM_PD pin which allow the system to issue an emergency power down while also being able to sequence up to ten different devices all with a precise predefined sequence. The device also offers the option of battery backup power, a precise 32.768 kHz clock, and the ability to communicate faults via I2C. ACT and SLEEP pins allow for the device to change state depending on the logic level present on each. The NIRQ pin serves as an interrupt flag to alert the system to possible faults, and the NRST pin asserts logic high under reset condition.



Figure 1-1. TPS38700Q1EVM Board Top





Figure 1-2. TPS38700Q1EVM Board Bottom

1.1 Related Documentation

Datasheet: TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer

1.2 TPS38700-Q1 Applications

- Advanced Driver Assistance System (ADAS)
- Medical robotics
- Industrial robotics



2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS38700Q1EVM schematic, bill of materials (BOM), and layout.

2.1 TPS38700Q1EVM Schematic



Figure 2-1. TPS38700Q1EVM Schematic 1 of 2





Figure 2-2. TPS38700Q1EVM Schematic 2 of 2

SCL_D

SCL_D_BUF

SCL

R35

SCL_BUF



2.2 TPS38700Q1EVM Bill of Materials

	Table 2-1. BOM						
DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER	
РСВ	1		Printed Circuit Board		LP048	Any	
C1, C2, C13, C15, C16	5	10 µF	10 μF ±10% 25 V Ceramic Capacitor X7S 0805 (2012 Metric)	0805	C2012X7S1E106K125AC	TDK	
C3, C4, C14	3	0.1 µF	0.1 μF ±10% 10 V Ceramic Capacitor X7R 0402 (1005 Metric)	0402	885012205018	Wurth Electronics	
C5, C6	2	12 pF	CAP, CERM, 12 pF, 50 V, +/- 5%, C0G/NP0, 0201	0201	GRM0335C1H120JA01D	MuRata	
C7, C9, C10	3	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX	
C8	1	10 µF	10 μF ±10% 10 V Ceramic Capacitor X5R 0603 (1608 Metric)	0603	C1608X5R1A106K080AC	TDK	
C11, C12	2	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A101JAT2A	AVX	
D1, D2	2	Red	LED, Super Red, SMD	SMD	150060SS75000	Wurth Elektronik	
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.		N/A	N/A	
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear		SJ-5303 (CLEAR)	3М	
J1, J2, J5	3		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 TH	ED120/2DS	On-Shore Technology	
J3, J4, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18	15		Header, 100mil, 3x1, Gold, TH	3x1 TH	TSW-103-07-G-S	Samtec	
J19	1		Header (shrouded), 100mil, 5x2, Gold, TH	5x2 TH	5103308-1	TE Connectivity	
J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J34, J35	15		Header, 100mil, 2x1, Gold, TH	2x1 TH	TSW-102-07-G-S	Samtec	
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll		THT-14-423-10	Brady	
R1, R2, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29	26	10.0 kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo	
R3, R32	2	1Ω	1 Ω ±1% 0.25 W, ¼ W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	0603	RCS06031R00FKEA	Vishay	
R4, R33	2	1.0 kΩ	RES, 1.0 kΩ, 5%, 0.1 W, 0603	0603	RC0603JR-071KL	Yageo	
R5	1	4.7 kΩ	RES, 4.70 kΩ, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity	
R30, R31	2	2.2 kΩ	RES, 2.2 kΩ, 5%, 0.1 W, 0603	0603	RC0603JR-072K2L	Yageo	
R34, R36	2	10.0 kΩ	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	RCG060310K0FKEA	Vishay Draloric	

Table 2-1. BOM (continued)						
DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R35	1	1.0 kΩ	RES, 1.0 kΩ, 5%, 0.1 W, AEC- Q200 Grade 0, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R37, R38	2	21.0 kΩ	RES, 21.0 kΩ, 1%, 0.1 W, 0603	0603	RC0603FR-0721KL	Yageo
R39, R40	2	0 Ω	0 Ω Jumper 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	0603	ERJ-3GEY0R00V	Panasonic
SW1, SW2, SW3	3		Switch Tactile N.O. SPST Round Button J-Bend 32VAC 32 VDC 1VA 100000Cycles 3N SMD Tube/T/R	SMD	KT11P3JM34LFS	C&K Components
TP1, TP2, TP3, TP4, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP18, TP19, TP20, TP21, TP22, TP23, TP26, TP27, TP28	24		Terminal, Turret, TH, Triple	ТН	1598-2	Keystone
TP24, TP25	2		Test Point, Multipurpose, Purple, TH	тн	5129	Keystone
U2	1		Automotive, Level-Shifting I2C Bus Repeater, DGK0008A (VSSOP-8)	VSSOP-8	TCA9517DGKRQ1	Texas Instruments
U3	1		Dual-Channel, Low-Power Comparator with Integrated Reference (USON)	USON	TLV4082DRYR	Texas Instruments
U4	1		1 A Low-Quiescent-Current Low-Dropout (LDO) Regulator, DRV0006A (WSON-6)	WSON-6	TLV75712PDRVR	Texas Instruments
U5	1		1 A Low-Quiescent-Current Low-Dropout (LDO) Regulator, DRV0006A (WSON-6)	WSON-6	TLV75718PDRVR	Texas Instruments
U1	1		ASIL-A Multichannel I2C Programmable Voltage Sequencer (VQFN)	VQFN	TPS38700CRGER	Texas Instruments
Y1	1		Crystal, 32.768 kHz, 12.5 pF, SMD	SMD	NX3215SA-32.768K-STD- MUA-8	NDK



2.3 Layout and Component Placement

Figure 2-3 and Figure 2-4 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 2-5 and Figure 2-6 show the top and bottom layouts, Figure 2-7 and Figure 2-8 show the top and bottom layers, and Figure 2-9 shows the top solder mask of the EVM.

2.4 Layout



Figure 2-3. Component Placement—Top Assembly



Figure 2-4. Component Placement—Bottom Assembly



Schematic, Bill of Materials, and Layout



Figure 2-5. Layout—Top



Schematic, Bill of Materials, and Layout



Figure 2-6. Layout—Bottom





Figure 2-7. Top Layer





Figure 2-8. Bottom Layer



Figure 2-9. Top Solder Mask

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3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the EVM test points as well as their functional descriptions. All TPS38700-Q1 pins have a corresponding test point on the EVM. These test points are located close to the pins for more accurate measurements. In addition to the test points listed below, the EVM also has four additional GND test points.

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	EN1	Connection to EN1 pin	Allows the user to monitor the SENSE1 pin
TP2	EN2	Connection to EN2 pin	Allows the user to monitor the EN2 pin
TP3	EN3	Connection to EN3 pin	Allows the user to monitor the EN3 pin
TP4	EN4	Connection to EN4 pin	Allows the user to monitor the EN4 pin
TP6	ACT	Connection to ACT pin	Allows the user to set ACT input
TP7	EN5	Connection to EN5 pin	Allows the user to monitor the EN5 output
TP8	EN6	Connection to EN6 pin	Allows the user to monitor the EN6 output
TP9	NIRQ	Connection to NIRQ pin	Allows the user to monitor the NIRQ output
TP10	EN7	Connection to EN7 pin	Allows the user to monitor the EN7 output
TP11	EN8	Connection to EN8 pin	Allows the user to monitor the EN8 output
TP12	NRST	Connection to NRST pin	Allows the user to monitor the NRST output
TP13	EN9	Connection to EN9 pin	Allows the user to monitor the EN9 output
TP14	EN10/NEM_PD	Connection to EN10 pin and Emergency Shutdown pin	Allows the user to monitor the EN10 output
TP15	SLEEP	Connection to SLEEP pin	Allows the user to set SLEEP input
TP16	EN11/NRST_IN	Connection to EN11 pin and Reset In	Allows the user to monitor the EN11 output
TP18	EN12/NPWR_BTN	Connection to EN12 pin and Power Button	Allows the user to monitor the EN12 output
TP21	GND	GND for EVM	GND for EVM
TP22	CLK32K	Connection to CLK32K pin	Allows the user to monitor the CLK32K output
TP23	VENx	Connection to External Voltage	Allows the user to connect to an external voltage for pulling up enable pins
TP26	GND	GND for EVM	GND for EVM
TP27	GND	GND for EVM	GND for EVM
TP28	GND	GND for EVM	GND for EVM

Table 3-1. Test Points

3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS38700Q1EVM. As ordered, the EVM will have sixteen (16) jumpers installed. Figure 3-1 is provided as visual aid.

JUMPER	DEFAULT JUMPER CONFIGUATION	DESCRIPTION
J1	VBAT	For connecting VBAT power to the EVM
J2	VDD	For connecting VDD power to the EVM
J3 & J4	Shunt to bottom position	For connecting NRST and NIRQ to P1V8 or PEXT (Any external power)
J5	GND	For connecting GND to the EVM
J6	P1V8	For pulling- up ENABLE pins to P1V8 or VENX (Any external voltage)
J7 - J18	No connect	For pulling-up or down ENABLE pins (Only for open-drain configuration)/No connection for push-pull confiugration
J16	Shunt to top position	For pulling-up EN10 pin to P1V8.
J19	Connect	For connecting the EVM to TI's USB Interface Adapter
J20, J29, & J31	No connect	For connecting the on-board buffer to either P1V8, PEXT or P1V2. Only shunt one of these jumpers when using the buffer. Please revmove the shunt of J21 when using one of these jumpers.
J21	Shunt	For connecting the on-board bufffer IC to P3V3
J22 & J23	Shunt	For I2C lines to bypass buffer.
J24, J25, J27 & J28	No connect	For I2C lines to use the on-board buffer.
J30	No connect	For connecting VBAT to PEXT
J32	No connect	For connecting VENX to VBAT
J34 & J35	No connect	For manually pulling down NSLEEP and ACT pins

Table 3-2. List of On-board Jumpers



Figure 3-1. Jumper Settings



4 EVM Setup and Operation

This section describes the functionality and operation of the TPS38700Q1EVM. Refer to the TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer data sheet for details on the electrical characteristics of the device.

The TPS38700Q1EVM comes pre-populated with the TPS38700C03ARGERQ1. The EVM is capable of many different configurations in order to fully evaluate the functionality of all the TPS38700-Q1 device variants. The default configuration of the EVM Jumpers is mentioned in the Table 3-2. The TPS38700Q1EVM comes populated with I2C bus repeater, comparators, LDO, 32.768 kHz crystal and TPS38700C03ARGERQ1 programmable voltage sequencer.

The TPS38700Q1EVM also provides an option to apply a separate pull-up voltage to any of the ENABLE pins by changing the position of jumper J6 to VENx and connecting the pull-up voltage to test points TP23.

Equipment Needed

- TPS38700Q1EVM
- TI's USB Interface Adapter (with ribbon cable)
- Power Supply (3.3 V)
- Function Generator (provide pulse input for evaluation)
- Multi-channel Oscilloscope (review evaluation waveforms)
- Jumper Cables (additional evaluation)

4.1 Setup and GUI Installations

Follow the steps below for EVM connections and GUI installation:

- 1. Connect VBAT (J1) and VDD (J2) to 3.3 V from the power supply.
- 2. Connect GND (J5) to ground from the power supply.
- 3. Make sure the jumpers are connected as per the guidelines in the Table 3-2.
- 4. Power on the power supply briefly to check if the voltage is at 3.3 V and the quiescent current is at 10 mA. Once reviewed, power down the power supply.
- 5. Connect the Oscilloscope's channel 1 to TP1, channel 2 to TP2, and channel 3 to TP6.
- 6. Connect the function generator to TP6.
- 7. Connect the TI's USB Interface Adapter to J19 using a ribbon cable.
- 8. Connect the TI's USB Interface Adapter to the computer using the USB.
- 9. Final connections should look similar to . Figure 4-1.







Figure 4-1. EVM Connections for Testing EN1 and EN2



10. Install the GUI.

- a. Download the Fusion Digital Power Designer Platform GUI for TPS38700Q1EVM
- b. Open the downloaded file.
- c. In the Welcome Wizard window, click Next.



Figure 4-2. Welcome Setup Window

d. Accept the license agreement and then click Next.

👸 Setup - Fusion Digital Power Designer	_		×
License Agreement Please read the following important information before continuing.		Q	
Please read the following License Agreement. You must accept the agreement before continuing with the installation.	e terms of	this	
Important - Please read the following license carefully. This is a legally binding agreement. A this license agreement, you will be asked whether and agree to the terms of this license agreem click "I have read and agree" unless: (1) you ar to accept and agree to the terms of this license a behalf of yourself and your company; and (2) y enter into and to be bound by the terms of this leg agreement on behalf of yourself and your company	e agree fter you a rent. De re autho greeme rou inter gally bir ny.	ment ^ read ccept o not rized nt on nd to nding	
● I accept the agreement			
\bigcirc I do not accept the agreement			
< Back N	ext >	Can	icel

Figure 4-3. Setup License Agreement Window



e. The default destination folder works best. Click Next.

🛃 Setup - Fusion Digital Power Designer	-		×
Select Destination Location Where should Fusion Digital Power Designer be installed?			
Setup will install Fusion Digital Power Designer into the follow	ing fold	ler.	
To continue, click Next. If you would like to select a different folder, o	lick Bro	wse.	
rogram Files (x86)\Texas Instruments\Fusion Digital Power Designer	Bro	owse	
At least 72.6 MB of free disk space is required.			
< Back Next	>	Car	ncel

Figure 4-4. Setup Destination Window

f. Click Next for the Select Start Menu Folder option.

🔂 Setup - Fusion Digital Power Designer	_		×
Select Start Menu Folder Where should Setup place the program's shortcuts?			Ð
Setup will create the program's shortcuts in the following S	tart Mei	nu folder.	
To continue, click Next. If you would like to select a different folder,	click Br	owse.	
Texas Instruments\Fusion Digital Power Designer	B	rowse	
Don't create a Start Menu folder			
< Back Nex	:t >	Ca	ncel

Figure 4-5. Setup Window - Start Menu Selection



g. There is no need to install additional options for this EVM. Click Next.

🐻 Setup - Fusion Digital Power Designer	_		×
Select Additional Tasks Which additional tasks should be performed?		¢	
Select the additional tasks you would like Setup to perform while Power Designer, then dick Next.	installing Fu	ision Digit	al
Additional icons:			
Create a desktop icon			
Create a Quick Launch icon			
Other desktop shortcuts			
SMBus I2C SAA Debug Tool			
UCD9xxx Device GUI			
Additional Tasks:			
Add application directory to your system PATH			
< Back	Next >	Can	icel

Figure 4-6. Setup Window - Additional Tasks

h. Finally click Install to install the Fusion software.

1 🔁 S	etup - Fusion Digital Power Designer —		×
F	Ready to Install Setup is now ready to begin installing Fusion Digital Power Designer on your computer.		
1	Click Install to continue with the installation, or click Back if you want to review change any settings.	N Or	
	Destination location: C:\Program Files (x86)\Texas Instruments\Fusion Digital Power Designer		^
	<	>	~
	< Back Install	С	ancel

Figure 4-7. Setup Installation Window



i. Click on Finish to complete the installation setup and launch the software.



Figure 4-8. Installation Complete Window



4.2 GUI

This section shows the graphical user interface (GUI) the user will use to interact with the EVM. Refer to the TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer datasheet for details on the register description of the device.











EVM Setup and Operation

e to Hardware X Dis	scard Changes	C Refresh	All Store to	NVM Resto	re from NVM Cle	ear Faults	Change I2C A	ddress									
3700C Device Specific	Registers																
Config System Config	Sequence Confi	ig Watchdog	Config Alarr	ms (RTC) Confi	ig				^	Stat	tus Registers - Interru	ıpt					Status F
Fime Config —										INT	_SRC (10h)	GLR	IN	T SRC2 (11h)	OLR	1 6	EN ST/
250 🗸										7	F_INTERR	OLR	7	F_VENDOR	CLR		
Time slot between sequ	uencing points =	TIME[7:0] *	SSTEP + T_m	in, where T_m	in = 125 µs	-				6	EM_PD	613	6	F_SDA	CLR		EN1
	TIME[7:	0] Min (-	6%) T	ypical M	1ax (+6%)					5	WDT	018	5	RT_CRC	CLR		
Power-up / Sleep-exit	t 2	÷ 587	.5	625.0 💭	662.5 µs					4	PEC	OLR	4	BIST	OLR		EN2
Power-down / Sleep-e	entry 2	587	.5	625.0 🚑	662.5 µs					3	RTC	GLR	3	LDO	CLR		
										2	F_EN	OLR	2	TSD	OLR		EN3
									-	- III-							
P ins mapping If Pin not mapped (Non	ne), pin maintain (previous stat	e, unless ente	ering BACKUP o	r FAILSAFE state, i	in these two	o states, pin is	pulled Low.]	1	F_0SC	ØLR	1	ECC_DED	OLR.		
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti	ne), pin maintain p e of the time slot[ime slot where 1s	previous stat 1:15], pin will it is first up (o	e, unless ente be up (Power r down), and	ring BACKUP o r-up/Sleep-exit 15th is last up	r FAILSAFE state, i t sequence), or dow (or down).	in these two wn (Power-d	o states, pin is Iown/Sleep-ent	pulled Low. try		1	F_OSC F_NRSTIRQ	OLR OLR	1	ECC_DED PBSP	OLR OLR		EN4
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti	ne), pin maintain p e of the time slot[ime slot where 1s Powe	previous stat 1:15], pin will it is first up (o	e, unless ente be up (Power r down), and Power	ring BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i t sequence), or dow (or down).	in these two vn (Power-d E xit	o states, pin is lown/Sleep-ent Sleep I	pulled Low. try Entry		1 0 Stat	F_OSC F_NRSTIRQ tus Register - Control		1	ECC_DED PBSP			EN4 EN5
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti Pins 12 (CLK220E)	ne), pin maintain ; e of the time slot[ime slot where 1s Power	previous stat 1:15], pin will it is first up (c r Up	e, unless ente be up (Power r down), and Power	ering BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i t sequence), or dow (or down). Sleep E	in these two wn (Power-d	o states, pin is down/Sleep-ent Sleep I	pulled Low. try Entry		1 0 Stat	F_OSC F_NRSTIRQ tus Register - Control STAT (13h)	013	1 0	ECC_DED PBSP ST_RST (1Ah)			EN4 EN5
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E)	ne), pin maintain p e of the time slot[ime slot where 1s Powe 4th	previous stat 1:15], pin will it is first up (o r Up	e, unless ente be up (Power r down), and Power 4th	ering BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i t sequence), or dow (or down). Sleep E None	in these two wn (Power-d Exit	o states, pin is down/Sleep-ent Sleep I None	pulled Low. try Entry		1 0 Stat	F_OSC F_NRSTIRQ tus Register - Control STAT (13h) ST_WD_EN ST_VBRAT		1 0 LA 7 6	ECC_DED PBSP ST_RST (1Ah) NRST WDT RST			EN4 EN5 EN6
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1)	ne), pin maintain (e of the time slot[ime slot where 1s Power 4th 1st	previous stati (1:15], pin will it is first up (o r Up	e, unless ente l be up (Power r down), and Power 4th 5th	ering BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i t sequence), or dow (or down). Sleep E None None	in these two wn (Power-d Exit	o states, pin is lown/Sleep-ent Sleep I None None	pulled Low. try Entry		1 0 Stat 7 6 5	F_OSC F_NRSTIRQ usRegister - Control STAT (13h) ST_WD_EN ST_VBBAT ST_NRQ		1 0 7 6 5	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN			EN4 EN5 EN6
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the time Pins 13 (CLK320E) 19 (EN1) 20 (EN2)	he), pin maintain n e of the time slot[ime slot where 1s Power 4th 1st 1st	previous stat 1:15], pin will it is first up (c r Up	e, unless ente be up (Power r down), and Power 4th 5th 1st	ering BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i sequence), or dow (or down). Sleep E None None 1st	in these two wn (Power-d Exit	o states, pin is down/Sleep-ent Sleep I None None 3rd	Entry		Stat CTL 7 6 5 4	F_OSC F_NRSTIRQ us Register - Control STAT (13h) ST_WD_EN ST_VBBAT ST_NBAT ST_NRST		1 0 1 7 6 5 4	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD			EN4 EN5 EN6 EN7
Pins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the til Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3)	ne), pin maintain p e of the time slot[ime slot where 1s Power 4th 1st 1st 2nd	previous statu 1:15], pin will it is first up (c r Up V	e, unless enter be up (Power r down), and Power 4th 5th 1st 4th	ering BACKUP o r-up/Sleep-exit 15th is last up Down	r FAILSAFE state, i sequence), or dow (or down). Sleep E None None Ist 3rd	in these two wn (Power-d	o states, pin is lown/Sleep-ent Sleep I None None 3rd 2nd	pulled Low. try Entry V V V V V V V V V V V V V V V V V V V		1 0 Stat 7 6 5 4 3	F_OSC F_NRSTIRQ us Register - Control STAT (13h) ST_WD_EN ST_VBBAT ST_VBBAT ST_NIRQ ST_NRST ST_ACTSLP		1 0 1 7 6 5 4 3	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHDN			EN4 EN5 EN6 EN7
Pins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the tir Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3) 27 (EN4)	Power Power 4th 1st 2nd 2nd	previous statu (1:15], pin will it is first up (or r Up V V	e, unless ente be up (Power r down), and Power 4th 5th 1st 4th	ering BACKUP o r-up/Sleep-exit 15th is last up Down V V V	r FAILSAFE state, i t sequence), or dow (or down). Sleep E None None 1st 3rd	in these two wn (Power-d Exit V	o states, pin is lown/Sleep-ent Sleep I None 3rd 2nd Naco	Entry		1 0 Stat 7 6 5 4 3 2	F_OSC F_NRSTIRQ tus Register - Control STAT (13h) ST_WD_EN ST_WD_EN ST_VBBAT ST_NRQ ST_NRST ST_ACTSUP AT_ACTSHDN		1 0 7 6 5 4 3 2	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHDN WDT_SHDN	200		EN4 EN5 EN6 EN7 EN8
Pins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the to Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3) 22 (EN4)	he), pin maintain p of the time slot f ime slot where 1s Power 4th 1st 1st 2nd 2nd	previous stati 1:15], pin will it is first up (o r Up	e, unless enter be up (Power r down), and Power 4th 5th 1st 4th 4th	Pring BACKUP o r-up/Sleep-exit 15th is last up Down V V V V V V	r FAILSAFE state, i sequence), or dow (or down). Sleep E None None 1st 3rd None	in these two wn (Power-d	o states, pin is down/Sleep-ent Sleep I None 3rd 2nd None	Entry		Stat CTL 7 6 5 4 3 2 1:0	F_OSC F_NRSTIRQ tus Register - Control STAT (13h) ST_WD_EN ST_VBAT ST_NIRQ ST_NIRQ ST_NRST ST_ACTSUP AT_ACTSUP 00b: SHDN, Power Up/D		1 0 7 6 5 4 3 2 1:0	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHDN WDT_SHDN 00b: Normal ACT/SHD control	V pin	J	EN4 EN5 EN6 EN7 EN8
Pins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3) 22 (EN4) 23 (EN5)	he), pin maintain p of the time slot ime slot where 1s Power 4th 1st 1st 2nd 2nd 4th	revious stab 1:15, pin vill it is first up (c r Up v v v	e, unless enter be up (Power r down), and Power 4th 5th 1st 4th 4th 2nd	Down Down v v v v v v v v v	r FAILSAFE state, , t sequence), or dow (or down). Sleep E None 1st 3rd None None None	in these two wn (Power-d	o states, pin is ilown/Sleep-ent Sleep 1 None 3rd 2nd None None	Pulled Low. try Entry V V V V V V V V		Stat CTL 7 6 5 4 3 2 1:0	F_OSC F_NRSTIRQ tus Register - Control STAT (13h) ST_WD_EN ST_WD_EN ST_NIRQ ST_NIRQ ST_NIRQ ST_NIRST ST_ACTSLP AT_ACTSHDN 00b: SHDN, Power Up/D		1 0 7 6 5 4 3 2 1:0	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHDN WDT_SHDN 000: Normal ACT/SHD	N pin		EN4 EN5 EN6 EN7 EN8 EN9
Pins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the tr Pins 13 (CLK320E) 19 (EH1) 20 (EH2) 21 (EH3) 22 (EH4) 23 (EH5) 34 (EH6)	he), pin maintain p of the time slot[ime slot where 1s Power 4th 1st 1st 2nd 2nd 4th est.	revious stab 1:15, pin vill it is first up (c r Up v v v v v v v v v v v v v	e, unless enter be up (Power r down), and Power 4th 5th 1st 4th 4th 2nd 1=+	ring BACKUP o r-up/Sleep-exit 15th is last up Down V V V V V V V V	r FAILSAFE state, , t sequence), or dow (or down). Sleep E None 1st 3rd None None None	in these two wn (Power-d	o states, pin is lown/Sleep-ent None 3rd 2nd None None None	Entry Entry V V V V V V V V V V V V V		Stat Stat CTL 7 6 5 4 3 2 1 :0	F_OSC F_NRSTIRQ TUS Register - Control _STAT (13h) ST_WD_EN ST_WD_EN ST_VBBAT ST_NIRQ ST_NRST ST_NRST ST_ACTSLP AT_ACTSHDN Odb: SHDN, Power Up/D		1 0 7 6 5 4 3 2 1:0	ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHDN 00b: Normal ACT/SHD control	() ()	5	EN4 EN5 EN6 EN7 EN8 EN9

Figure 4-11. Sequence Config

frite to Hardware 🔀 Discard Changes 🛛 C Refresh All Store to NVM Restore from NVM Clear Faults Change I2C Address							
38700C Device Specific Registers							
ns Config System Config Sequence Config Watchdog Config Alarms (RTC) Config	^	Sta	tus Registers - Interrupt			Stat	tus F
WDT (80h:83h)		IN	r SRC (10h)] []	NT SRC2 (11h)	EN	ST
Disabled		7	F_INTERR 018	16	7 F_VENDOR		
On expires, first interrupt, then reset, then power-down according the Power-Down Mode		6	EM PD 013	l	5 F SDA 010	E	N1
On expires, then reset, then power-down according the Power-Down Mode		5	WDT (11)		5 RT CRC		
O On expires, power-down according the WDT_CFG.PDMD		4	PEC (TTT	HE	A RICT		
Automatic disable in sleep mode	1					E	N2
Disabled automatically in sleep mode	1	1					
U Enabled in sleep mode		2	F_EN		2 TSD	E	N3
Delay from POR (or from value written to WDT_CFG.WDTEN) to first open window		1	F_05C		1 ECC_DED 0		
Delay of 1 WDT period V × 2 ms = 2 ms		0	F_NRSTIRQ 018		PBSP 013	E	N4
Close window duration	1						
Open window duration 1 mm		Sta	tus Register - Control			E	N5
WDT period 2		СТ	L_STAT (13h)	L	AST_RST (1Ah)		
Power-Down Mode for WDT force power-down	1	7	ST_WD_EN	7	NRST		NG
Normal Act / Shuh pin control		6	ST_VBBAT	6	WDT_RST		NO
Force power-down sequence, then resume normal ACT/SHDN pin control after 1 sec delay		5	ST_NIRQ	5	NPWR_BTN		_
Force power-down sequence, then resume normal ACT/SHDN pin control when ACT/SHDN is I ow, or when RTC alarm occurs as		4	ST_NRST	4	NEM_PD	E	N7
per configuration in CTL_2, RTC_T, and RTC_A		3	ST_ACTSLP	3	ACTSHDN		
Key to reset WDT 0		2	AT_ACTSHDN	2	WDT_SHDN	E	N8
		1:0	00b: SHDN, Power Up/Down	1	control		
						E	N9
	~						
	>	< _					>
nnulon Clearlon					Tochuda po	ling activ	vitio

Figure 4-12. Watchdog Config

TEXAS INSTRUMENTS www.ti.com

00C Device Specific Registers						
onfig System Config Sequence Config Watchdog Config Alarms (RTC) Config		atus Registers - Inter	rupt			Status
Alarm		NT_SRC (10h)	OLR	INT SRC2 (11h)	OLR	EN S
) Disable Alarm	7	F_INTERR	OLR	7 F_VENDOR	OLR	
CTL_2.RTC_WAKE and CTL_2.RTC_PU are dear; RTC_A[31:0] are set to 0xFFFFFFFF.	6	EM PD	OLB	6 F SDA	0.03	ENI
) Alarm to assert NIRQ for interrupt based wake	5	WDT	6773	5 PT CPC	6073	
equal RTC_A[31:0], PSEQ interrupts MCU; MCU asserts either ACT/SLP or ACT/SHDN	3	055	0003		6223	
Autonomous wake from sleep. PSEQ ransitions from SLEEP -> ACTIVE	4	PEC	OUR	4 8151	OLR	EN
CTL_2.RTC_WAKE is set. When RTC_T[31:0] is equal RTC_A[31:0], an interrupt is asserted, INT_SRC.RTC status bit and CTL_1 ECRCE_ACT bit are set. As a result of interrupt, the processor wakes, determines rause of interrupt, deasserts ACT/SIP.	3	RTC	OLR	3 LDO	OLR	
and dars CTL_1.FORCE_ACT	2	F_EN	OLR	2 TSD	OLB	EN
Autonomous wake from shutdown. PSEQ transitions from SHDN2 ->ACTIVE	1	F_OSC	OLR	1 ECC_DED	OLR	
Requires a software shutdown and ACI (SHUN remains asserted. Processor set CI_2.PU, then set CI_1.SHUN to 11b. Ine PSEQ is forced into shutdown mode until RTC_T[31:0] is equal RTC_A[31:0], or ACT/SHDN de-asserted and re-asserted by the system.	0	F_NRSTIRQ	OLR	0 PBSP	GLR	EN
<u>RTC_A [74h:77h]</u>	St	atus Register - Contro	al l			
alue at POR = 0x00000000. Value at POR = 0xFFFFFFF		TL STAT (13h)		LAST RST (1Ah)		EN
iotal seconds 241 💭 0x000000F1 sec Total seconds 4,294,967,295 🗁 0xFFFFFFF sec	7	ST WD EN		7 NRST		
0 🗘 days 0 ⊕ h 4 ⊕ min 1 ⊕ sec 49,710 ⊕ days 6 ⊕ h 28 ⊕ min 15 ⊕ sec		ST_WD_LN		6 WDT RST		EN
	5	ST_NIDO		5 NPWR BTN		
Read Write	4	ST_NDST		4 NEM PD		EN
	3	ST ACTSUP		3 ACTSHDN		
	2	AT ACTSHDN		2 WDT SHDN		
	10	0 00b: SHDN, Power Up/	Down	1:0 00b: Normal ACT/SHDM control	l pin	EN
						EN
	× .					

Figure 4-13. Alarms Config

ile	intents - rusion Digital Pow	er bevice doi - 1	P358700C @ 000	(301), 120	Address: 1	200 (7611)								- 2 4
) Write to Hardw	vare 🛛 🗙 Discard Changes 🛛 🕻	C Refresh All St	ore to NVM Rest	ore from NVM	Clear Fa	ults Change	e I2C Address	5						
TP538700C Dev	vice Specific Registers													
<u>1 2 3 4</u>										Clear	Status	Refresh All W	rite All	
Code 👻	Register Name	= Group =	Value (Hex)	б. К			В	it Fields				Poll =		
				0	0	0	0	0	0	0	0			^
							a	LOSE						
0x81	WDT_CLOSE	WDT	0x00	7	<i>6</i>	5	4	3	2	1	<i>0</i>	Refresh	Write	
						0	U	U			0			
002	WDT ODEN	WDT	0×00				WOT	T_OPEN					Weite	
0x82	WD1_OPEN	WD1	0.00	0	Ō	0	Ū	0	0	0	0	M C Kerrean		
							wo	T_KEY						
0x83	WDT_KEY		0x00	7	6	5	4	3	2	1	0	Refresh	Write	
				0	0	0	0	0	0	0	0			
				RSVD	WRK	SEQS	SBQP	SEQC	WDT	RTC	сть			_
0xF0	PROT0	PROT	0x00	7	<i>6</i>	5	4	3	2	<i>1</i>	0	Refresh	Write	-
				RSVD	WRK	SEQS	SEQP	SEQC	WDT	RTC	сть			
0xF1	PROT1	PROT	0x00	7	6	5	4	3	2	1	0	Refresh	Write	
				0	0	0	0	0	0	0	0			~
<														
Copy Log	ClearLog												Indu	de polling activities
cion Digital Pou	wer Designer v7422 Alpha	USB Adapter v1.0	11 [DEC: 400 kH+1	TPS387000	C @ 604 (3C	b)	_		Not Sav	ed			Ja Texas Instrument	wrs I fusion digital nower

Figure 4-14. Registers



4.3 Quick Start

Follow the steps below precisely to quickly evaluate the TPS38700-Q1. In this quick start, we will be looking at Enable 1 and Enable 2 signals after the ACT pin is triggered.

- 1. Make the connections described in Section 4.1. Skip the GUI installation if the TPS38700Q1EVM GUI is already installed.
- 2. Power the EVM by turning on the power supply. Note that the voltage and current at the supply are 3.3 V and 10 mA.
- 3. Once the TI's USB Interface Adapter is connected to EVM and the laptop, launch the evaluation software Fusion Digital Power Designer.
- 4. Click on I2C GUI in the bottom right.

No Devices Found! No compatible PMBus devices were found. Please check that the serial cable end of your USB adapter is attached to your device and power is supplied to your device. Scanning Mode: DeviceIDAndCodeAndICDeviceID USB Adapter Firmware Version: 1.0.11 Bus Speed: Packet Error Checking: Bus Made: ALERT Pullup: 2.2 kΩ ∨ 0 100 kHz ● Enabled ● Serial CLOCK Pullup: 2.2 kΩ ∨ 0 400 kHz ● Disabled ● Pareitel DATA Pullup: 2.2 kΩ ∨ Signals SMBALERT#: ACK: High Refresh	Fusion Di Version 7.4.	gital P 2.2 [202	ower 0-12-21	Dəsig 1	nər		
Scanning Mode: DeviceIDAndCodeAndICDeviceID USB Adapter Firmware Version: 1.0.11 Bus Speed: Packet Error Checking: Bus Mode: ALERT Pullup: 2.2 kΩ ∨ 0 100 kHz • Enabled • Serial CLOCK Pullup: 2.2 kΩ ∨ • 400 kHz • Disabled • Parallel DATA Pullup: 2.2 kΩ ∨ Signals SMBALERT#: ACK: High Refresh	No Devices Fo	devices were	found. Pleas	se check tha	it the serial cable	e end of your USB adapter	r is attached to your device and
USB Adapter Firmware Version: 1.0.11 Bus Speed: Packet Error Checking: Bus Mode: ALERT Pullup: 2.2 kΩ ♥ ○ 100 kHz ○ Enabled ○ Serial CLOCK Pullup: 2.2 kΩ ♥ ○ 400 kHz ○ Disabled ○ Paraitel DATA Pullup: 2.2 kΩ ♥ Signals SMBALERT#: ACK: High Refresh	Scanning Mode:	DeviceI	DAndCode	AndICDe	viceID		
Bus Speed: Packet Error Checking: Bus Mode: ALERT Pullup: 2.2 kΩ ♥ 0 100 kHz ● Enabled ● Beribit CLOCK Pullup: 2.2 kΩ ♥ ● 400 kHz ● Disabled ● Parallel DATA Pullup: 2.2 kΩ ♥ Signals SMBALERT#: ACK: High Refresh ■	USB Adapter Firr	mware Versi	ion: 1.0.1	1			
○ 100 kHz ● Enabled ● Gerial CLOCK Pullup: 2.2 kΩ ∨ ● #00 kHz ● Disabled ● Parallel DATA Pullup: 2.2 kΩ ∨ Signals SMBALERT#: ACK: High Refresh	Bus Speed:	Packet Er	rror Checki	ng:		ALERT Pullup:	2.2 kΩ 🗸
O HOO KHZ O Disabled O Parallel DATA Pullup: 2.2 kΩ ✓ Signals SMBALERT#: ACK: High Refresh	🔾 100 kHz	Enable	ed		•) Serial	CLOCK Pullup:	2.2 kΩ 🗸
Signals SMBALERT#: ACK: High Refresh	• 400 kHz	🔿 Disabl	led			DATA Pullup:	2.2 kΩ 🗸
34 14 24 24 24	SMBALERT#:	ACK: High	(Refres	h		
Control Lines: "1 "2 "3 "4 "5	Control Lines:	#1	#2	#3	#4	#5	
(dick to set) High High High High Refresh All	(dick to set)	OHigh	OHigh) High	O High	OHigh	Refresh All

Figure 4-15. Fusion Welcome Window

5. Click on Change Scan Mode to select TPS38700x and then click OK.

👆 Texas Instruments - Fusion I	igital Power Designer				. • 🗙
File Tools					
Q Skip scanning for all Change S	an Mode Start Polling	Polling Interval	1000 ms		
# Address △ D	evice				
Log					
Timestamp	Message				
Copy Log Clear Log					Include poling activities
Fusion Digital Power Designer v7.6.	5.Beta No Adapter			Not Saved	TEXAS INSTRUMENTS fusion digital power



🤣 Texas Instr		_ _ X
File Tools		
Q Skip scanning	g for all Change Starn Mode ▶ Start Polling Polling Interval 1000 ms	
# Addre	Set All Addresses To: Skip TPS535x0/63831 TPS596xx TPS38700x XPS53830 TPS542A40 TPS54xC2x Allow address zero	
	1d 0x01 TF533700x V 18d 0x12 TF533700x V 50d 0x22 TF533700x V 666 0x42	TPS38700x
	24 0x02 IPS38700x	TPS38700x TPS38700x
	4d 0x.04 TPS38700x ✓ 21d 0x.15 TPS38700x ✓ 37d 0x.25 TPS38700x ✓ 53d 0x.35 TPS38700x ✓ 69d 0x.45	TPS38700x
	5d 0x05 TF538700x 🕑 22d 0x16 TF538700x 💟 38d 0x26 TF538700x 💟 54d 0x36 TF538700x 💟 70d 0x46	TPS38700x
	6d 0x06 TPS38700x V 23d 0x17 TPS38700x V 39d 0x27 TPS38700x V 55d 0x37 TPS38700x V 71d 0x47	TPS38700x
	7d 0x07 11538700x ♥ 24d 0x18 11538700x ♥ 40d 0x28 11538700x ♥ 56d 0x38 11538700x ♥ 72d 0x48	TPS38700x =
Log	9d 0x09 TFS38700x V 26d 0x1A TFS38700x V 42d 0x2A TFS38700x V 58d 0x3A TFS38700x V 74d 0x4A	TPS38700x
Timestamp	10d 0x0A TPS38700x 🗸 27d 0x18 TPS38700x V 43d 0x28 TPS38700x V 59d 0x38 TPS38700x V 75d 0x48	TPS38700x
These arrives	11d 0x06 TF533700x V 28d 0x1C TF533700x V 44d 0x2C TF533700x V 60d 0x3C TF533700x V 76d 0x4C	TPS38700x
	138 UNUU IN-SARJUUK V 298 UNUU IN-SARJUUK V 458 UNUX V 518 UNUU IN-SARJUUK V 778 UNEU 146 UNUE ITESSR700K V 306 UNUE ITESSR700K V 466 UNUE ITESSR700K V 528 UNUE ITESSR700K V 786 UNUE	TPS38700x
	15d 0x.0F TFS38700x ♀ 31d 0x.1F TFS38700x ♀ 47d 0x.2F TFS38700x ♀ 63d 0x.3F TFS38700x ♀ 79d 0x.4F	TPS38700x
	16d 0x10 TFS38700x 🗸 32d 0x20 TFS38700x 🗸 48d 0x30 TFS38700x 🗸 64d 0x40 TFS38700x 🔽 80d 0x50	TPS38700x
	17d 0x11 TFS33700x	TPS38700x
	ОК	1
Copy Log	ClearLog	Include polling activities
Fusion Digital Po	vover Designer v7.66.Beta No Adapter	Texas Instruments fusion digital power

Figure 4-17. Fusion Scan Selection Window



6. Scan for the TPS38700Q1EVM by clicking on "Scan for TPS38700x" on top left of the window.

👆 Texas Instrum	s - Fusion Digital Power Designer	. •
File Tools		
Q Scan for TPS3870	Change Scan Mode Start Polling Polling Interval 1000 ms	
# Address	△ Device	
(1		
Log		_
l i		
Timestamp	Message	
13:09:13.249	SetPullUps (Alert: 2.2 kΩ; Clock: 2.2 kΩ; Data: 2.2 kΩ): ACK	
13:09:13.344	SetPedMode (PEC): ACK	
13:09:13.365	SetBusSpeed (Speed400KHz): ACK	

Figure 4-18. Fusion Scan Window - Scanning for TPS38700Q1EVM

7. Once the EVM is discovered, select Click to Configure (text in blue).

🕀 Te	cas Instruments	- Fusion	Digital Powe	r Designer							_ ē 🔀
File	Tools										
Q, Sca	n for TPS38700x	Change	Scan Mode	Start Polling	Polling Intervi	al	1000 r	ns			
#	Address	۵	Device								
	1 3Ch (60d)	1	TPS38700C							Click to Configure	
Log											
							_	_			
Times	tamp		Message								
13:20	:10.132		Scanning US	B Adapter #1 at	address 121d (T	PS38700x) fa	r device	s			
13:20	:10.196		I2CRead (Ad	ldress 121d, Cm	d 0x01): NACK <	empty>					
13:20	:10.252		Scanning US	B Adapter #1 at	address 122d (T	PS38700x) fo	r device	s			
13:20	:10.303		I2CRead (Ad	ldress 122d, Cm	d 0x01): NACK <	empty>					
13:20	:10.356		Scanning US	B Adapter #1 at	address 123d (T	PS38700x) fo	r device	s			
13:20	:10.411		I2CRead (Ad	ldress 123d, Cm	d 0x01): NACK <	empty>					
13:20	:10.471		Scanning US	B Adapter #1 at	address 124d (T	PS38700x) fo	r device	s			
13:20	:10.524		I2CRead (Ad	ldress 124d, Cm	d 0x01): NACK <	empty>					
13:20	:10.580		Scanning US	B Adapter #1 at	address 125d (T	PS38700x) fa	r device	s			
13:20	:10.633		I2CRead (Ad	ldress 125d, Cm	d 0x01): NACK <	empty>					
13:20	:10.694		Scanning US	B Adapter #1 at	address 126d (T	PS38700x) fa	r device	s			
13:20	:10.753		I2CRead (Ad	ldress 126d, Cm	d 0x01): NACK <	empty>					-
13:20	:10.801		Found 1 dev	ice.							~
Cop	oy Log Clear	Log									Include polling activities
Eurion	Digital Rower Dec	ioner v7	1.2.2 Alpha	ISP Adapter v1	0.11 (BEC: 400)	au an l		_	Net Court	Ja Towas by	munum the fusion digital namor

Figure 4-19. Fusion Scan Window - Scan for TPS38700Q1EVM Completed



8. Go to the Sequence Config tab. In the Pins mapping section, change the pin 19's (EN1) Power Up sequence from 1st to 4th sequence. Now, the Enable 1 signal is part of the 4th power-up sequence. Hence, delaying the signal by about 2 ms from Enable 2 signal (which is still part of the first power-up sequence).

					onean radits	onange izo A					_			_
700C Device Specific	Registers							uk:						
Config System Config	Sequence Config	Watchdog Confi	Alarms (RTC) Co	onfig				^ Sta	atus Registers - Inte	rrupt				State
ime Config ———								IN	IT_SRC (10h)	OLR	IN	T SRC2 (11h)	OLR	EN S
250 🗸								7	F_INTERR	OLR	7	F_VENDOR	CLR	
Time slot between sequ	uencing points = 1	IME[7:0] * SSTEP	+ T_min, where T	_min = 125 µs				6	EM_PD	OLR	6	F_SDA	CL8	EN
	TIME[7:0]	Min (-6%)	Typical	Max (+6%)				5	WDT	OLR	5	RT_CRC	OLE	
Power-up / Sleep-exit	t 2 🗧	587.5	625.0 💭	662.5 µ	JS			4	PEC	013	4	BIST	OLK	EN
Power-down / Sleep-e	entry 2	587.5	625.0 💭	662.5 µ	JS			3	RTC	018	3	LDO	GUR	
								2	F_EN	OLE	2	TSD	OLR	EN
ins mapping If Pin not mapped (Non	ne), pin maintain pr	evious state, unle	ss entering BACKU	P or FAILSAFE stat	e, in these two	o states, pin is	pulled Low.	2	F_EN F_OSC	OLR OLR	2	TSD ECC_DED		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti	ne), pin maintain pr e of the time slot[1: ime slot where 1st i	evious state, unle 15], pin will be up s first up (or dowr	ss entering BACKU (Power-up/Sleep-(n), and 15th is last	P or FAILSAFE stat exit sequence), or o up (or down).	e, in these two down (Power-c	o states, pin is down/Sleep-en	pulled Low. try	2	F_EN F_OSC F_NRSTIRQ	618 618 618	2 1 0	TSD ECC_DED PBSP		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins	ne), pin maintain pr e of the time slot[1: ime slot where 1st i Power I	evious state, unle 15], pin will be up s first up (or down	ss entering BACKU (Power-up/Sleep-(n), and 15th is last Power Down	P or FAILSAFE state exit sequence), or o up (or down). Slee	e, in these two down (Power-c p Exit	o states, pin is down/Sleep-en Sleep	pulled Low. try Entry	2 1 0 Sta	F_EN F_OSC F_NRSTIRQ atus Register - Cont	618 618 618	2 1 0	TSD ECC_DED PBSP		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E)	ne), pin maintain pr e of the time slot[1: ime slot where 1st i Power (4th	evious state, unle 15], pin will be up s first up (or down Jp	ss entering BACKU (Power-up/Sleep-d)), and 15th is last Power Down	P or FAILSAFE state exit sequence), or o up (or down).	e, in these two down (Power-c p Exit	o states, pin is down/Sleep-en Sleep None	pulled Low. try Entry	2 1 0 Sta	F_EN F_OSC F_NRSTIRQ atus Register - Cont TL_STAT (13h)	rol	2 1 0	TSD ECC_DED PBSP ST_RST (1Ah)		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 10 (CH1)	e of the time slot[1: ime slot where 1st i Power I 4th	evious state, unle 15], pin will be up s first up (or down Jp 1 V 4th	ss entering BACKU (Power-up/Sleep-t-), and 15th is last Power Down	P or FAILSAFE state exit sequence), or o up (or down).	e, in these two down (Power-c p Exit	o states, pin is down/Sleep-en Sleep None	pulled Low. try Entry	2 1 0 5tt 7 6	F_EN F_OSC F_NRSTIRQ atus Register - Cont TSTAT (13h) ST_WD_EN ST_VBBAT	rol	2 1 0 LA 7 6	TSD ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1)	he), pin maintain pro e of the time slot[1: ime slot where 1st i Power 1 4th 1st	evious state, unle 15], pin will be up s first up (or down yp v 4th v 5th	ss entering BACKU (Power-up/Sleep-d), and 15th is last Power Down	P or FAILSAFE state exit sequence), or o up (or down). Sleep None	e, in these two down (Power-c p Exit	o states, pin is down/Sleep-en Sleep None None	pulled Low. try Entry	2 1 0 5 1 7 6 5	F_EN F_OSC F_NRSTIRQ TL_STAT (13h) ST_WD_EN ST_VBBAT ST_NIRQ	rol	2 1 0 1 7 6 5	TSD ECC_DED PBSP ST_RST (1Ah) INRST WDT_RST NPWR_BTN		EN
ins mapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1) 20 (EN2)	he), pin maintain pr e of the time slot[1: me slot where 1st i Power I 4th 1st 1st	evious state, unle 15), pin will be up s first up (or down Jp I V 4th V 5th V 1 sth	ss entering BACRU (Power-up/Sleep-4), and 15th is last Power Down V V	P or FAILSAFE stati exit sequence), or o up (or down). Siece; None Ist	e, in these two down (Power-c p Exit	o states, pin is down/Sleep-en Sleep None None 3rd	pulled Low. try Entry V	2 1 0 Sta 5 4	F_EN F_OSC F_NRSTIRQ TL_STAT (13h) ST_WD_EN ST_VBBAT ST_NBRA ST_NBRA ST_NRST	rol	2 1 0 7 6 5 4	TSD ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD		EN EN EN EN
In smapping If Pin not mapped (Nor If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3)	he), pin maintain pr e of the time slot[1: me slot where 1st i Power I 4th 1st 1st 1st 2nd	evious state, unle 15j, pin will be up s first up (or down Jp I V 4th V 5th V 1st	ss entering BACKU (Power-up/Sleep-4 n), and 15th is last Power Down V V V	P or FAILSAFE state exit sequence), or d up (or down). None None Ist 3rd	p Exit	o states, pin is down/Sleep-en Sleep None None 3rd 2nd	pulled Low. try Entry V V	2 1 0 5 5 4 3	F_EN F_OSC F_NRSTIRQ atus Register - Cont TL_STAT (13h) ST_WD_EN ST_VBBAT ST_NIRQ ST_NIRQ ST_NRST ST_ACTSLP	rol	2 1 0 7 6 5 4 3	TSD ECC_DED PBSP ST_RST (1Ah) NRST WDT_RST NPWR, BTN NEM_PD ACTSHON NMT_CONT		EN EN EN EN
Ins mapping If Pin not mapped (Non If Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EII1) 20 (EII2) 21 (EII3) 22 (EII4)	he), pin maintain pr of the time slot[1: me slot where 1st i 4th 1st 1st 2nd 2nd	evious state, unle 15), pin will be up s first up (or down 1p 4th V 5th V 1st V 4th V 4th V 4th	ss entering BACKU (Power-up/Sleep-4)), and 15th is last Power Down V V V V	P or FAILSAFE state exit sequence), or d up (or down). None None Ist 3rd None	e, in these two down (Power-o p Exit	o states, pin is down/Sleep-en None None 3rd 2nd None	pulled Low. try Entry V V	2 1 0 5 5 7 6 5 4 3 3 2 1 1	F_EN F_OSC F_NRSTIRQ atus Register - Cont fL_STAT (13h) ST_WD_EN ST_VBBAT ST_NIRQ ST_NIRQ ST_NIRT ST_NIRT ST_ACTSLIP AT_ACTSLID AT_ACTSLID	rol	2 1 0 7 6 5 4 3 2 1:0	TSD ECC_DED PBSP ST_RST (1Ah) IRRST WDT_RST NPWR_BTN NPWR_BTN NEMP ACTSHON NOT_NORNALCT/SPEND		EN EN EN EN
Its mapping It Pin not mapped (Nor It Pin is mapped to one sequence) within the ti Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3) 22 (EN4) 23 (EN5)	he), pin maintain pr e of the time slot[1: me slot where 1st Power 1 4th 1st 1st 2nd 2nd 4th	evious state, unle 15), pin will be up s first up (or down 1p 4th V 5th V 1st V 4th V 4th V 2nc	ss entering BACRU (Power up/Skep- n), and 15th is last Power Down V V V V V V	P or FAILSAFE state exit sequence), or o up (or down). None Ist Ist Ist Ist None	e, in these two down (Power-o p Exit V V V V	o states, pin is down/Sleep-en None None 3rd 2nd None	pulled Low. try Entry V V V	2 1 0 7 7 6 5 4 3 2 1:0	F_EN F_OSC F_NRSTIRQ tus Register - Cont T_STAT (13h) ST_WD_EN ST_NRQ ST_NRQ ST_NRQ ST_NRQ ST_NRQ ST_NRQ ST_NRQ ST_NRQ ST_ACTSUP AT_ACTSUP AT_ACTSUP	rol	2 1 0 7 6 5 4 3 2 1:0	TSD ECC_DED PBSP ST_RST (1Ah) NRRST WDT_RST NPWR_BTN NEM_BTN NEM_PD ACTSHDN WDT_SHDN 00b: Normal ACT/SHDN prototor		EN EN EN EN EN
Ins mapping	he), pin maintain pr e of the time slot[1: me slot where 1st 4th 1st 1st 2nd 4th 4th	evious state, unle 15), pin will be up s first up (or down y 4th v 5th v 1 sth v 1 sth v 1 sth v 4th v 2 nct	ss entering BACRU (Power up/Skep- n), and 15th is last V V V V V V V	P or FAILSAFE state exit sequence), or o up (or down). None Ist Ist Ist Ist Ist None	e, in these two down (Power-c p Exit V V V V	o states, pin is down/Sleep-en None None 3rd 2nd None None	pulled Low. by Entry V V V V	2 1 0 5 5 4 3 2 1:0 7 7 6 5 4 3 2 1:0	F_EN F_OSC F_NRSTIRQ tutus Register - Cont T_STAT (13h) ST_WD_EN ST_VBBAT ST_NIRQ ST_NIRQ ST_NIRQ ST_NIRQ ST_NIRT ST_ACTSHDN AT_ACTSHDN 000b: SHDN, Power U	rol	2 1 0 7 6 5 4 3 2 1:0	TSD ECC_DED PBSP ST_RST (1Ah) HRST WDT_RST NEH_PD ACTSHDN WDT_SHDN 00b: Normal ACT/SHDN p control		EN EN EN EN EN

Figure 4-20. TPS38700 GUI Window - Sequence Config Tab

- 9. Change the trigger in the oscilloscope from channel 1 to channel 3 to get the trigger from ACT pin.
- 10. Set the Function Generator to create a 3.3 V pulse waveform. Turn-on the output from the Function Generator connected to the ACT pin to trigger the power-up sequence.
- 11. The output at the oscilloscope should look like the Figure 4-21 where green waveform is the pulse to the ACT pin (TP6), red waveform is Enable 2 signal and blue waveform is the Enable 1 Signal.



Figure 4-21. Expected Output Signal

5 Revision History

Changes from Revision * (July 2021) to Revision A (April 2022)

Page



•	First public release	.19
•	Edited the Main GUI Screen image to reflect the new TPS38700-Q1 package pinout	25

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