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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E35RC-FW115-N

Overview:

- 3.5-inch TFT: 480x640 (64x85)
- 2-lane MIPI Interface
- DSI
- Wide View
- White LED back-light
- Transflective/ Normally Black
- No Touch Panel
- 115 NITS
- Controller: HX8363-A
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transflective type TFT-LCD Panel, driver circuit and back-light unit. The resolution of a 3.5" TFT-LCD contains 480x640 pixels and can display up to 65K/262K/16.7M colors.

Features

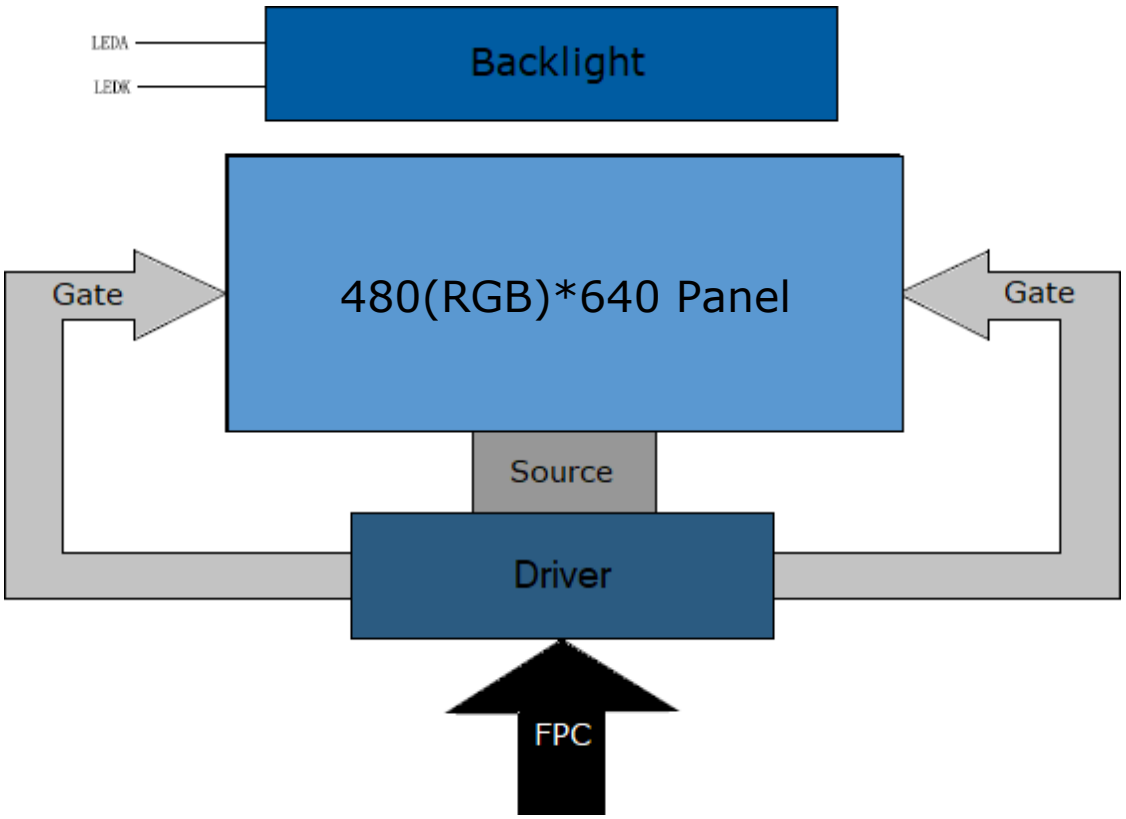
Low Input Voltage: 3.3V (TYP)
Display Colors of TFT LCD: 65K/262K/16.7M colors
Interface: 2-lane MIPI Interfaces

General Information Items	Specification Main Panel	Unit	Note
Display area (AA)	53.57(H) *71.42(V) (3.5 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*640	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1116 (H) x 0.1116 (V)	mm	-
Viewing angle	Wide angle	o'clock	-
TFT Controller IC	HX8363-A	-	-
Display mode	Transflective/Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

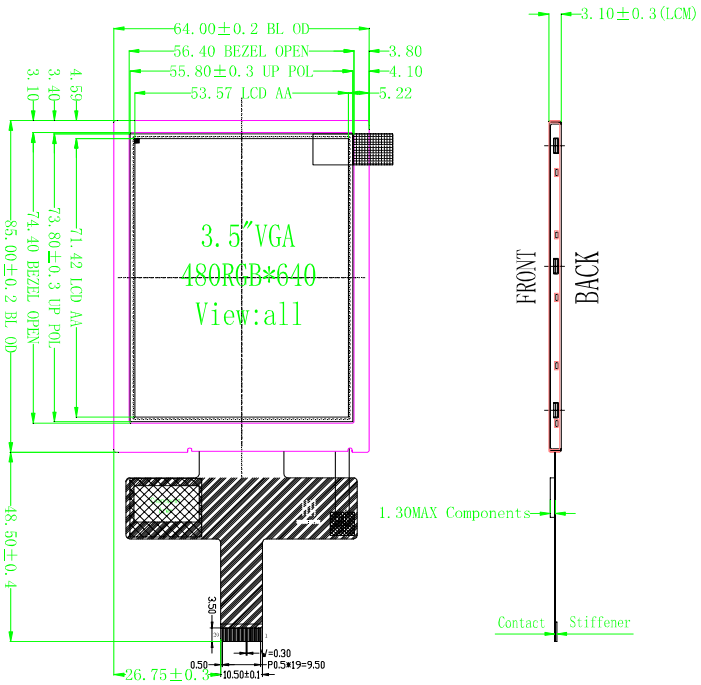
Mechanical Information

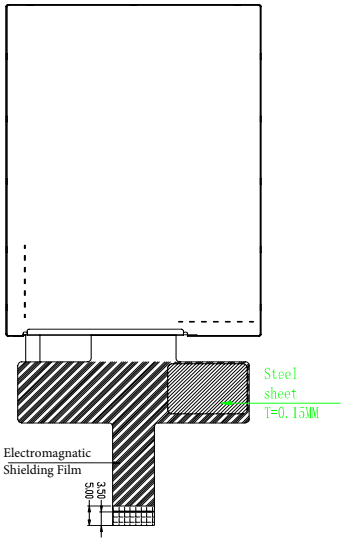
Item		Min	Typ.	Max	Unit	Note
Module size	Horizontal(H)		64.00		mm	-
	Vertical(V)		85.00		mm	-
	Depth(D)		3.10		mm	-
Weight			TBD		g	-

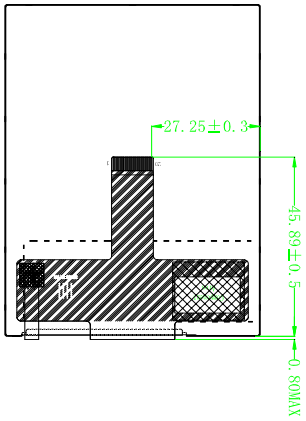
1. Block Diagram



ReV.	Revision content description	Date
A	FIRST	2018.01.03







NO.	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VCI
7	IOVCC
8	NC
9	RESET
10	GND
11	MIPI_D1P
12	MIPI_D1N
13	GND
14	MIPI_CLP
15	MIPI_CLN
16	GND
17	MIPI_D0P
18	MIPI_D0N
19	GND
20	GND

NOTES:

1. DISPLAY TYPE: 3.5", TFT-LCD, AIFF TRANSFLECTIVE
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION: WIDE VIEWING
4. DRIVER IC: HX8363-A (COG)
5. VCI 3.3V(TYP),IOVCC=1.65-3.3V
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 6 LED, 20mA, 18.6±0.3V
8. RoHS COMPLIANT.

B/L Circuit

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TOLERANCE( )	DRAWING NAME	E35RC-FW115-N	
	PARTS NO.		
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn		Unit
	Checked		mm
Scale 1:1	Approve		Page 1/1

3. Input Terminal Pin Assignment

Recommended Connector: FH19C-20S-0.5SH(10)

NO.	Symbol	Description	I/O
1	NC	NC	--
2	LEDK	Cathode pin of the backlight.	P
3	NC	NC	--
4	LEDA	Anode pin of the backlight.	P
5	NC	NC	--
6	VCI	Supply voltage (3.3V)	P
7	IOVCC	I/O power supply voltage (1.65-3.3V)	P
8	NC	NC	--
9	RESET	External reset input. Initializes chip with low input. Execute power-on reset after supplying power.	I
10	GND	Ground	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-). Leave pin open when not used.	I/O
12	MIPI_D1N		
13	GND	Ground	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK +/-). Leave pin open when not used.	I
15	MIPI_CLN		
16	GND	Ground	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn +/-). Leave pin open when not used.	I/O
18	MIPI_D0N		
19	GND	Ground	P
20	GND	Ground	P

4. LCD Optical Characteristics

4.1 Transmissive mode

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	-	300	--		(2)
Response time	Rising+ Falling	TR+TF		--	30	50	msec	(4)
Color gamut		S (%)		--	60	--	%	(5)
Color Filter Chromaticity	White	W_X		0.248	0.288	0.308		(5)(1)
		W_Y		0.272	0.312	0.332		
	Red	R_X		0.425	0.465	0.505		
		R_Y		0.286	0.326	0.366		
	Green	G_X		0.277	0.317	0.357		
		G_Y		0.458	0.498	0.538		
	Blue	B_X		0.135	0.175	0.215		
		B_Y		0.075	0.115	0.155		
Viewing angle	Hor.	ΘL	CR>10	60	80	--	Deg	(1)(6)
		ΘR		60	80	--		
	Ver.	ΘU		60	80	--		
		ΘD		60	80	--		
Option View Direction		Wide angle						

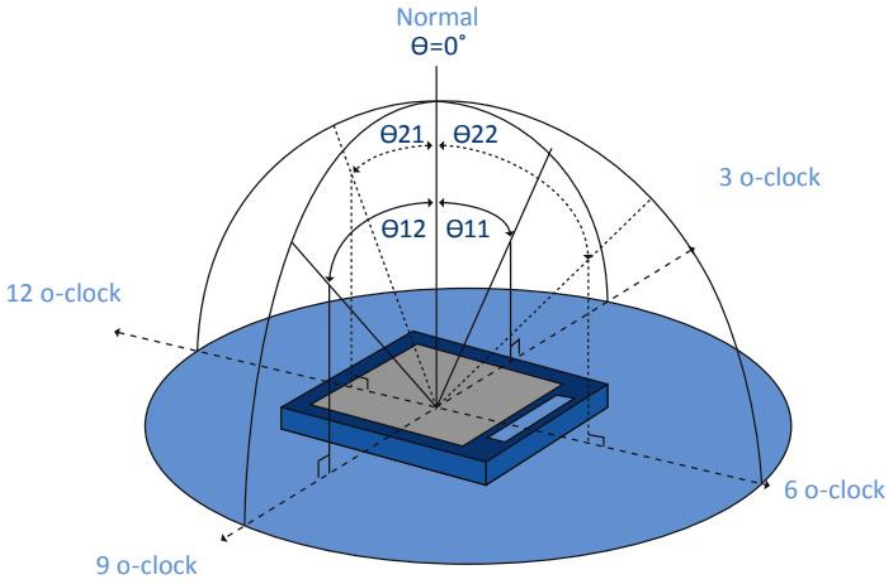
4.2 Reflective mode

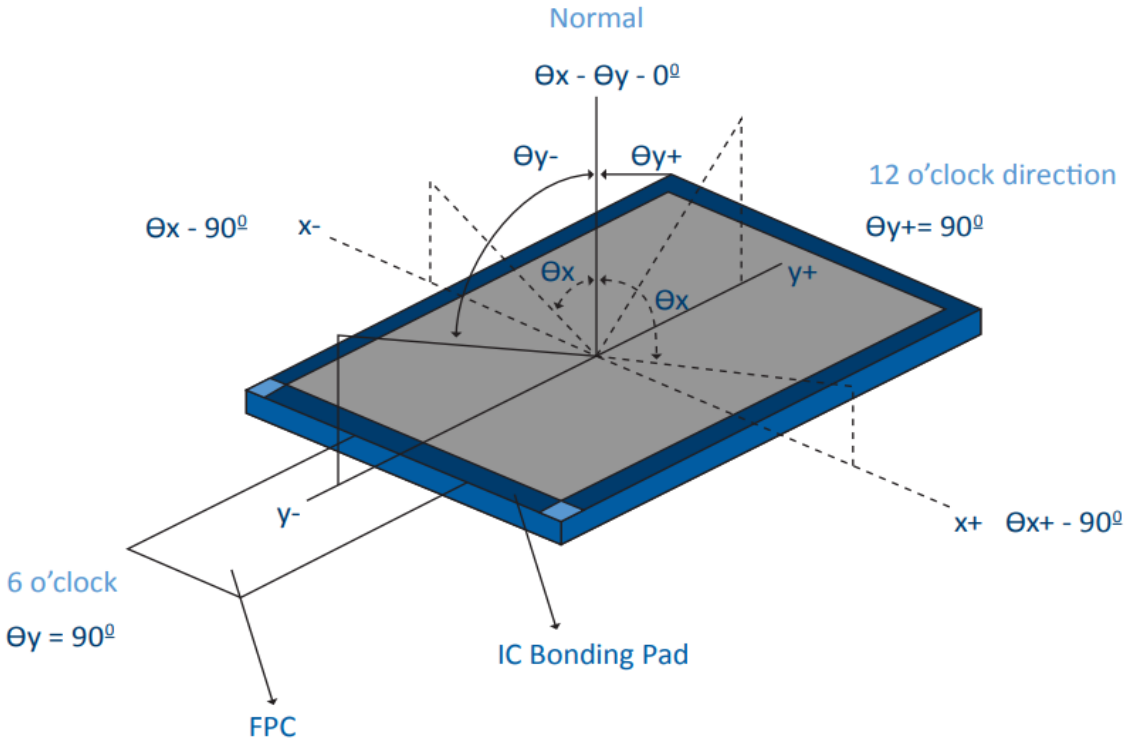
Item	Symbol	Min	Typ.	Max	Unit	Note
Reflection Ratio (with polarizer)	R (θ = ϕ = 0°)	-	7	-	%	(3)
Reflective Contrast Ratio	Cr = 0°	-	20	-		(3)
Viewing Angle (Cr ≥ 2)*	Θ21	-	45	-	deg	(1)(2)
	Θ22	-	45	-		
	Θ12	-	45	-		
	Θ11	-	45	-		

Measuring Conditions: dark room Ambient temperature: 25 ± 2℃ 15min. warm-up time

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

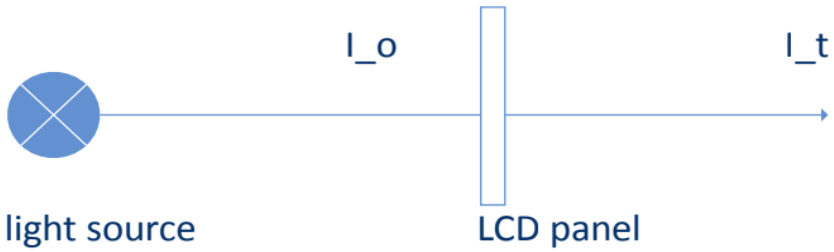




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

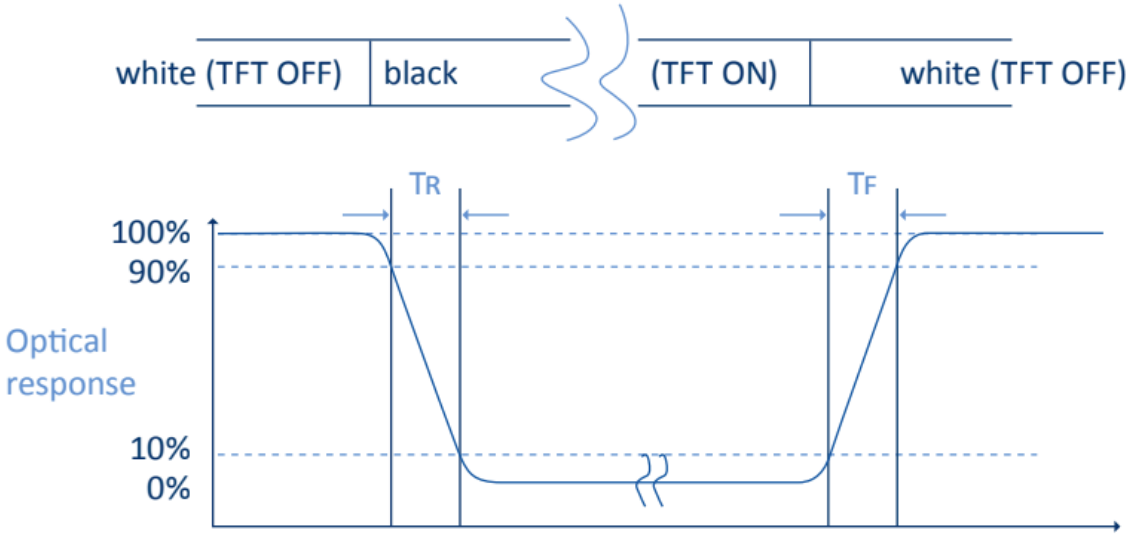


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

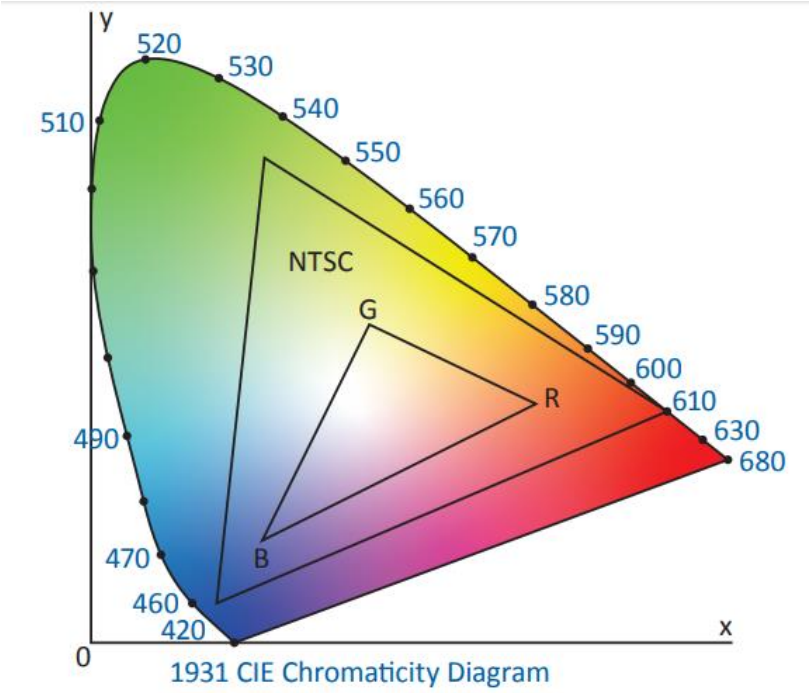
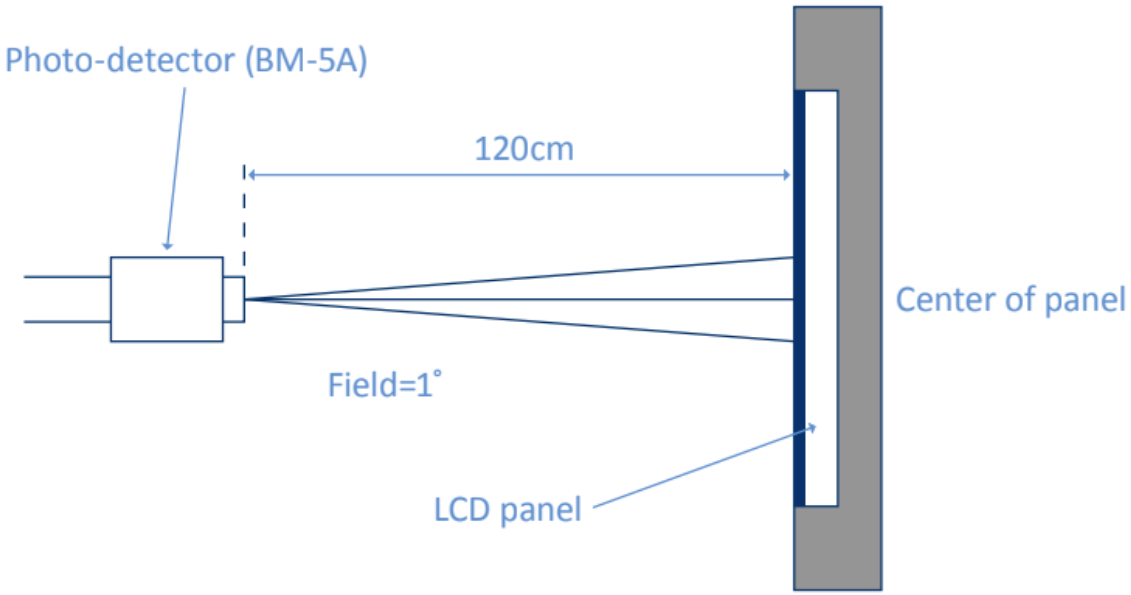


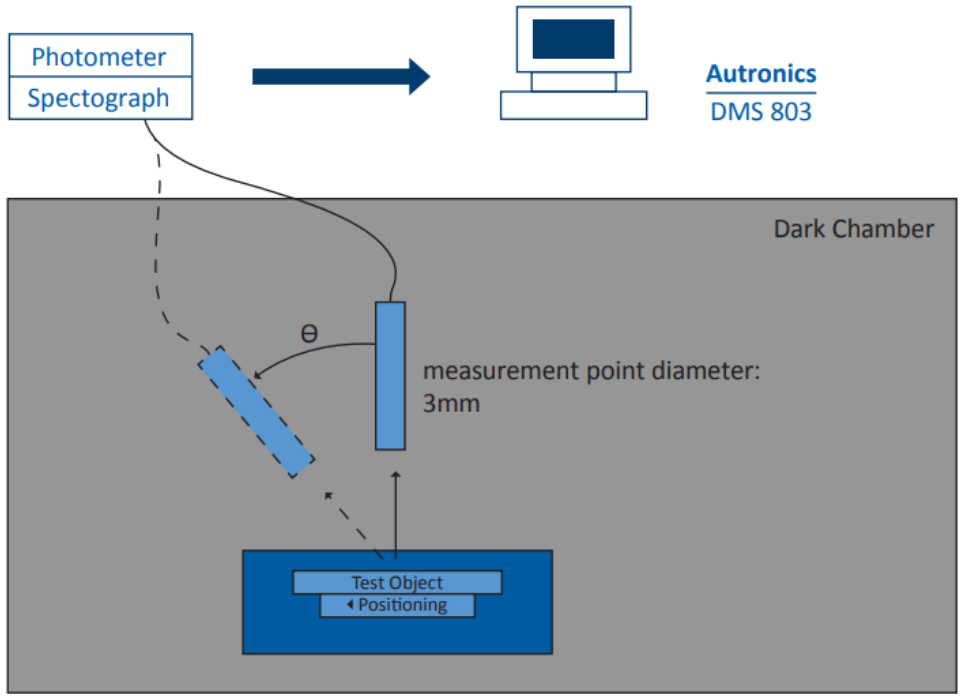
Fig. 1931 CIE chromacity diagram

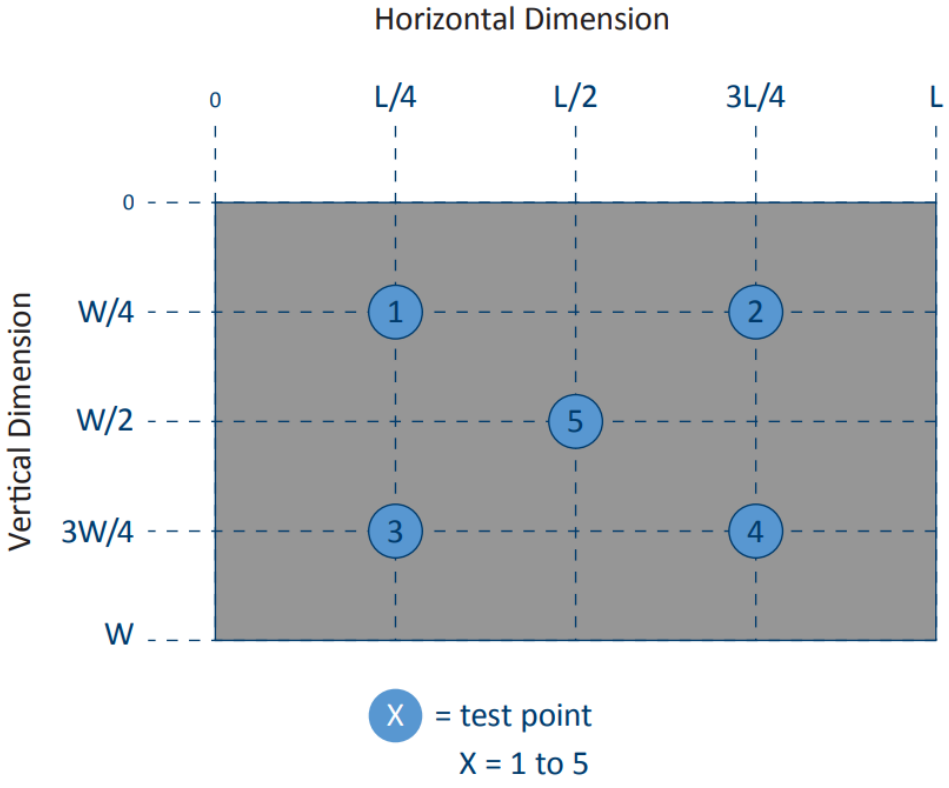
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Interface Operation Voltage	VDDIO	-0.3	4.6	V
Operating temperature	TOP	-20	+70	℃
Storage temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	
Interface Operation Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current Consumption	IDD	--	13	--	mA	
Level input voltage	VIH	0.7 IOVCC		IOVCC	V	
	VIL	-0.3		0.3 IOVCC	V	
Level output voltage	VOH	0.8 IOVCC		IOVCC	V	
	VOL	GND		0.2 IOVCC	V	

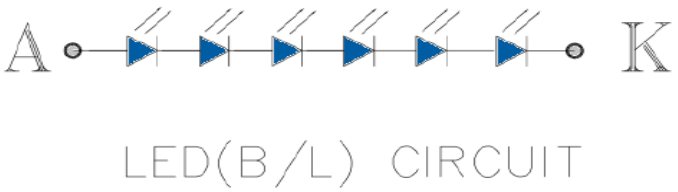
5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	15	20	--	mA	
Forward Voltage	VF	--	18.6	--	V	
LCM Luminance	LV	--	115	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

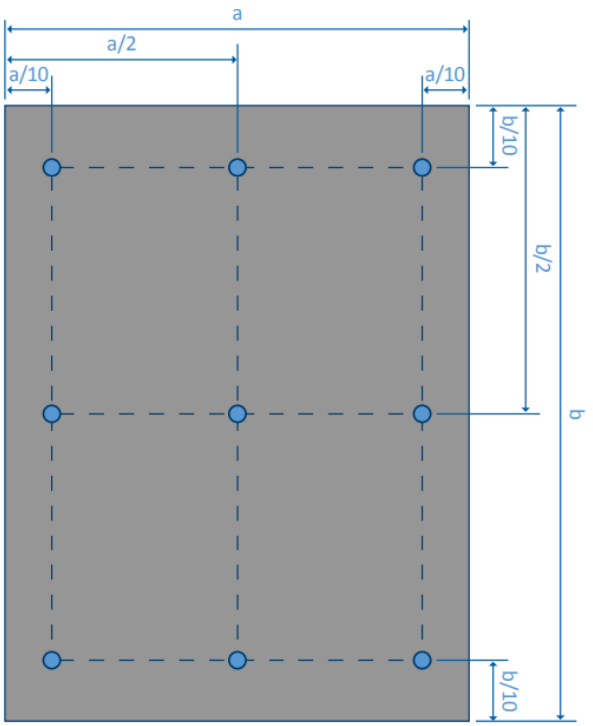
The back-light system is edge-lighting type with 6 chips White LED

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Note 3: Luminance Uniformity of these 9 points is defined as below:



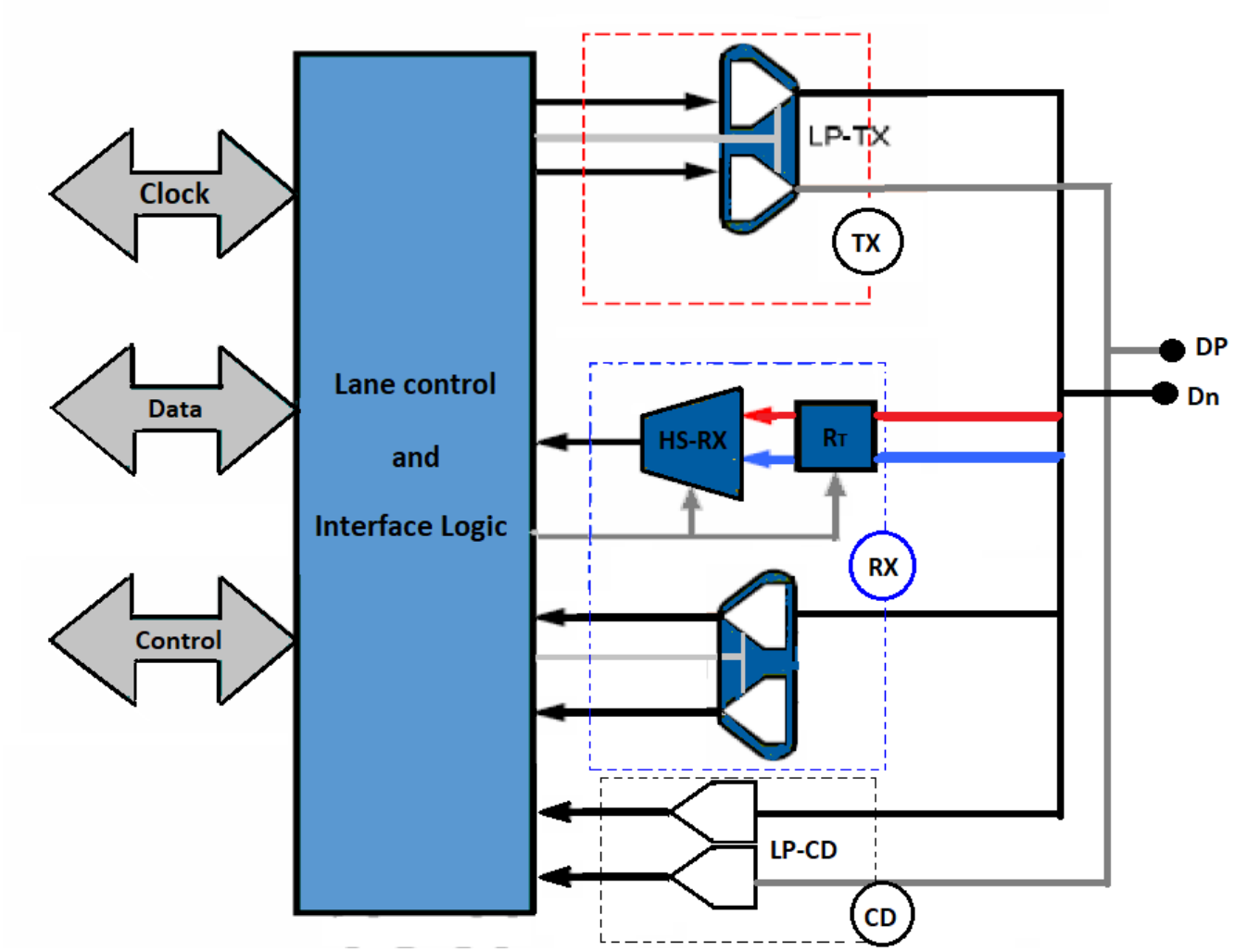
$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

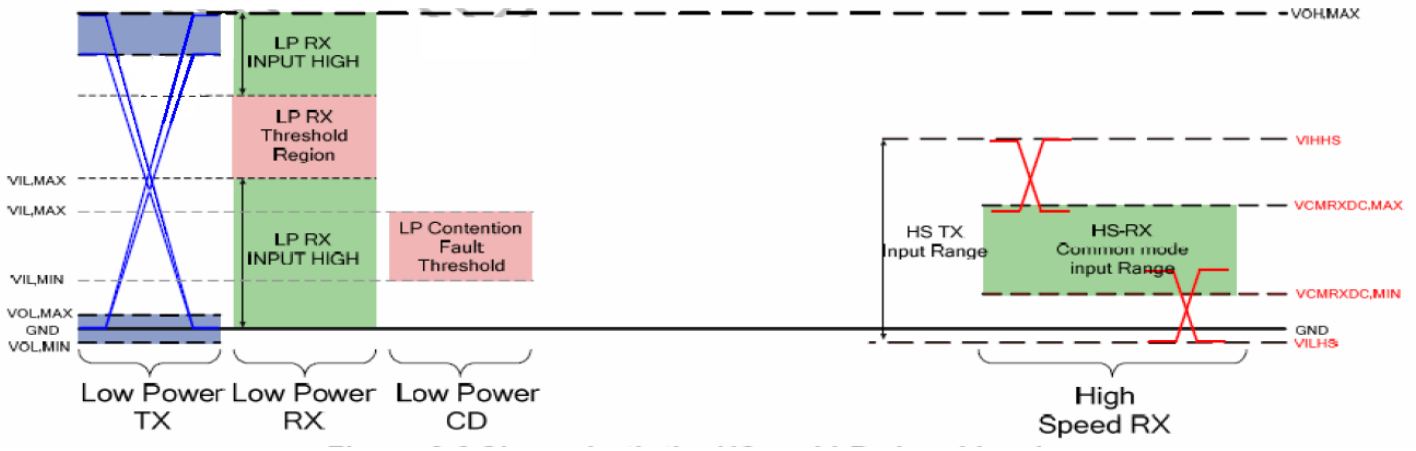
6. MIPI Interface Characteristics

6.1 Electrical Characteristics of D-PHY Layer

In general, the DSI-PHY may contain the following electrical functions: High-speed receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-power Receiver (LP-RX) and the Low-power Contention Detector (LP-CD). The figure below shows the complete set of electrical functions required for a fully featured PHY transceiver.



Where the HS receiver utilizes low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The figure shows both the HS and LP signal levels on the left and right sides, respectively. Because the HS signaling levels are below the LP low -level input threshold, the lane switches between low-power and high-speed mode during normal operation.



6.2 The Electrical Characteristics of Low-Power Transmitter

The low power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the lines in all low power operating modes. It is important that the static power consumption of a LP transmitter be as low as possible. The following tables list the AC and DC characteristics for LP-TX.

Parameter	Description	Min	Nom	Max	Units	Note
V_{OL}	Thevenin output low level	-50		50	mV	
V_{OH}	Thevenin output high level	1.1		1.3	V	
Z_{OLP}	Output impedance of LP-TX	110			Ω	1

Note:

1. Though no maximum value for Z_{OLP} is specified the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Parameter	Description	Min	Nom	Max	Units	Note
t_{RLP}/t_{FLP}	15%-85% rise and fall time			25	ns	1, 4
$\delta V/\delta t_{SR}$	Slew rate	30		500	mV/ns	1, 2, 3, 4
C_{LOAD}	Load capacitance			70	pF	

Note:

1. When the output is loaded with a capacitive load C_{LOAD}.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50mV segment of the output signal transition.
4. The slew rate δV/δtSR is the derivative of the LP transmitter output signal voltage.

6.3 High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, Z_{ID}, between the positive input pin Dp and the negative input pin Dn. The following tables list the AC and DC characteristics for HS-RX.

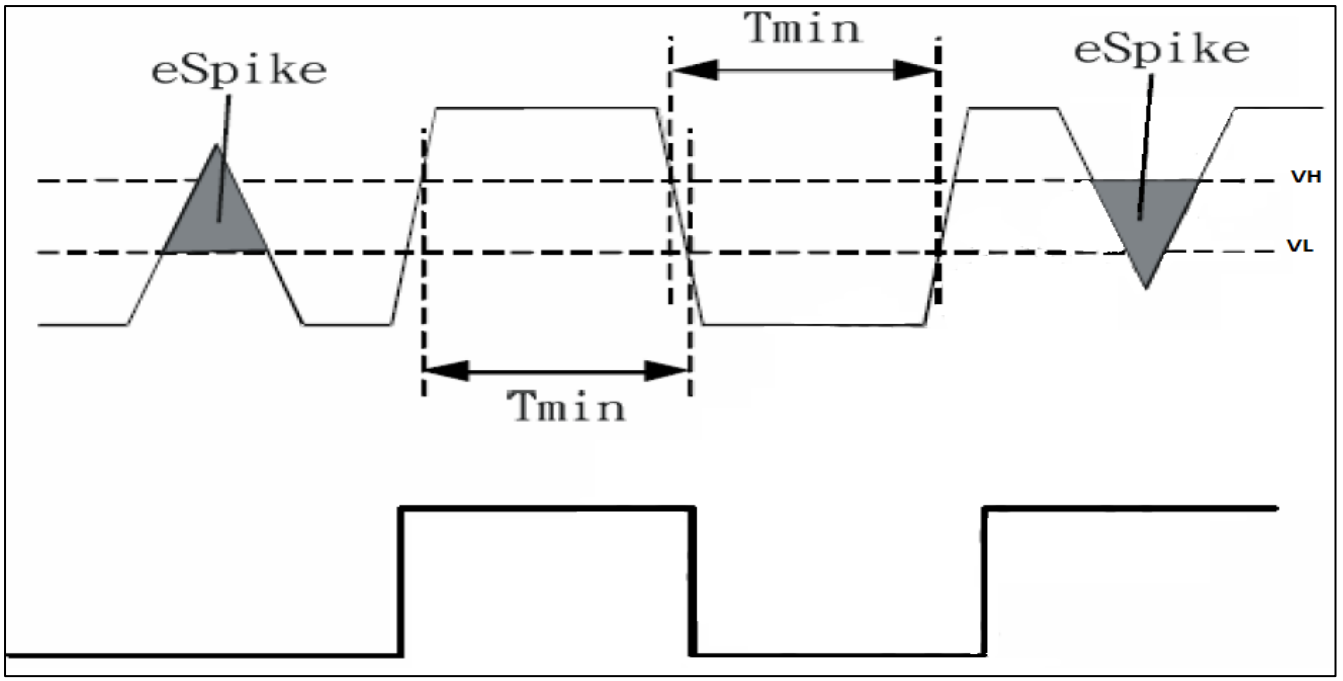
Parameter	Description	Min	Nom	Max	Units	Note
V_{IDTH}	Differential input high threshold			110	mV	1, 4
V_{IDTL}	Differential input low threshold	-110			mV	1, 4
V_{ILHS}	Single ended input low voltage	-40			mV	2
V_{IHHS}	Single ended input high voltage			460	mV	2
V_{CMRXDC}	Common mode voltage Hs receive mode	70		330	mV	2, 3
Z_{ID}	Differential input impedance	80	100	125	Ω	
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz			100	mVpp	5
C_{CM}	Common mode termination			60	pF	6

Notes:

1. The summation of transmission line and bonding pad resistance is assumed to be less than 5 ohms for each input pin.
2. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
3. This table value includes a ground difference of 50mV between the transmitter and receiver, the static common mode level tolerance and variations below 450MHz.
4. One data lane configuration.
5. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

6.4 Low-Power Receiver

The low power receiver is an un-terminated, single ended receiver circuit. The LP receiver is used to detect the low power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than the espike. The filter shall allow pulses wider than Tmin to propagate through the LP receiver. The related diagram shows input glitch rejection of low power receivers. The tables list the AC and DC characteristics for LP-RX.



Parameter	Description	Min	Nom	Max	Unit	Note
V_{IL}	Logic 0 input threshold			550	mV	
V_{IH}	Logic 1 input threshold	880			mV	
e_{SPIKE}	Input pulse rejection			300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20			ns	4
T_{INT}	Peak to peak interference voltage			200	mV	
f_{INT}	Interference frequency	450			MHz	

Notes:

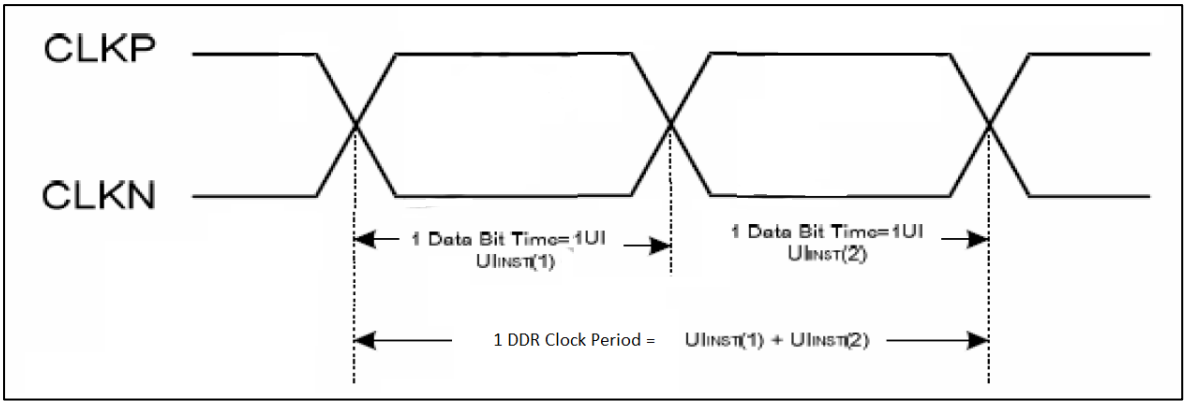
1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

6.5 High-Speed Data Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the forward direction. In either the forward or reverse signaling modes there shall be only one clock source. In the reverse direction, clock is sent in the forward direction and one of four possible edges in used to launch the data.

The master side of the link shall send a differential clock signal to the slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP-CLKN, and similarly for the “falling edge”. Therefore, the period of the clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown below.



The same clock source is used to generate the DDR clock and launch the serial data. Since the clock and data signals propagate together over a channel of specified skew, the clock may be used directly to sample the date lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the lane module to eliminate these instantaneous variations.

The UIINST specifications for the clock signal are summarized below:

Parameter	Symbol	Min	Nom	Max	Unit	Note
UI instantaneous	UI_{INST}	2.5		12.5	ns	1, 2

Notes:

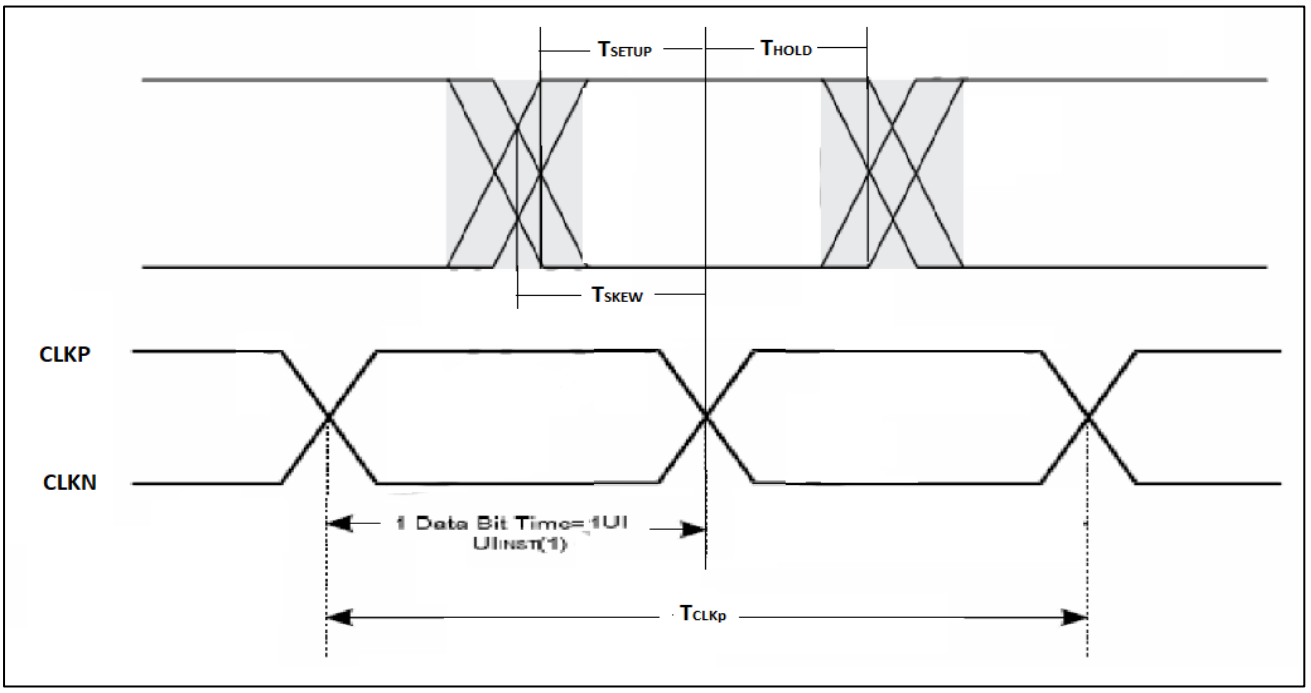
1. This value corresponds to a minimum 80 Mbps data rate and one data lane configuration.
2. The minimum UI shall not be violated for any single bit period, i.e. any DDR half cycle within a data burst.

The timing relationship of the DDR clock differential signal to the data differential signal is shown below. Data is launched in a quadrature relationship to the clock such that the clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.



6.6 Data-Clock Timing Specifications

The data clock timing specifications are shown in the table below. Implementers shall specify a value UINST, MIN that represents the minimum instantaneous UI possible within a high-speed data transfer for a given implementation. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½ UINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX} and THOLD[RX], describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising and falling clock edge. THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver that it will operate at the maximum specified acceptable bit error rate.

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Data to clock setup time (receiver)	$T_{SETUP[RX]}$	0.35			UIINST	1
Clock to data hold time (receiver)	$T_{HOLD[RX]}$	0.25			UIINST	1

Notes:

1. One data lane condition.

6.7 Reset Timing

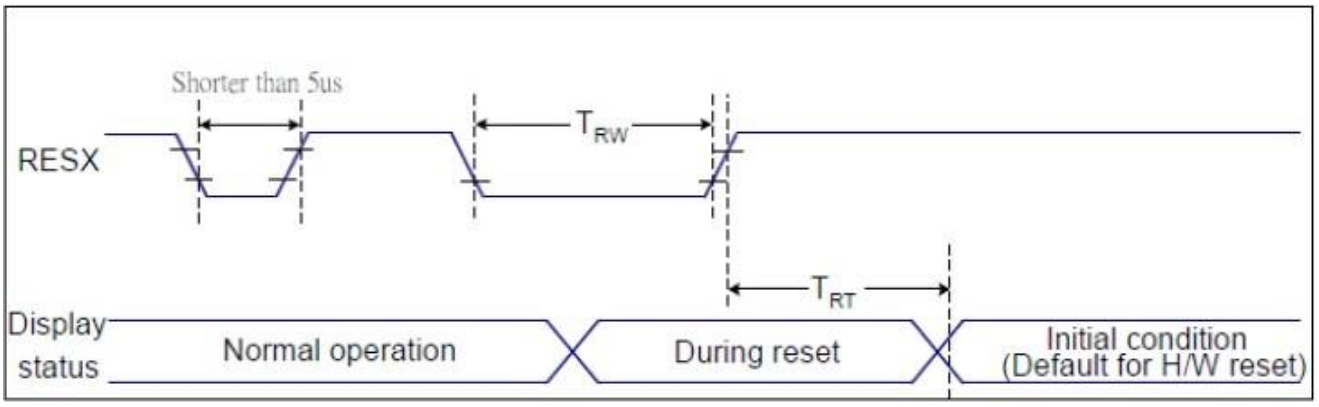


Figure 7 Reset Timing

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

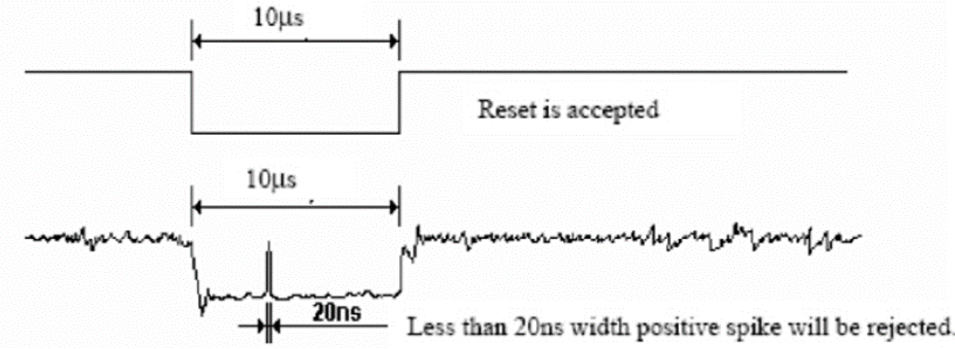
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

7.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.