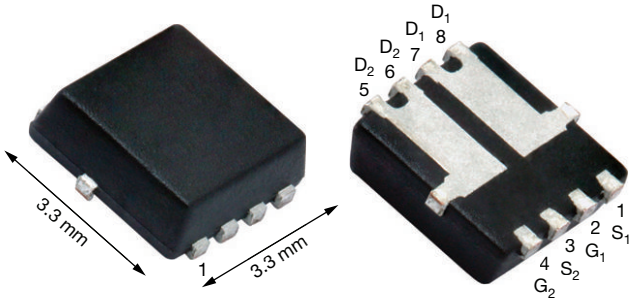
N- and P-Channel 100 V (D-S) MOSFET

PowerPAK® 1212-8 Dual



Top View Bottom View

FEATURES

- TrenchFET® power MOSFETs
- Thermally enhanced PowerPAK®
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

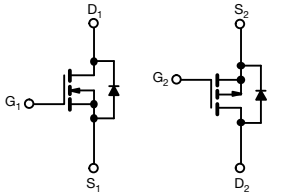
Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- DC/DC converters
- Active clamp
- Brushless DC motors
- AC/DC inverter
- Motor drive switch



PRODUCT SUMMARY

	N-CHANNEL	P-CHANNEL
V_{DS} (V)	100	-100
$R_{DS(on)}$ (Ω) at V_{GS} = ± 10 V	0.167	0.251
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.186	0.338
Q_g typ. (nC)	2.4	4.0
I_D (A) [a, b]	4	
Configuration	N- and p-pair	

ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SIS590DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V_{DS}	100	-100	V
Gate-source voltage		V_{GS}	± 20		
Continuous drain current	T_C = 25 °C	I_D	4 [g]	4 [g]	A
	T_C = 70 °C		4 [g]	4 [g]	
	T_A = 25 °C		2.7 [a, b]	2.3 [a, b]	
	T_A = 70 °C		2.1	1.8	
Pulsed drain current (t = 100 µs)		I_{DM}	8	10	
Continuous source-drain diode current	T_C = 25 °C	I_S	14.9	19.3	
	T_C = 70 °C		9.5	12.3	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	4	10	W
Single pulse avalanche energy		E_{AS}	0.8	5.0	
Maximum Power Dissipation	T_C = 25 °C	P_D	17.9	23.1	
	T_C = 70 °C		11.4	14.8	
	T_A = 25 °C		2.5 [a, b]	2.6 [a, b]	
	T_A = 70 °C		1.6	1.7	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	40	50	38	48	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.6	7	4.3	5.4	

Notes

a. Based on silicon capability only
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 94 °C/W
g. Package limited

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	100	-	-	V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-100	-	-	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch	-	79	-	mV/°C
		I_D = -250 µA	P-Ch	-	-68	-	
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch	-	-4.4	-	
		I_D = -250 µA	P-Ch	-	4.3	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.5	-	2.5	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1.5	-	-2.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	N-Ch	-	-	± 100	nA
			P-Ch	-	-	± 100	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	N-Ch	-	-	1	µA
		V_{DS} = -100 V, V_{GS} = 0 V	P-Ch	-	-	-1	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch	-	-	10	
		V_{DS} = -100 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch	-	-	-10	
On-state drain current [b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	N-Ch	4	-	-	A
		$V_{DS} \leq$ -5 V, V_{GS} = -10 V	P-Ch	-4	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.5 A	N-Ch	-	0.139	0.167	Ω
		V_{GS} = -10 V, I_D = -2.3 A	P-Ch	-	0.197	0.251	
		V_{GS} = 4.5 V, I_D = 1.0 A	N-Ch	-	0.155	0.186	
		V_{GS} = -4.5 V, I_D = -2.0 A	P-Ch	-	0.260	0.338	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 2.7 A	N-Ch	-	10	-	S
		V_{DS} = -10 V, I_D = 2.3 A	P-Ch	-	24	-	
Dynamic [a]							
Input capacitance	C_{iss}	N-channel V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz P-channel V_{DS} = -50 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	-	265	-	pF
			P-Ch	-	325	-	
Output capacitance	C_{oss}		N-Ch	-	20	-	
			P-Ch	-	90	-	
Reverse transfer capacitance	C_{rss}		N-Ch	-	2	-	
			P-Ch	-	5	-	
Total gate charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 0.2 A	N-Ch	-	5.2	104	nC
		V_{DS} = -50 V, V_{GS} = -10 V, I_D = -9 A	P-Ch	-	11.2	22.4	
		N-channel V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 0.2 A P-channel V_{DS} = -50 V, V_{GS} = -4.5 V, I_D = 2.3 A	N-Ch	-	2.4	4.8	
			P-Ch	-	5.7	11.4	
Gate-source charge	Q_{gs}		N-Ch	-	1.0	-	
			P-Ch	-	2.4	-	
Gate-drain charge	Q_{gd}		N-Ch	-	0.5	-	
			P-Ch	-	2.5	-	
Gate resistance	R_g	f = 1 MHz	N-Ch	0.24	1.2	2.4	Ω
			P-Ch	0.76	3.8	7.6	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX**	**UNIT**
Dynamic [a]							
Turn-on delay time	$t_{d(on)}$	N-channel V_{DD} = 10 V, R_L = 2 Ω, $I_D \cong$ 2.1 A, V_{GEN} = 10 V, R_g = 1 Ω; P-channel V_{DD} = -10 V, R_L = 2 Ω, $I_D \cong$ -1.8 A, V_{GEN} = -10 V, R_g = 1 Ω	N-Ch	-	12	25	ns
			P-Ch	-	15	30	
Rise time	t_r		N-Ch	-	45	90	
			P-Ch	-	50	100	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	22	45	
			P-Ch	-	30	60	
Fall time	t_f		N-Ch	-	12	25	
			P-Ch	-	11	20	
Turn-on delay time	$t_{d(on)}$	N-channel V_{DD} = 10 V, R_L = 2 Ω, $I_D \cong$ 2.1 A, V_{GEN} = 4.5 V, R_g = 1 Ω; P-channel V_{DD} = -10 V, R_L = 2 Ω, $I_D \cong$ -1.8 A, V_{GEN} = -4.5 V, R_g = 1 Ω	N-Ch	-	6	15	
			P-Ch	-	10	15	
Rise time	t_r		N-Ch	-	21	40	
			P-Ch	-	23	45	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	20	40	
			P-Ch	-	26	50	
Fall time	t_f		N-Ch	-	10	20	
			P-Ch	-	10	20	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_A = 25 °C	N-Ch	-	-	2.1	A
			P-Ch	-	-	-2.2	
Pulse diode forward current (t = 100 µs)	I_{SM}		N-Ch	-	-	8	
			P-Ch	-	-	-10	
Body diode voltage	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V	N-Ch	-	0.8	1.2	V
		I_S = -1.8 A, V_{GS} = 0 V	P-Ch	-	-0.81	-1.2	
Body diode reverse recovery time	t_{rr}	N-channel I_F = -1.8 A, dI//dt = 100 A/µs, T_J = 25 °C; P-channel I_F = -1.8 A, dI/dt = -100 A/µs, T_J = 25 °C	N-Ch	-	23	46	ns
			P-Ch	-	37	74	
Body diode reverse recovery charge	Q_{rr}		N-Ch	-	21	42	nC
			P-Ch	-	65	130	
Reverse recovery fall time	t_a		N-Ch	-	21	-	ns
			P-Ch	-	34	-	
Reverse recovery rise time	t_b		N-Ch	-	2	-	
			P-Ch	-	3	-	

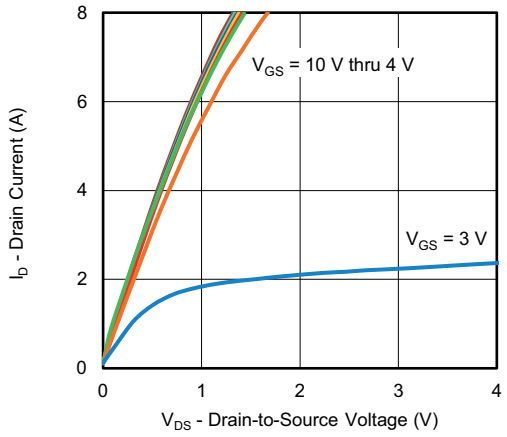
Notes

a. Guaranteed by design, not subject to production testing.

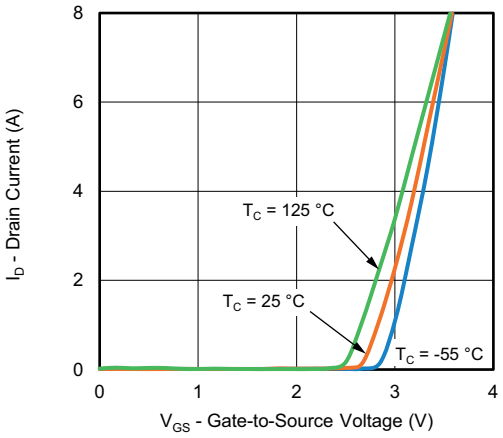
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

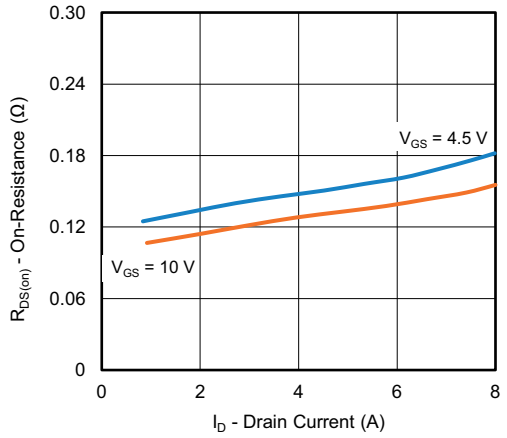
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



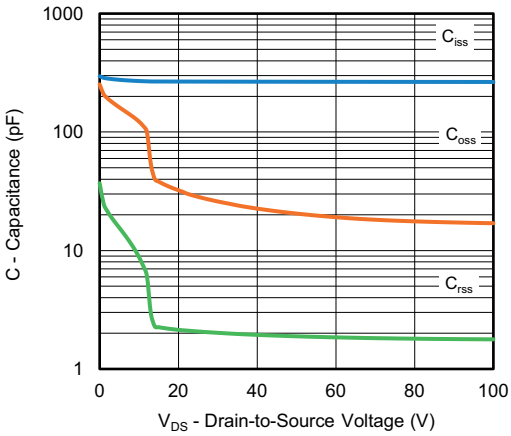
Output Characteristics



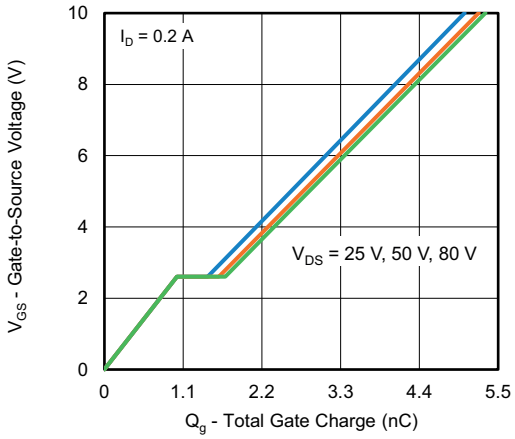
Transfer Characteristics



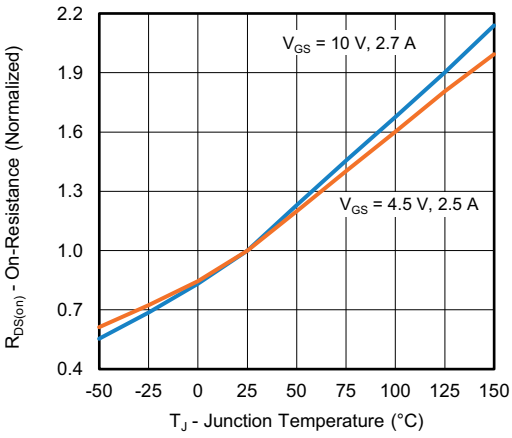
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

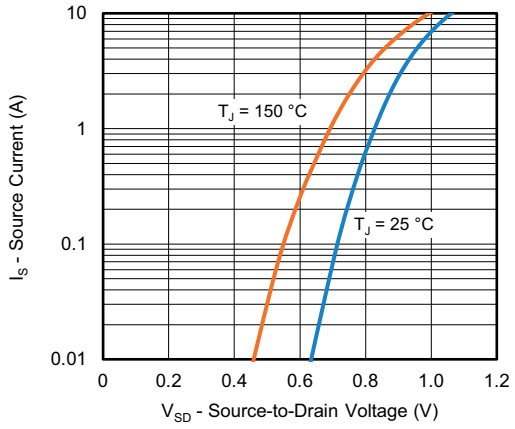


Gate Charge

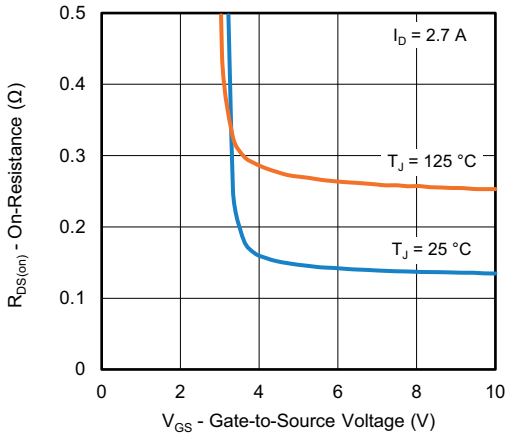


On-Resistance vs. Junction Temperature

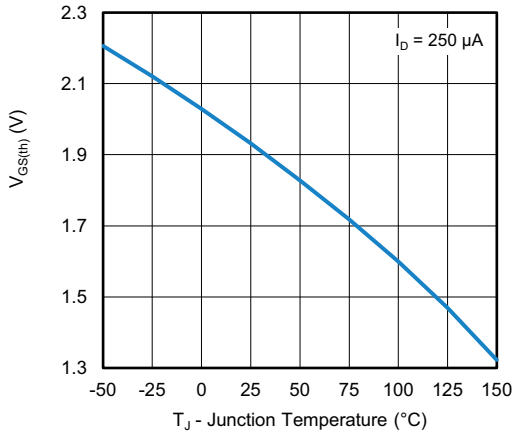
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



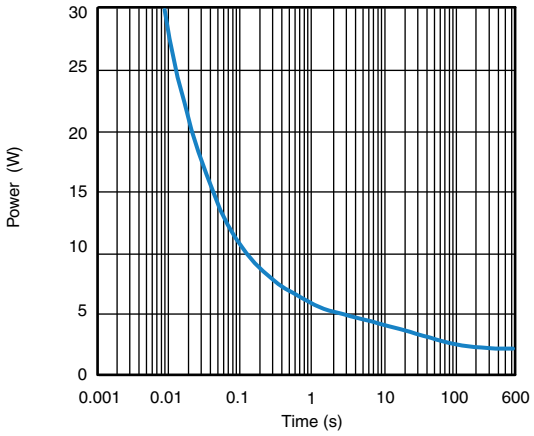
Source-Drain Diode Forward Voltage



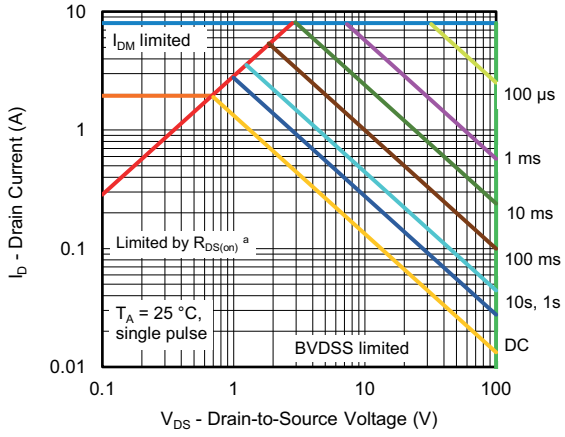
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)

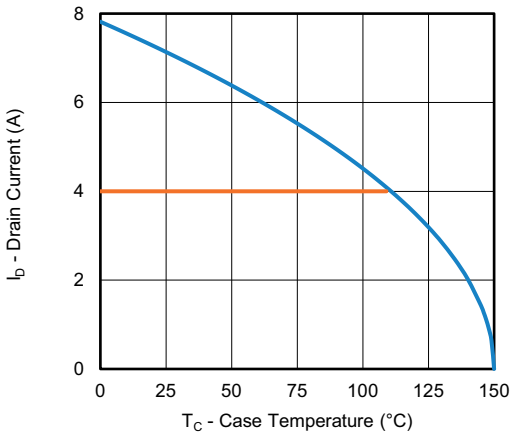


Safe Operating Area, Junction-to-Ambient

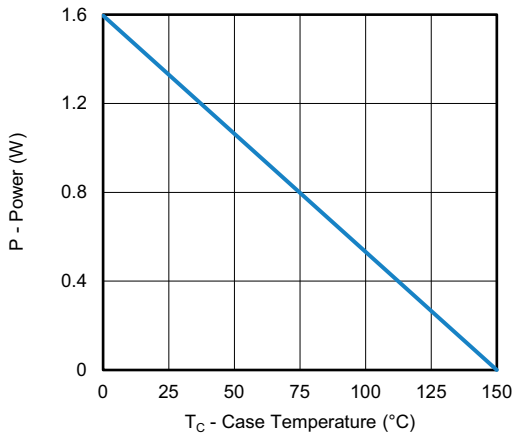
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

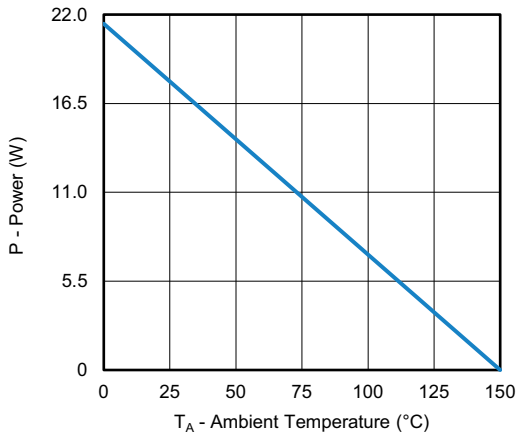
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power Junction to Ambient

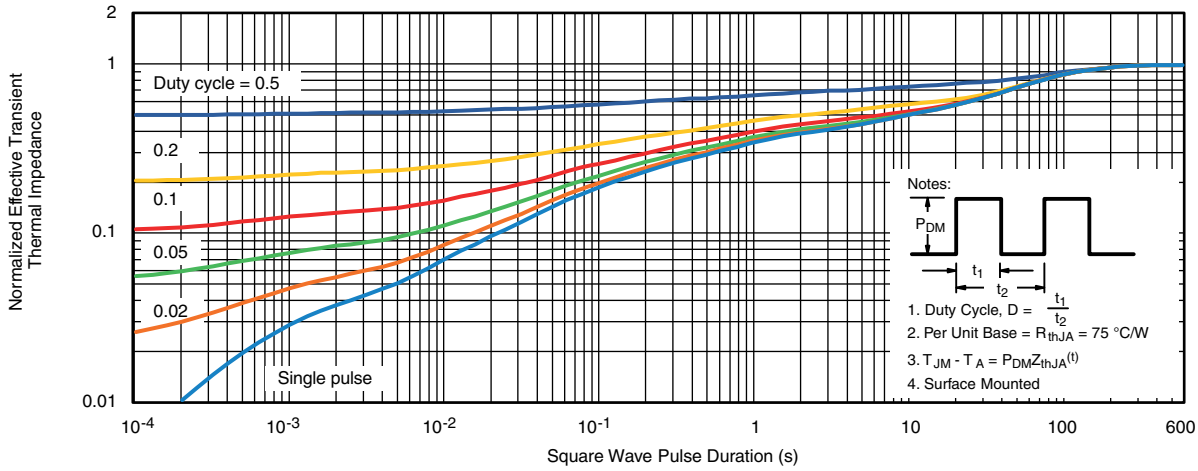


Power Junction to Case

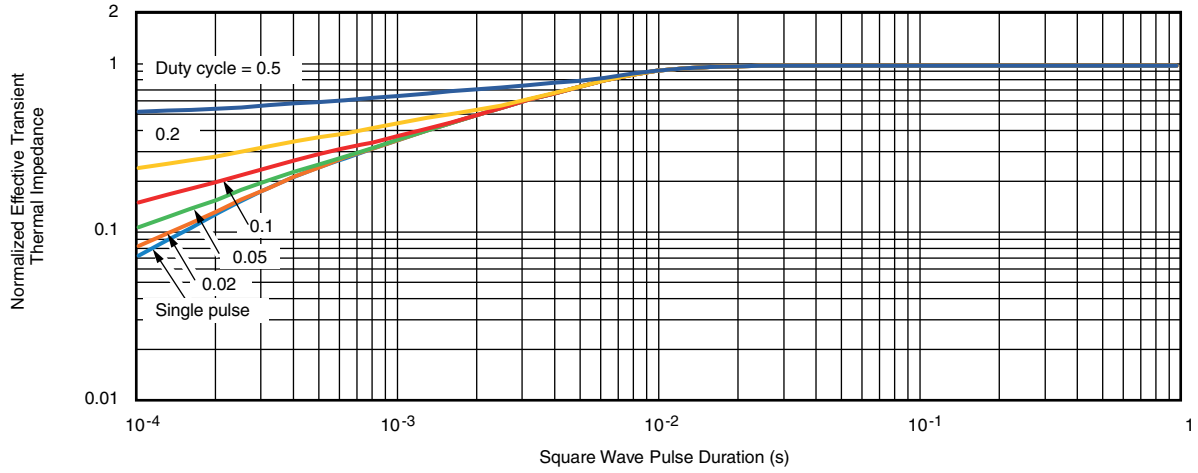
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

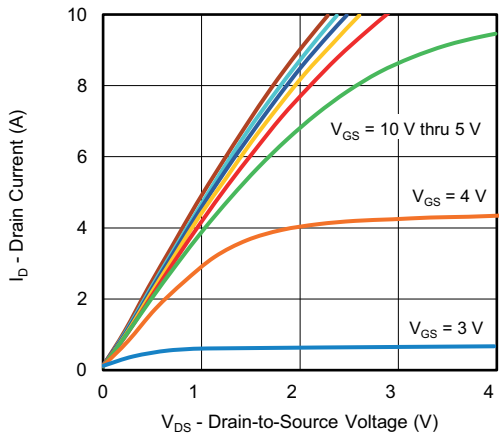


Normalized Thermal Transient Impedance, Junction-to-Ambient

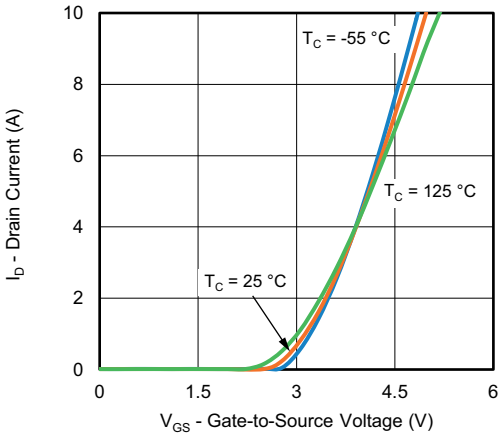


Normalized Thermal Transient Impedance, Junction-to-Case

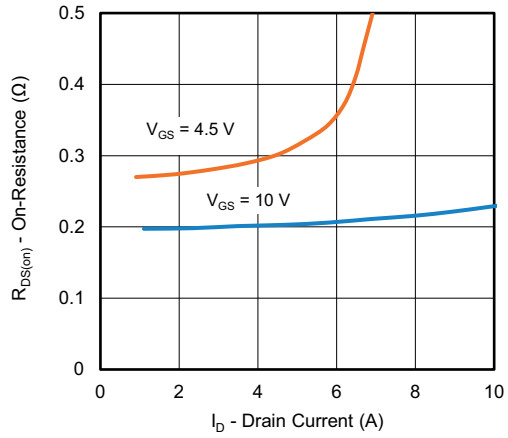
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



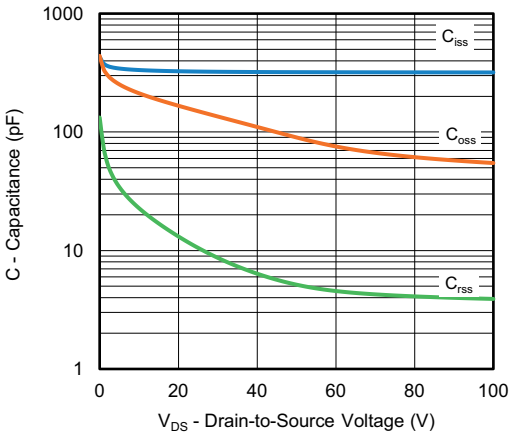
Output Characteristics



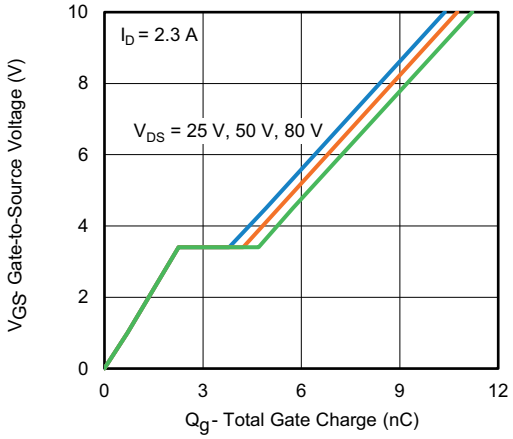
Transfer Characteristics



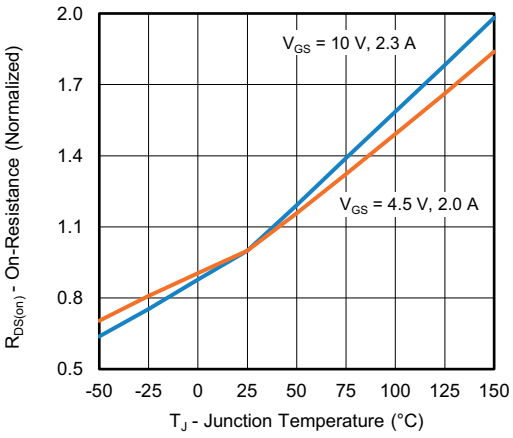
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

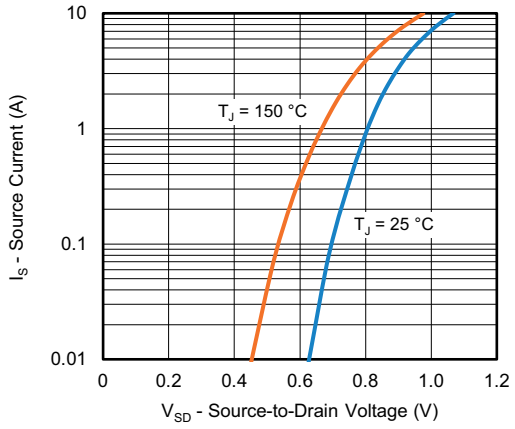


Gate Charge

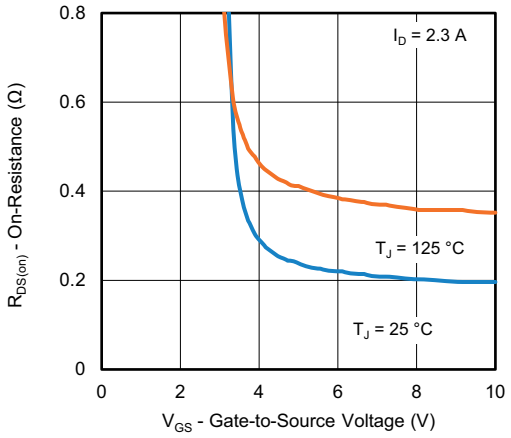


On-Resistance vs. Junction Temperature

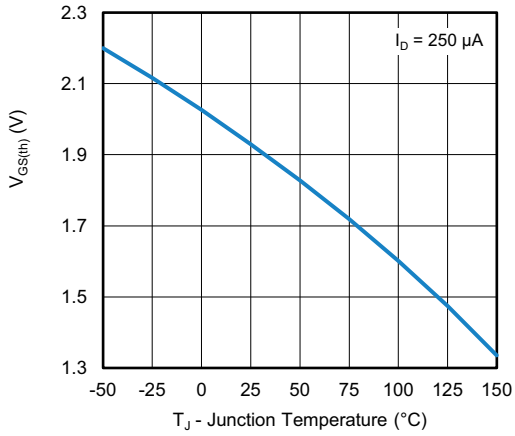
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



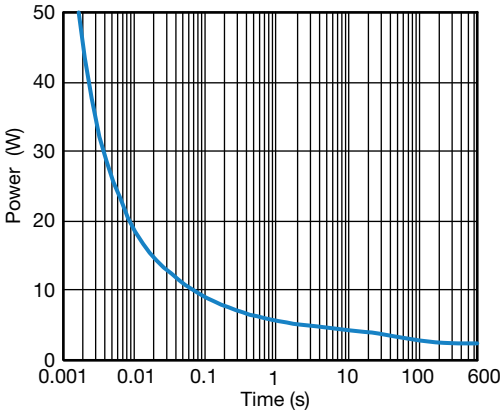
Source-Drain Diode Forward Voltage



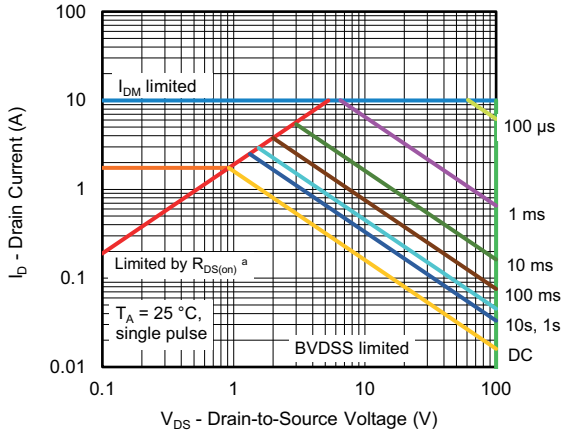
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

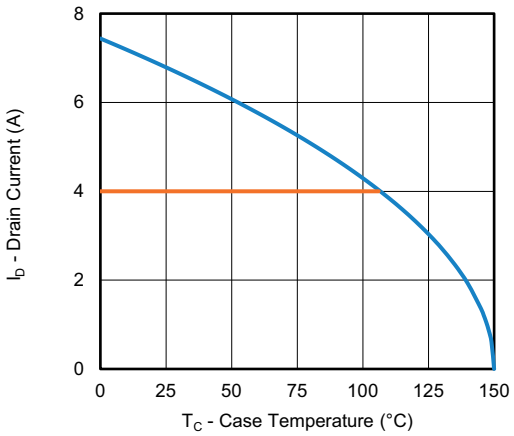


Safe Operating Area, Junction-to-Ambient

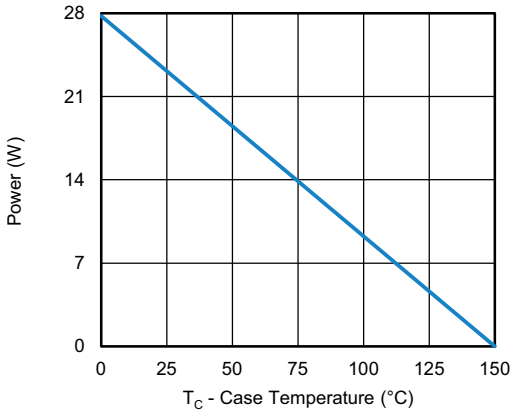
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

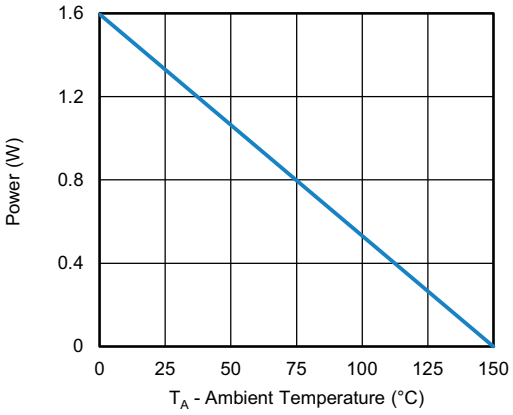
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power Junction to Ambient

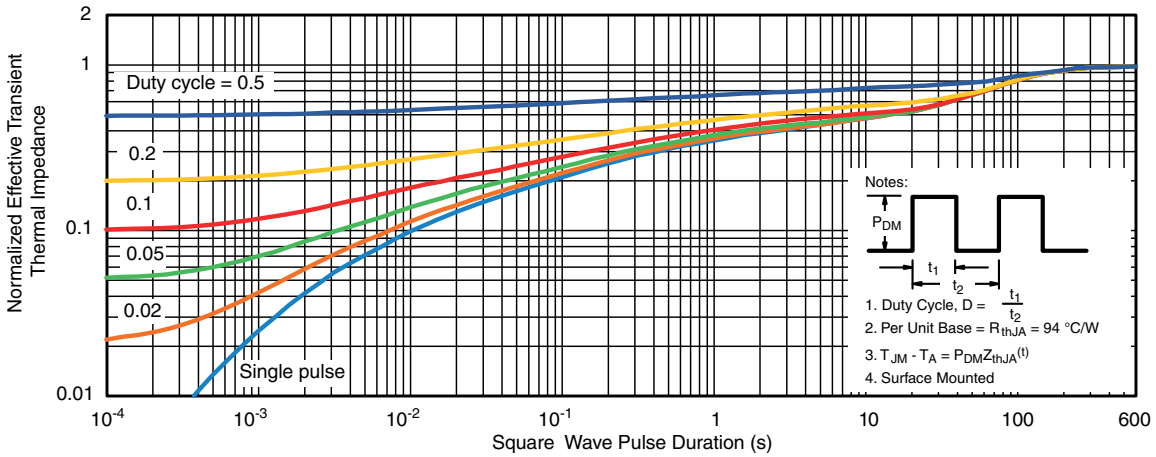


Power Junction to Case

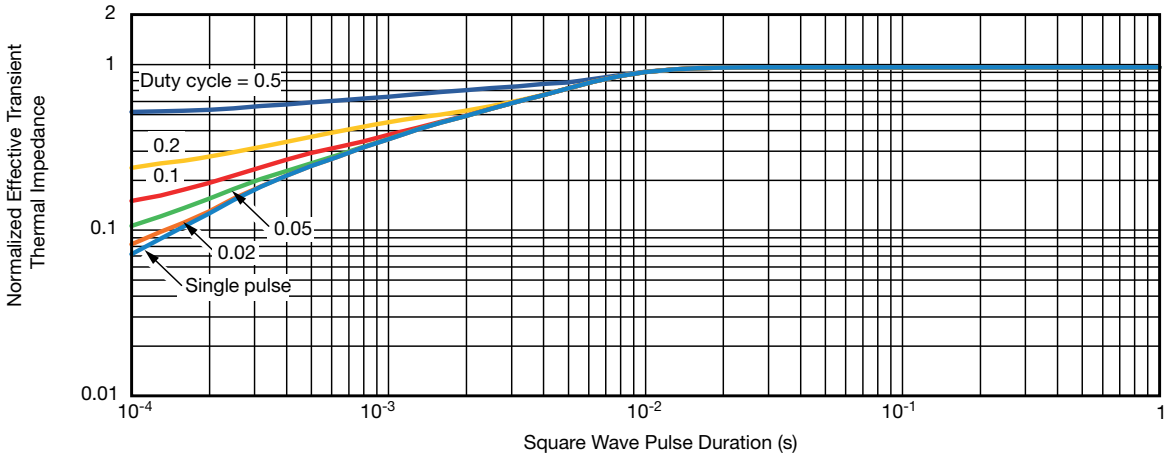
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



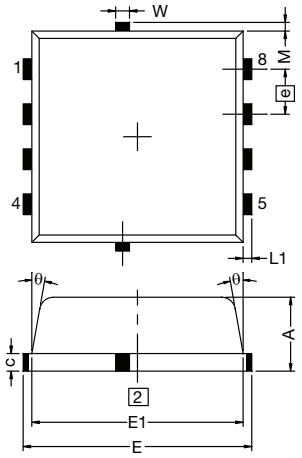
Normalized Thermal Transient Impedance, Junction-to-Ambient

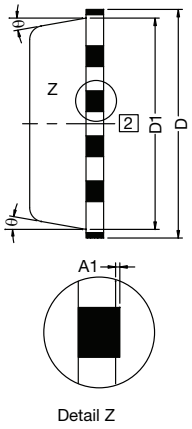


Normalized Thermal Transient Impedance, Junction-to-Case

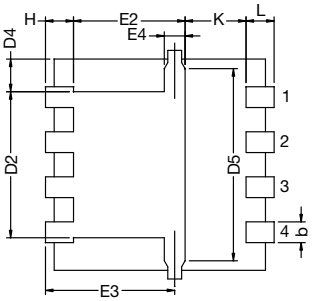
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63046.

PowerPAK® 1212-8, (Single / Dual)

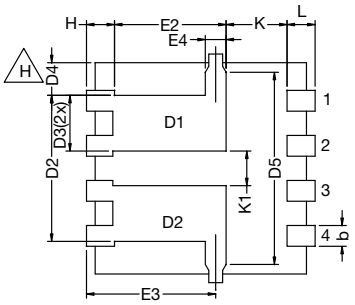




Detail Z



Backside view of single pad

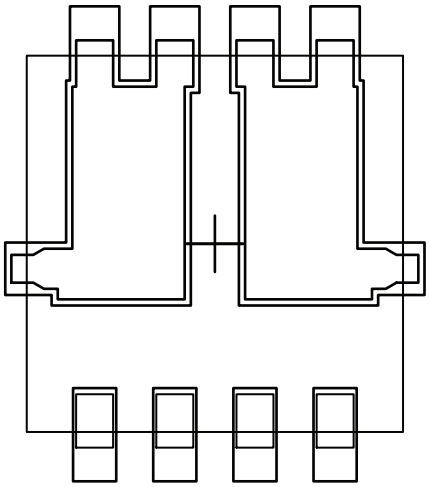


Backside view of dual pad

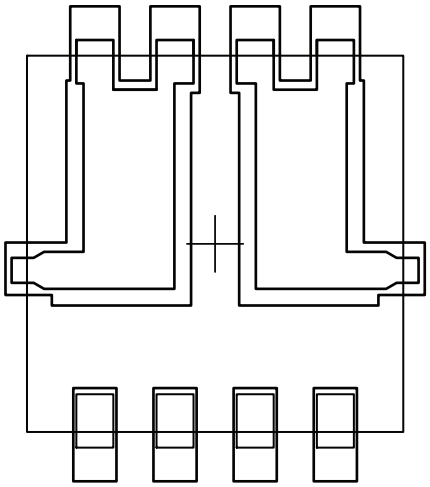
Notes
1. Inch will govern
2 Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S16-2667-Rev. M, 09-Jan-17 DWG: 5882						

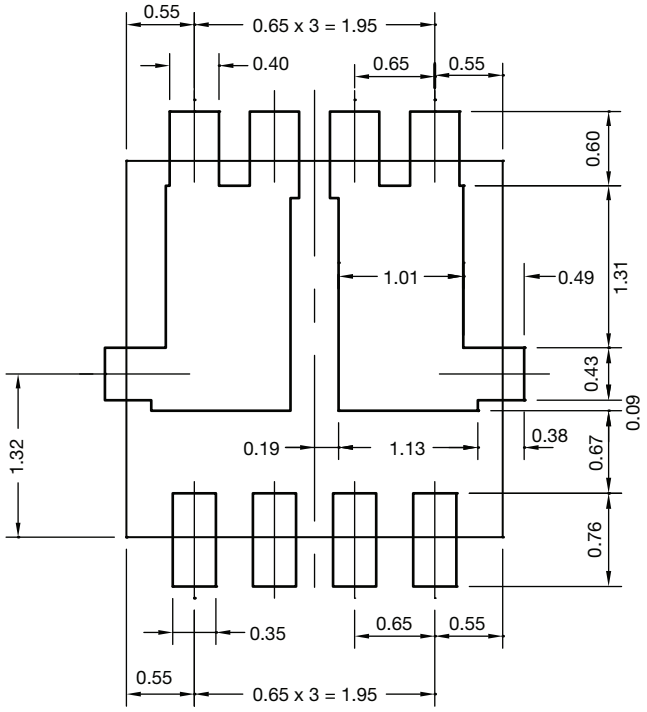
Recommended Land Pattern for PowerPAK® 1212-8 Dual



For BW package



For BWL package



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