MAX25431

Automotive 40V, 2.2MHz, H-Bridge Buck-Boost Controller

General Description

The MAX25431 is a current-mode buck-boost controller. The device operates with input voltages from 6V to 36V. The switching frequency is resistor programmable from 220kHz to 2.2MHz and can be synchronized to an external clock.

The device output voltage is available as 5V fixed or adjustable from 3V to 25V. The wide input voltage range, along with its ability to maintain constant output voltage during battery transients, makes the devices ideal for automotive applications. In light-load applications, a logic input (FSYNC) allows the devices to operate in fixed-frequency, forced-PWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit followed by hiccup during sustained overloads, input under-voltage lockout (UVLO), output overvoltage protection and thermal shut- down with automatic recovery.

The MAX25431 is available in a small 4mm x 4mm 24-pin TQFN-EP SW package.

Applications

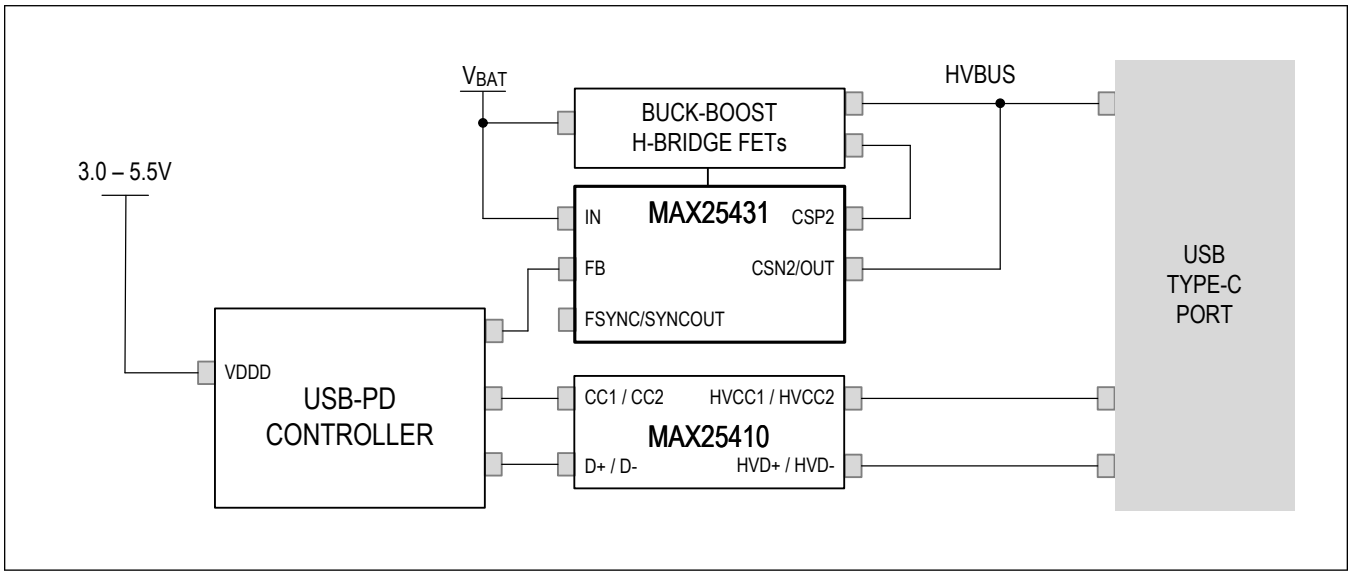
- USB Hubs, Breakout Boxes and Multimedia Hubs
- Dedicated Charging Modules
- Rear-Seat Entertainment Modules

Benefits and Features

- Meets Stringent Automotive Quality and Reliability Requirements
  - Operating V_{IN} Range: 6V to 36V Allows Operation In Cold-Crank Conditions
  - Tolerates Input Transients to 40V
  - EN Pin Compatible from +3.3V to +40V
  - -40°C to +125°C Automotive Temperature Range
  - AEQ-100 Qualified
- Efficient Solution in a Small Solutions Size
  - Fixed 5V Output Voltage and Adjustable 3V to 25V
  - High Switching Frequency Allows Use of Small External Components
  - Small 4mm x 4mm 24-Pin SWTQFN Package
- Low Quiescent Current Helps Designers Meet Stringent OEM Current Requirements
  - 10µA (max) Quiescent Current in Shutdown
- EMI Mitigation to meet CISPR25 Class 5 Requirements
  - 220kHz to 2.2MHz Operating Frequency
  - Fixed-Frequency PWM Mode with Spread Spectrum
  - External Frequency Synchronization or SYNC OUT Capability

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



Absolute Maximum Ratings

IN ..... -0.3V to +40V
EN, LX1, CSP1, CSN1 ..... -0.3V to V_{IN} + 0.3V
LX2, OUT, CSP2, CSN2 ..... -0.3V to +30V
CSP_ to CSN_ ..... -0.3V to +0.3V
BST1 to LX1, BST2 to LX2 ..... -0.3V to 6V
BST1, DH1 ..... -0.3V to 46V
BST2, DH2 ..... -0.3V to 36V
DH_ to LX_ ..... -0.3V to $V_{BST\_}$ + 0.3V
V_{CC}, PGOOD ..... -0.3V to 6V
DL_, COMP, FB, SLP, FSW, FSYNCH. ..... -0.3V to V_{CC} + 0.3V
PGND_ ..... -0.3V to 0.3V
OUT/FB Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (Multilayer Board)
24L TQFN .....
(T_A = +70°C, derate 23.58 mW/°C above +70°C) 1886.6mW
Operating Temperature Range ..... -40ºC to +125ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -40ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC
Soldering Temperature ..... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 SW-TQFN

Package Code	T2444Y+4C
Outline Number	21-100290
Land Pattern Number	90-0022
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	42.4°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3.2°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = V_{EN} = 14V, T_A = T_J = -40°C to +125°C, CVCC = 4.7µF, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Normal operation (Note 3)	6		36	V
IN UVLO	$V_{IN\_UVLO\_R}$	Rising		6.5	6.7	V
	$V_{IN\_UVLO\_F}$	Falling		5.8	6.0	
Shutdown Supply Current	I_{IN_SHDN}	V_{EN} = 0V		5	10	µA
V_{CC} REGULATOR						
V_{CC} Output Voltage	V_{CC}	V_{IN} > 6V, I_{VCC} = -1mA to -40mA		5		V
V_{CC} Undervoltage Lockout	$UVLO_{VCC}$	V_{CC} rising		4	4.25	V
		V_{CC} falling		3.5	3.8	
V_{CC} Short-Circuit Current Limit	$IVCC_{SC}$	V_{CC} shorted to AGND		20		mA

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 14V, T_A = T_J = -40°C to +125°C, CVCC = 4.7µF, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUCK BOOST CONTROLLER						
Fixed Output Voltage	V_{OUT_5V}	V_{FB} = V_{CC}	4.9	5	5.1	V
Output Voltage Adjustable Range			3		25	V
Soft-Start Ramp Time	T_{START}		4	7	10	ms
Minimum On Time	T_{ON_MIN}	Buck mode (Q_{t1})		80		ns
Dead Time	DT	Rising and falling edges of DH_ to DL_ and DL_ to DH_		20		ns
DH Pullup Resistance	R_{DH_PULLUP}	V_{CC} = 5V, I_{DH}= -100mA		2	4	Ω
DH Pulldown Resistance	$R_{DH\_PULLDOWN}$	V_{CC} = 5V, I_{DH}= 100mA		1	2	Ω
DL Pullup Resistance	R_{DL_PULLUP}	V_{CC} = 5V, I_{DL} = -100mA		2	4	Ω
DL Pulldown Resistance	$R_{DL\_PULLDOWN}$	V_{CC} = 5V, I_{DL} = -100mA		1	2	Ω
DL1, DL2 Leakage Current	I_{DL_LKG}	V_{EN} = 0V, V_{DL1} = V_{DL2} = 0V to 5V, T_A = +25°C			1.0	µA
DH1 Leakage Current	I_{DH1_LKG}	V_{EN} = 0V, V_{DH1} = V_{LX1} = 0V, T_A = +25°C			1.0	µA
		V_{EN} = 0V, V_{DH1} = 5V, V_{LX1} = 0V			10	
DH2 Leakage Current	I_{DH2_LKG}	V_{EN} = 0V, V_{DH2} = V_{LX2} = 0V, T_A = +25°C			1.0	µA
		V_{EN} = 0V, V_{DH2} = 5V, V_{LX2} = 0V			10	
CURRENT SENSE						
CS Limit Threshold	V_{OC1}	V_{CSP1} - V_{CSN1} rising		50	60	mV
CS Runaway Limit Threshold	V_{OC2}	V_{CSP2} - V_{CSN2} rising, V_{OUT} > 0V		75	90	mV
CS Negative Limit Threshold	V_{OC3}	|V_{CSP2} - V_{CSN2}| rising, V_{OUT} > 3V, F_{SYNC} = V_{CC}	-26	-20	-16	mV
ERROR AMPLIFIER						
Regulated Feedback Voltage	V_{FB}		1.233	1.25	1.267	V
FB Leakage Current	I_{FB_LKG}	V_{FB_LKG} = 5.5V, T_A = +25°C			1	µA
FB Line Regulation Error	REG_{FB}	V_{IN} = 7V to 36V, V_{FB} = 1.25V		0.01		%/V
Transconductance (from FB to COMP)	G_M	V_{FB} = 1.25V, V_{CC} = 5V	500	750	1050	µS
SLP Output Voltage	V_{SLP}	I_{RT} = 100µA	1.2	1.25	1.3	V
SWITCHING FREQUENCY						
FSW Pin Voltage	V_{FSW}	I_{FSW} = 10µA	1.20	1.23	1.27	V
PWM Switching Frequency	f_{SW1}	R_{FSW} = 12kΩ	2.0	2.2	2.4	MHz
	f_{SW2}	R_{FSW} = 73.2kΩ	360	420	460	kHz

Electrical Characteristics (continued)

(V_{IN} = V_{EN} = 14V, T_A = T_J = -40°C to +125°C, CVCC = 4.7µF, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Switching Frequency Range	f_{RNG}		0.220		2.2	MHz
FSYNC External Clock Input	f_{SYNC1}	Minimum sync pulse width of 100ns, percentage of internal clock frequency set by R_{FSW}	80		100	%
Spread Spectrum	SPS	Spread spectrum enabled		f_{SW} ±3%		
OUTPUT MONITORS						
Output Overvoltage Threshold	V_{OUT_OVP}	Detected with respect to V_{FB} rising	105.5	108	111.4	%
Output Overvoltage Hysteresis	$V_{OUT\_OVP\_HYS}$			3		%
PGOOD Threshold	P_{GOOD_R}	% of V_{OUT}, rising	92.8	95	98	%
	P_{GOOD_F}	% of V_{OUT}, falling	89.5	92	95	
PGOOD Output Low Voltage	V_{PGOODL}	I_{SINK} = 1mA			0.2	V
PGOOD Leakage Current	I_{PGOOD_LEAK}	V_{PGOOD} = V_{CC}, T_A = +25°C			1	µA
PGOOD Debounce Time	T_{PGOOD}	Fault detection, rising		60		µs
		Fault detection, falling		13		
LOGIC INPUTS (EN, FSYNC)						
Input High Level	V_{THDIMH}	V_ rising	2.1			V
Input Low Level	V_{THDIML}	V_ falling			0.8	V
Input Leakage Current	I_{IN_LEAK}	V_ = 5.5V, T_A = +25°C			1	µA
FSYNC Pulldown Resistance	$R_{FSYNCH-PD}$			1		MΩ
SYNC OUT Drop Voltage	V_{SYNCHL}	PIN 12 programmed as SYNC OUT, ISYNC/SOURCE = 1mA		0.2		V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TH_SHTDWN}	(Note 2)		170		ºC
Thermal Shutdown Hysteresis	T_{TH_HYS}	(Note 2)		20		ºC

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

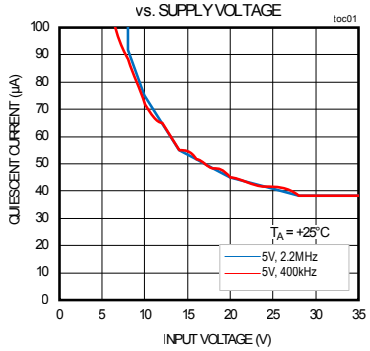
Note 2: Guaranteed by design; not production tested.

Note 3: During initial startup, V_{SUP} rising must cross 6.7V. The normal operating range is then valid.

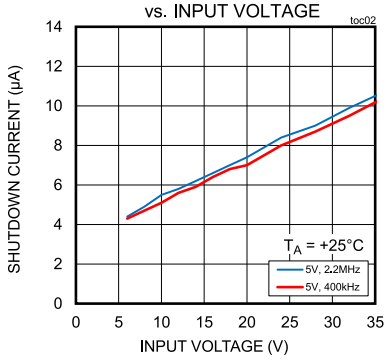
Typical Operating Characteristics

(V_{SUP} = V_{EN} = 14V, T_A = +25°C, unless otherwise noted.)

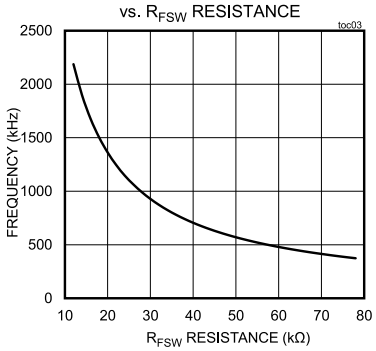
STANDBY QUIESCENT CURRENT vs. SUPPLY VOLTAGE



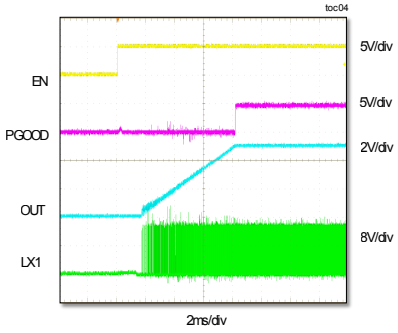
SHUTDOWN CURRENT vs. INPUT VOLTAGE



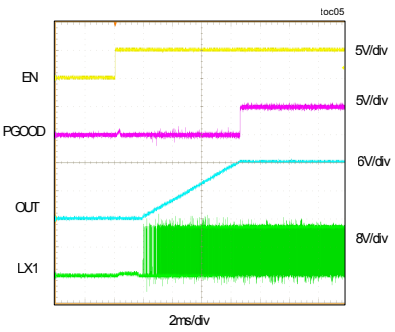
FREQUENCY vs. R_{FSW} RESISTANCE



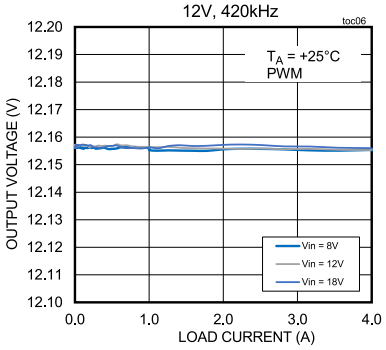
2.2MHz, 5V, STARTUP



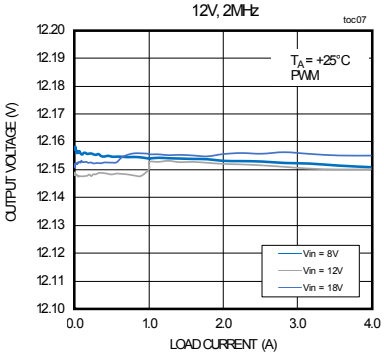
2MHz, 12V, STARTUP



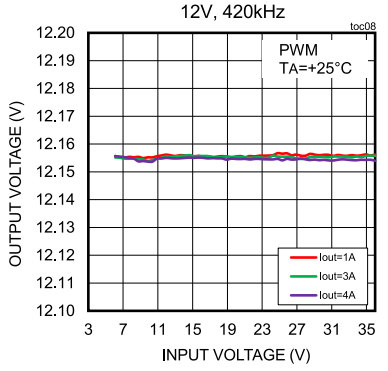
LOAD REGULATION 12V, 420kHz



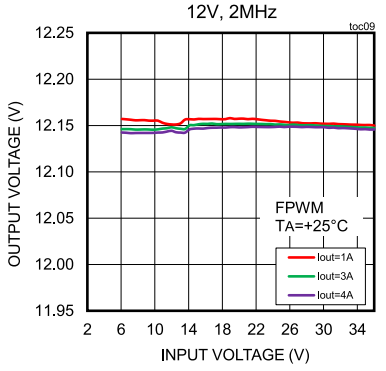
LOAD REGULATION 12V, 2MHz



LINE REGULATION 12V, 420kHz



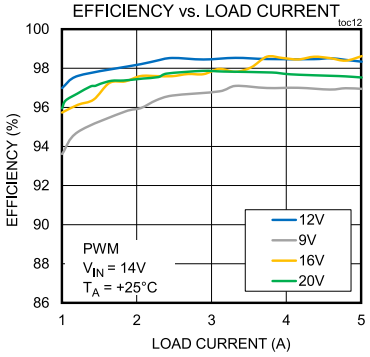
LINE REGULATION 12V, 2MHz



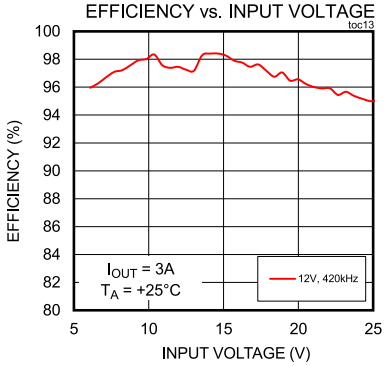
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, T_A = +25°C, unless otherwise noted.)

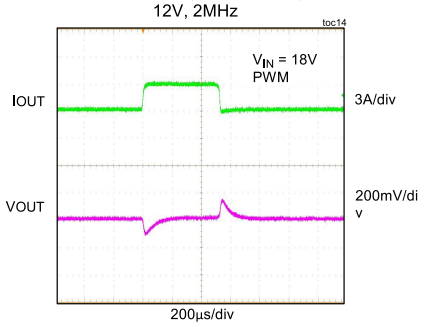
EFFICIENCY vs. LOAD CURRENT



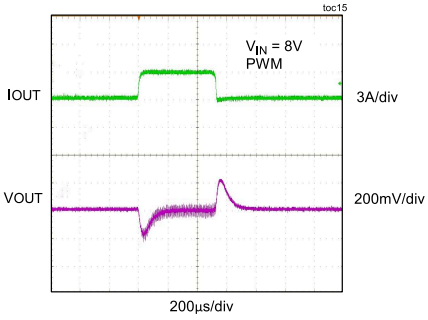
EFFICIENCY vs. INPUT VOLTAGE



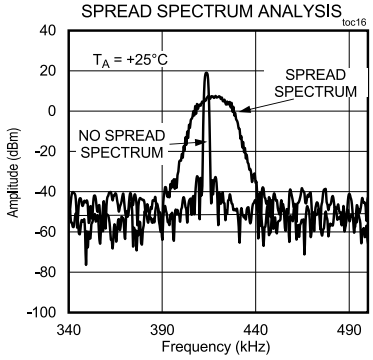
LOAD STEP (BUCK MODE)
12V, 2MHz



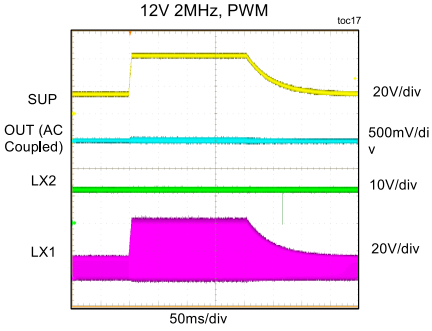
LOAD STEP (BOOST MODE)
12V, 2MHz



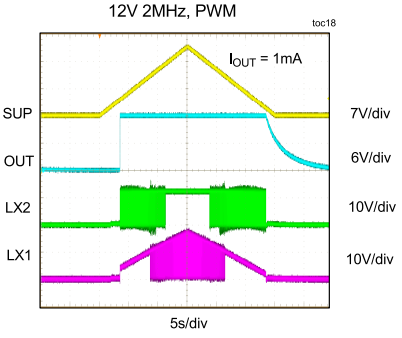
5V 420KHZ, BUCK MODE
SPREAD SPECTRUM ANSYSIS



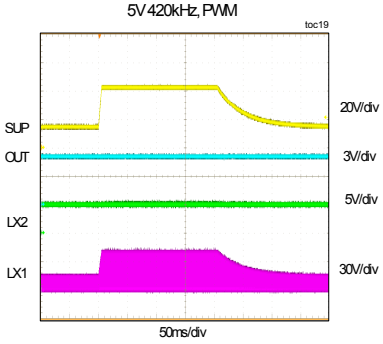
LOAD DUMP
12V 2MHz, PWM



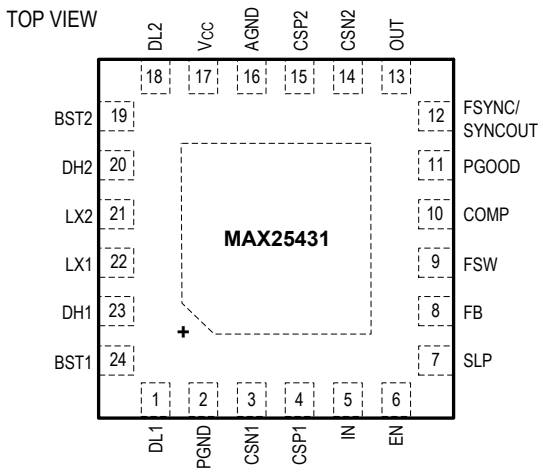
SLOW VIN RISE
12V 2MHz, PWM



LOAD DUMP
5V 420kHz, PWM



Pin Configuration



TQFN
(4mm x 4mm)

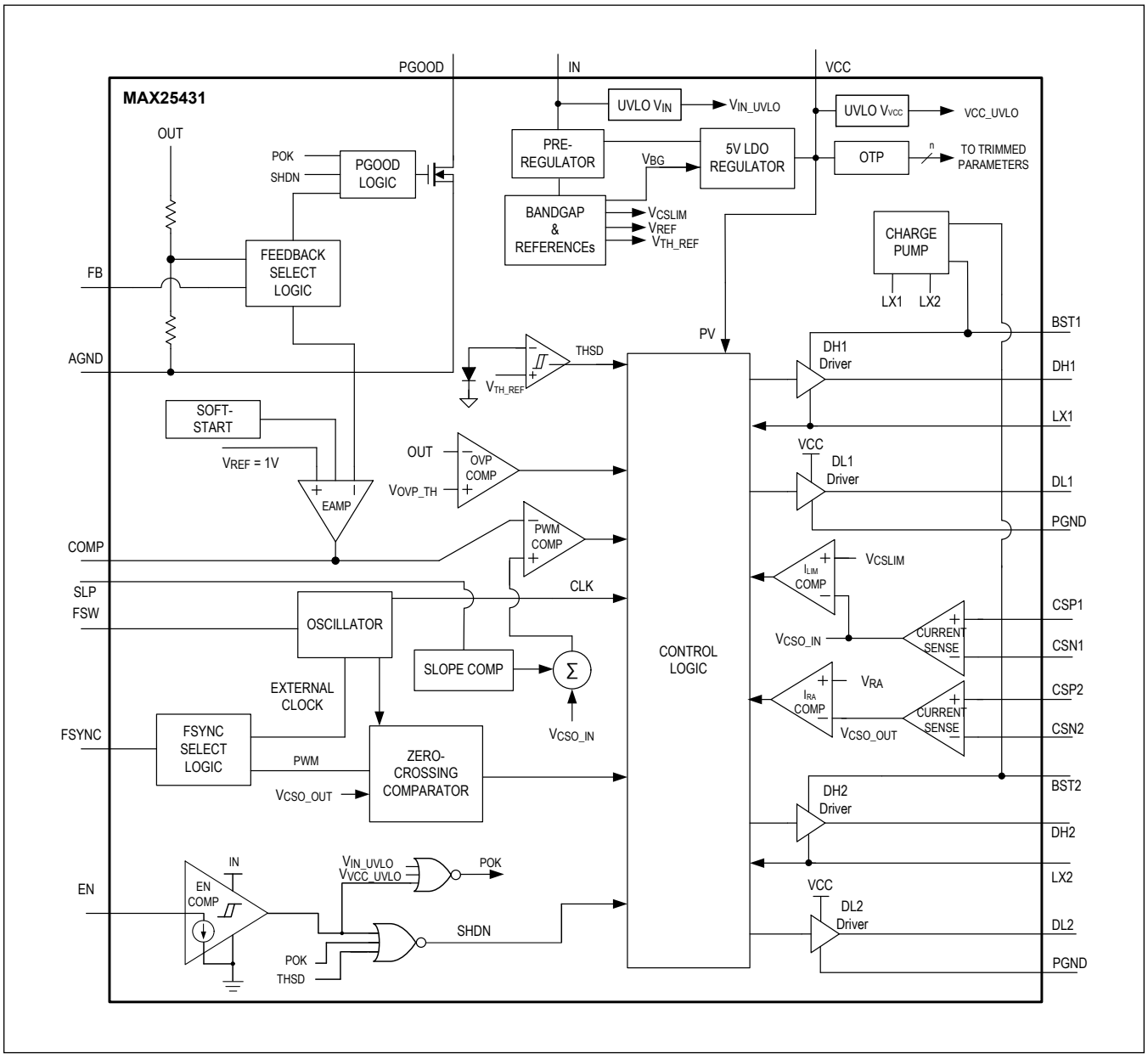
Pin Description

PIN	NAME	FUNCTION
1	DL1	Buck Low Side Gate Drive
2	PGND	Power Ground
3	CSN1	Negative Input of the Input Side Current-Sense Amplifier. Connect CSN1 to the negative side of the input current-sense resistor.
4	CSP1	Positive Input of the Input Side Current-Sense Amplifier. Connect CSP1 to the positive side of the input current-sense resistor.
5	IN	Voltage Supply Input. IN powers up the internal linear regulator. Bypass IN to PGND with a ceramic capacitor as suggested in the *Typical Application Circuit*.
6	EN	High-Voltage Enable Input. Driving EN high enables the buck-boost controller.
7	SLP	Slope Compensation for Peak Current Mode Control. Connect a resistor between SLP and AGND to set the desired slope compensation for the current feedback loop.
8	FB	Feedback Analog Input. Connect an external resistive divider from OUT to FB and AGND to set the desired output voltage. Connect to V_{CC} to set the output voltage to 5V.
9	FSW	Switching Frequency Setting. Connect a resistor between FSW and AGND to set the desired frequency.
10	COMP	Error Amplifier Output. Connect the external compensation network of the feedback loop between COMP and AGND for stable operation.
11	PGOOD	Open-Drain, Power Good Output Indicator. An external pullup is required.
12	FSYNC/ SYNCOUT	Connect FSYNC to an external frequency source for synchronization. SYNCOUT is available to output 180° out of phase clock for dual port synchronization.
13	OUT	Switching Regulator Voltage Output. Connect recommended capacitor values between OUT and PGND as per the *Typical Application Circuit.*

Pin Description (continued)

PIN	NAME	FUNCTION
14	CSN2	Negative Input of the Output Side Current-Sense Amplifier. Connect CSN2 to the negative side of the output current-sense resistor.
15	CSP2	Positive Input of the Output Side Current-Sense Amplifier. Connect CSP2 to the positive side of the output current-sense resistor.
16	AGND	Analog Ground of the IC. Connect to ground plane reference of the PCB.
17	V_{CC}	Linear Regulator Output. V_{CC} powers up the internal circuitry. Bypass with 4.7µF ceramic capacitor to AGND.
18	DL2	Boost Low-Side Gate Drive
19	BST2	Bootstrap Capacitor for High-Side Driver of the LX2 Node. Connect a 0.1µF capacitor from BST2 to LX2.
20	DH2	Boost High-Side Gate Drive.
21	LX2	OUT to PGND Switching Output Node. High impedance when the part is off. Connect to one of the external inductor terminals.
22	LX1	IN to PGND Switching Input Node. High impedance when the part is off. Connect to the other external inductor terminal.
23	DH1	Buck High-Side Gate Drive.
24	BST1	Bootstrap Capacitor for High-Side Driver of LX1 Node. Connect a 0.1µF capacitor between BST1 and LX1.
-	EP	Exposed Pad. EP must be connected to the ground plane on the PCB, but it is not a current-carrying path and is needed only for thermal transfer.

Functional Diagram



Detailed Description

The MAX25431 is a current-mode buck-boost H-bridge controller. Based on the input and output voltage of the application, the controller operates in buck or boost mode and transitions seamlessly between these modes to maintain a constant output voltage. The architecture consists of a peak-current-mode control loop that senses the inductor current using an external current-sense resistor. The slope compensation for the current loop can be set using an external resistor. Output voltage is fed back to the IC using a resistor-divider network across the FB pin. The voltage loop is compensated externally using an RC network on the COMP pin.

The operating frequency in the MAX25431 is resistor programmable from 200kHz to 2.2MHz and can be synchronized to an external clock. This provides the designer flexibility to reduce the solution size by using high-frequency operation. Spread spectrum is enabled and helps minimize EMI.

A fast-acting current limit offers reliable overcurrent protection. The current limit can be set by the two external current-sense resistors that work in conjunction to provide a reliable current limit. After an overload condition is detected, the IC shuts down and reattempts startup after some time. The MAX25431 also includes a thermal- shutdown feature with automatic recovery.

Line Regulator Output (V_{CC})

The device includes an internal 5V linear regulator (V_{CC}) that provides power to the internal circuit blocks. The IC powers up once the voltage on V_{CC} crosses the undervoltage-lockout (UVLO) rising threshold and shuts down when V_{CC} falls below the UVLO falling threshold. MAX25431 does not include switchover.

Connect a 4.7µF ceramic capacitor from V_{CC} to AGND.

Synchronization Input (FSYNC)

FSYNC is a logic-level input useful for operating-mode selection and frequency control. Connecting FSYNC to V_{CC} or to an external clock enables fixed-frequency, forced-PWM operation.

The external clock frequency at FSYNC can be lower than the internal clock by 20%. The devices synchronize to the external clock in two cycles. When the external clock signal at FSYNC is absent for more than two clock cycles, the devices use the internal clock. MAX25431ATGA: SYNCIN tracks the MAX25431ATGB SYNCOUT (PWM with spread spectrum). If SYNCIN is not clocked then internal PWM clock is used.

The MAX25431ATGB includes SYNCOUT which outputs a 180° out-of-phase clock and internal PWM mode is enabled. MAX25431ATGB SYNCOUT includes spread spectrum. When used in master-slave configuration add a 10kΩ pull down on VOUT_slave if slave is disabled while SYNCIN is still active.

Power-Good Output (PGOOD)

The device features an open-drain power-good output (PGOOD). PGOOD asserts when V_{OUT} rises above 95% of its regulation voltage. PGOOD deasserts when V_{OUT} drops below 92% of its regulation voltage. Connect PGOOD to V_{CC} with a 10kΩ resistor.

Soft-Start

A fixed-frequency auxiliary oscillator determines the softstart time for the MAX25431. Hence, all output voltages and frequency have a 6.5ms (typ) soft-start time.

Spread-Spectrum

The operating frequency is varied ±3% centered on FSW. The modulation signal is a triangular wave with a period of 110µs at 2.2MHz. Therefore, FSW takes 110µs to ramp down 3% and back to 2.2MHz and the same time in the other direction. The cycle repeats. For operations at FSW values other than 2.2MHz, the modulation signal scales proportionally (e.g., at 400kHz, the 110µs modulation period increases to 110µs x 2.2MHz/0.4MHz = 550µs). The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the FSYNC pin and pass any modulation (including spread spectrum) present on the driving external clock.

Internal Oscillator (FSW)

The switching frequency (f_{SW}) is set by a resistor (RFSW) connected from FSW to AGND. For example, a 420kHz switching frequency is set with R_{FSW} = 73.2kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Overvoltage Protection

The device includes a cycle-by-cycle overvoltage protection. A dedicated internal comparator monitors the output voltage with fixed thresholds. If the output voltage goes higher than 108% (typ) of the regulated value, buck high-side switch (Q_{t1}) and boost low-side switch (Qb2) are turned off. The switching is turned off until the output voltage falls below 106% (typ) of the regulated value.

Short-Circuit Protection

The MAX25431 comes with two separate current-sense signals for a quick and robust short-circuit protection. The current-sense resistor on the input side (R_{CS1}) sets the cycle-by-cycle peak current limit for the device. If the input current hits this peak current limit 16 times consecutively and the output voltage is less than 60% of the regulation value, the device stops switching and enters hiccup mode. The autoretry time in hiccup mode is 26ms (typ). The current sense on the output side (R_{CS2}) sets the runaway current limit. If output current hits the runaway current limit only once while the output voltage is less than 60% of the regulation voltage, the device stops switching and enters hiccup mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +170°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down converter, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 20°C.

Applications Information

Inductor Selection

Design of inductor is a compromise between the size, efficiency, control bandwidth, and stability of the converter. For a buck-boost application, selecting the right value of inductor becomes even more critical due to the presence of right-half-plane (RHP) zero in boost and buck-boost mode. A bigger inductance value would reduce RMS current loss in MOSFETs and core/winding losses in the inductor. On the other hand, it slows the control loop and reduces the frequency of the RHP zero that can cause stability concerns.

Start the inductor selection based on the inductor current ripple as a percentage of the maximum inductor current in buck mode using the equations below. Choose the highest inductance between LBUCK and LBOOST. Minimum duty cycle in buck or boost will yield the highest inductor current ripple.

$$L_{BUCK} > \frac{\left(V_{IN\_MAX} - V_{OUT\_MIN}\right) \cdot D_{BUCK\_MIN}}{f_{SW} \cdot \Delta I_L} \text{ (eq. 1)}$$

$$L_{BOOST} > \frac{V_{IN\_MIN} \cdot D_{BOOST\_MAX}}{f_{SW} \cdot \Delta I_L \cdot V_{IN\_MIN}} \text{ (eq. 2)}$$

$$\Delta I_L = I_{OUT\_MAX} \cdot LIR \text{ (eq. 3)}$$

$$D_{BUCK\_MIN} = \frac{V_{OUT\_MIN}}{V_{IN\_MAX} \cdot \eta_{BUCK}} \text{ (eq. 4)}$$

$$D_{BOOST\_MAX} = 1 - \frac{V_{IN\_MIN} \cdot \eta_{BOOST}}{V_{OUT\_MAX}} \text{ (eq. 5)}$$

L_{BUCK}, L_{BOOST} : minimum inductance needed in buck mode and boost mode, respectively, in H.

f_{SW}: switching frequency in Hz.

V_{IN_MIN} , V_{IN_MAX} : minimum and maximum voltage seen at the power stage input, respectively.

I_{OUT_MAX} : maximum DC output current supported in the application.

LIR : desired peak-to-peak inductor current ripple ratio. Ratio of Δ_{IL}/I_{OUT_MAX}.

D_{BUCK_MIN}, D_{BOOST_MAX} : minimum and maximum duty cycle in Buck and Boost mode, respectively.

η_{BUCK}, η_{BOOST} : efficiency at maximum load in buck mode and boost mode, respectively.

V_{OUT_MIN} : lowest output voltage seen in the application. For fixed PDO applications, use 5.15V (Vsafe5V).

V_{OUT_MAX} : highest output voltage seen in the application. 5.15V, 9V, 15V or 20V for fixed PDOs applications.

Select the final value of inductance considering the ripple in both regions of operation, inductor derating and RHP zero. Once the final value of inductance is selected, calculate the peak inductor current and choose an inductor with saturation current approximately 20% more than the peak inductor current. Low DCR helps achieve higher efficiency by reducing inductor conduction loss during high output power with low input voltage.

Example

P_{OUT_MAX} = 100W ; V_{IN_MIN} = 6V ; V_{IN_MAX} = 18V ; V_{OUT_MIN} = 5.15V ; V_{OUT_MAX} = 20V ; f_{SW} = 400kHz ; I_{OUT_MAX} =5A ; η_{BUCK} = η_{BOOST} = 95% ; LIR is chosen to be 55% to keep the inductor small.

For this example, L_{BUCK} > 3.5 uH and L_{BOOST} > 3.9 uH. Therefore, an inductor with a value of 4.7µH will be selected.

Inductor saturation current must be considered when choosing the inductor.

The high input current seen during low V_{IN}/High P_{OUT} conditions has an impact on the current saturation rating of the inductor and therefore its size. The MAX25431 advantage is its flexibility with regards to output power thanks to its scalable peak input current limit. When selecting the input current sense resistor value (R_{CS1}), consider the output power, inductor saturation current, minimum input voltage seen at the power stage but also the minimum V_{BUS} voltage to meet at the user port. When the peak input current reaches the I_{OC1} threshold defined by R_{CS1}, the controller will

automatically enter cycle-by-cycle input current limit which may cause V_{BUS} to droop below the minimum specification at the port. Cable compensation will not increase V_{BUS} in this condition as the input current (and therefore the input power) is limited.

Once the input sense resistor value is selected, the inductor saturation current rating (I_{SAT}) value can be chosen. The I_{SAT} value must be higher than the input peak I_{LIM} threshold by some safe margin to avoid saturating the core.

$$I_{SAT} > I_{OC1\_MAX}$$

$$I_{SAT} > \frac{V_{OC1\_MAX}}{R_{CS1}}$$

Example

R_{CS1} = 3mΩ and V_{OC1_MAX} = 60mV yields I_{OC1_MAX} = 20A, therefore:

$$I_{SAT} > 20A$$

Input Capacitor Design

The input capacitor reduces peak currents drawn from the power source and minimizes noise and voltage ripple on the input caused by the circuit switching. In buck mode, input current is discontinuous with maximum ripple. The RMS current is shown in the following equation:

$$I_{RMS} = \frac{I_{OUT\_MAX} \cdot \sqrt{V_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}}{V_{IN}} \text{ (eq. 6)}$$

The maximum input RMS current occurs at V_{IN} = 2 x V_{OUT}. Substituting V_{IN} previously, the equation then becomes:

$$I_{RMS\_MAX} = \frac{I_{OUT\_MAX}}{2} \text{ (eq. 7)}$$

The input voltage ripple in buck mode is given by:

$$\Delta V_{IN} = \frac{\left(1 - D_{BUCK}\right) \cdot I_{OUT} \cdot D_{BUCK}}{f_{SW} \cdot C_{IN}} \text{ (eq. 8)}$$

It is recommended to keep the input voltage ripple below 1% of the input voltage to limit noise that could be conducted through the battery harness.

Maximum input voltage ripple occurs in buck mode at a duty cycle of 0.5 and at max output current. Select a higher value for the final capacitor or bank of capacitors to account for DC Bias and tolerance derating.

Use the following equation to determine the input capacitance needed to meet the input voltage ripple requirement:

$$C_{IN} > \frac{0.25 \cdot I_{OUT\_MAX}}{f_{SW} \cdot \Delta V_{IN\_MAX} \cdot \left(1 - \left(C_{IN\_TOL} + C_{IN\_DCBIAS}\right)\right)} \text{ (eq. 9)}$$

Example

*f_{SW} = 400kHz ; I_{OUT_MAX} =5A ; D_{BUCK} = 0.5 ; C_{IN_TOL} = 10% ; C_{IN_DCBIAS} = 10% ; ΔV_{IN_MAX} = 12V * 0.01 = 0.12V*

For this example, C_{IN} > 27µF.

Select the input capacitor that can handle the given RMS current at the operating frequency. Ceramic capacitors come with extremely low ESR and help reduce the peak-to-peak ripple voltage at the input voltage. Good quality electrolytic capacitors are also available with low ESR, which give higher capacitance at low cost.

Electrolytic (bulk) input capacitors help reduce input voltage drop during large load transients. ESR in bulk capacitors help dampen line transients. A good combination of electrolytic and ceramic capacitors can help achieve the target specifications and minimize cost.

Place a high-frequency decoupling ceramic capacitor to filter high di/dt and reduce EMI caused by Qt1 turn on. Choose a small package, such as 0402, with low ESL.

Choose a voltage rating of 50V for applications where a 40V load dump can be seen at the input.

Output Capacitor Design

Output capacitance is selected to satisfy the output load-transient requirements. During a load step, the output current changes almost instantaneously whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. Select a capacitor based on the maximum allowable overshoot/undershoot on the output voltage. Typically, the worst-case response from a load transient is in boost mode. Use the following equations to contain the undershoot within the given specifications in boost mode:

$$C_{OUT} \geq \frac{L \times \Delta I_{LSTEP}^2}{2 \times V_{SUP\_MIN} \times D_{MAX} \times V_{UNDER}} + \frac{(\Delta I_{LSTEP} \times \Delta t_{DELAY})}{V_{UNDER}}$$

where t_{DELAY} = Time delay for the next control pulse after a load step. For fixed-PWM mode, t_{DELAY} is the turn-off time in buck/boost mode.

Select the output capacitance to handle load transients in deep boost mode. t_{DELAY} is the delay for the PWM modulator to react after a load step. In PWM mode, the worst-case delay would be (1-D) x t_{SW} when the load step occurs right after a turn-on cycle. With the previous example values:

$$C_{OUT} \geq 120\mu F$$

Once the output capacitance is selected, the output voltage undershoot/overshoot can be calculated for buck region of operation using the following equations:

$$V_{UNDER\_BUCK} = \frac{L \times \Delta I_{LSTEP}^2}{2 \times (V_{SUP} - V_O) \times D_{MAX} \times C_{OUT}}$$

$$V_{OVER\_BUCK} = \frac{L \times \Delta I_{LSTEP}^2}{2 \times V_O \times C_{OUT}}$$

Output-Voltage Setting

Connect FB to V_{CC} to enable the fixed output voltage (5V) set by a preset internal resistive voltage-divider connected between the feedback (FB) pin and AGND. To externally adjust the output voltage between 4V and 25V, connect a resistive divider from the output (OUT) to FB to AGND (Figure 1). Calculate RFB1 and RFB2 with the following equation:

$$R_{FB1} = R_{FB2}[(\frac{V_O}{V_{FB}}) - 1]$$

where V_{FB} = 1.25V (typ). See the *Electrical Characteristics* table.

Current-Sense Resistor Selection

The MAX25431 uses two external current-sense resistors for inductor current control and current-limit implementation. Input current-sense resistor feedback is used for the current loop, setting the peak current limit and PFM current limit. Output current-sense information is used for runaway current limit.

Select an input current-sense resistor based on the maximum input current for the application (typically at minimum at input voltage). The differential voltage across R_{CS1} for input current-limit threshold is 50mV. Calculate the peak input current using this equation:

$$I_{INPEAK} = \frac{V_O \times I_O}{V_{SUPMIN}} + \frac{V_{SUPMIN} \times (1 - \frac{V_{SUPMIN}}{V_O})}{L \times f_{SW} \times 2}$$

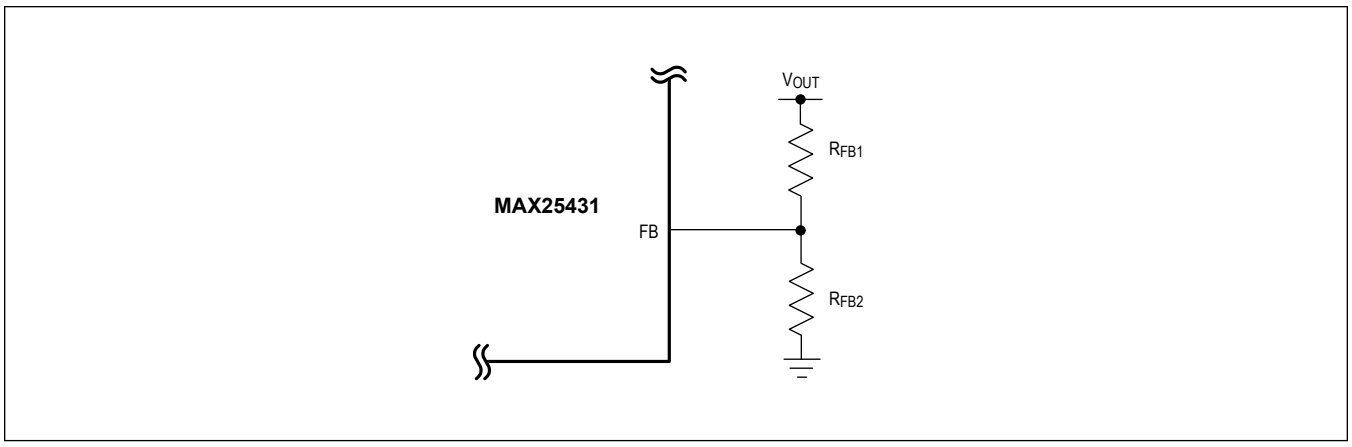


Figure 1. Setting the Output Voltage for the MAX25431

Calculate the current-sense resistor by setting the peak current limit (I_{LIM}) slightly higher than the peak input current (I_{INPEAK}) calculated above.

$$R_{CS1} = \frac{50mV}{I_{LIM}}$$

Since one event of runaway current limit would make the controller enter hiccup mode, design the runaway current limit higher than the peak current to keep a safe margin. The MAX25431 has internal runaway current limit set to 50% higher than peak current limit (i.e., 75mV), which enables the designer to use the same current-sense resistors on input and output.

$$R_{CS2} = \frac{75mV}{I_{LIM-RUNAWAY}}$$

Slope Compensation

An external slope compensation is typically required for current-mode control due to its inherent instability. A properly designed current-mode control with external slope compensation removes the instability and provides noise immunity from current-sense signals. The MAX25431 offers a simple way to set the slope compensation by connecting a resistor between SLP pin and AGND. The resistor for slope compensation can be calculated using equation the below:

$$R_{SLOPE} = \frac{1.25V \times 0.09}{V_{p2p}} \times \frac{1}{8pF \times f_{SW}}$$

Design the slope compensation to lower the quality factor of the double pole at half the switching frequency of current-mode control (Q_P) given by equation:

$$Q_P = \frac{1}{\pi \times (m_c \times D' - 0.5)}$$

where m_C, the compensation ramp factor, is given by:

$$m_c = 1 + \frac{S_e}{S_n}$$

S_e = Slope of the external ramp

S_n = Rising slope of inductor current

V_{p2p} = The peak-to-peak voltage of the external slope compensation

Error-Amplifier Compensation Design

The MAX25431 uses an internal transconductance amplifier with its inverting input and output terminals available to the user for external frequency compensation, as shown in Figure 2.

The controller uses a peak current-mode-controlled architecture to regulate the output voltage by forcing the required current through the external inductor. The external current-sense resistor senses the inductor current information. The current-mode control splits the double pole in the feedback loop caused by the inductor and output capacitor into two single poles. One of the poles is moved to a high frequency outside the typical bandwidth of the converter, making it a single-pole system. This makes compensation easy with only Type II required to compensate the loop. In boost mode, an extra right-half plane (RHP) zero is introduced by the power stage to add extra phase delay in the control loop. To avoid any significant effect of the RHP zero on the converter stability, the compensation is designed such that the bandwidth is approximately 1/4 of the worst-case RHP zero frequency.

The design of external compensation requires some iterations to reach an optimized design. Care must be taken while designing the compensation for working in 'deep' boost mode and heavy load (V_{SUP_MIN}) as RHP zero frequency reduces.

A convenient way to design compensation for both buck and boost modes is to design the compensation at minimum input voltage and heavy load (deep boost mode). At this operating point, RHP zero is at its lowest frequency. Design the compensation to achieve a bandwidth close to 1/4 of the RHP zero frequency in deep boost mode. Verify the gain and phase margin with the designed compensation in buck mode. The closed-loop gain of the converter is a combination of the power-stage gain of the converter and error-amplifier gain.

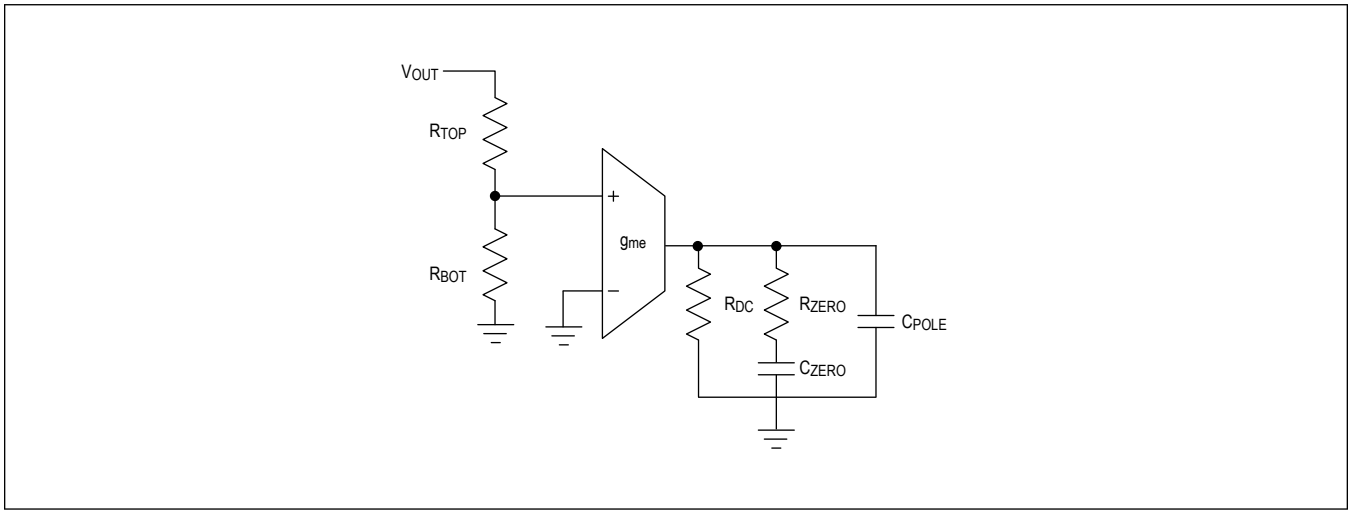


Figure 2. Setting the Output Voltage for the MAX25431.

$$\frac{\hat{V}_O}{\hat{V}_C} = \frac{R_L \times (1 - D)}{G_{CS} \times 2} \times \frac{(1 + \frac{S}{\omega_{ESR}}) \times (1 - \frac{S}{\omega_{RHP}})}{(1 + \frac{S}{\omega_{p\_BOOST}}) \times F_H(s)}$$

where:

G_{CS} = Current-sense gain = R_{CS1} x 24

R_{CS1} = Sense resistor connected to CSP1:

$$\omega_{P\_BOOST} = \frac{2}{R_L \times C_{OUT}};$$

$$\omega_{ESR} = \frac{1}{R_C \times C_{OUT}};$$

$$\omega_{RHP} = \frac{R_L \times (1 - D)^2}{L};$$

$$F_H(S) = 1 + \frac{S}{\omega_N \times Q_P} + \left(\frac{S}{\omega_N}\right)^2$$

$$Q_P = \frac{1}{\pi \times (m_C \times D' - 0.5)};\ \omega_N = \frac{\pi}{T_{SW}}$$

Error-amplifier transfer function:

$$H_{EA}(S) = g_m \times R_{DC} \frac{\left(1 + \frac{S}{\omega_{Z\_COMP}}\right)}{\left(1 + \frac{S}{\omega_{p1\_COMP}}\right) \times \left(1 + \frac{S}{\omega_{P2\_COMP}}\right)}$$

where:

$$\omega_{Z\_COMP} = \frac{1}{R_{ZERO} \times C_{ZERO}}$$

$$\omega_{P1\_COMP} = \frac{1}{R_{DC} \times C_{ZERO}}$$

$$\omega_{P2\_COMP} = \frac{1}{R_{ZERO} \times \frac{(C_{POLE} \times C_{ZERO})}{(C_{POLE} + C_{ZERO})}}$$

$$\cong \frac{1}{R_{ZERO} \times C_{POLE}} \text{ if } C_{POLE} << C_{ZERO}$$

Closed loop gain:

Closed loop gain = Power stage gain x EA gain

External MOSFET Selection

Four external MOSFETs are required for the H-bridge buck-boost architecture supported by the MAX25431, as shown in the *Typical Application Circuit*. During the buck-mode of operation, Q_{t2} remains on and Q_{b2} remains off. Q_{t1} and Q_{b1} switch to regulate the output voltage. During the boost mode, Q_{t1} remains on, Q_{b1} remains off, and Q_{t2} and Q_{b2} switch to regulate the output voltage. In the buck-boost region, all four switches are used to control the output voltage. The MOSFETs must be selected based on certain critical parameters such as on-resistance, breakdown voltage, output capacitance, and input capacitances. A low R_{DSON} reduces the conduction losses in the MOSFET and a small gate/output capacitance reduces switching losses. Typically, a lower R_{DSON} MOSFET would have higher gate charge for the same breakdown voltage. Hence, a compromise must be made depending on conditions to which the MOSFET is subjected.

The MAX25431 comes with a 5V gate drive with a high current capability to support switching of 4 MOSFETs at high frequency. In the buck-boost region, the device switches between pure buck and boost modes to reduce the gate-drive current and increases the efficiency.

Boost Cap and Diode Selection

A boost-strap circuit is used to drive the floating gates of high-side switches Q_{t1} and Q_{t2}. Boost cap provides the gate charge to the high side FET during the high-side turn-on and is recharged when the bottom switch turns on. Hence, the capacitance value of the boost capacitor must be selected such that the voltage drop during the discharge is under acceptable limits. Choosing a very large capacitor value slows down the charging of the capacitor, and it might not completely charge in the minimum off-time of the top switch.

Select the boost diode based on the average gate-drive current and blocking voltage for the diode. The maximum blocking voltage for the diode must be high enough to block the maximum drain-to-source voltage for the FET. A fast reverse-recovery diode would prevent any current being sourced into the bias supply from drain-to-source voltage. For the MAX25431, the gate drive is powered by the V_{CC} regulator, which is 5V (typ).

Since boost capacitor provides the gate charge to top switch, the value of boost capacitance needed for less than a Δ_{VBOOST} ripple on boost capacitor can be written as:

$$C_{BOOST} \geq \frac{Q_G}{\Delta V_{BOOST}}$$

Average gate-drive current through the diode can be calculated as:

$$I_G = Q_g \times f_{SW}$$

where Q_g = Total gate charge of the top MOSFET.

Start the design by setting the output voltage and switching frequency for the controller. Selecting R_{FB2} = 10kΩ gives R_{FB1} = 86kΩ, to set the output voltage to 12V. Connect a 13kΩ resistor between the FSW and AGND pins to set the switching frequency to 2MHz.

Selecting the Current-Sense Resistor

The input current-sense resistor sets the peak current limit of the converter. For a 5A (max) output current, the maximum input current is 20A. The peak current-limit threshold for the input current sense is 50mV (typ).

$$I_{LPEAK} = \frac{V_O \times I_O}{V_{SUPMIN}} + \frac{V_{SUPMIN} \times (1 - \frac{V_{SUPMIN}}{V_O})}{L \times f_{SW} \times 2} = 15.55$$

Hence, the input current-sense resistor must be selected such that the peak current limit is higher than the peak input current. For this application:

$$\text{Select } R_{CS1} = 3m\Omega;\ I_{LIM} = \frac{50mV}{3m\Omega} = 16.67A$$

The runaway current limit is set by the output currentsense resistor at a 75mV threshold. Select the output current-sense resistor such that the runaway current limit is higher than the peak current limit by some safe margin:

$$\text{Select } R_{CS2}=3m\Omega;\ I_{LMIN-RUNAWAY} = \frac{75mV}{2m\Omega} = 25A$$

Table 1. Design Example

PARAMETERS	VALUE
V_{OUT}	12
f_{SW}	2MHz
V_{SUP}	4V–18V
I_{OUT}	5A (max)

Inductor Design

Start inductor selection by assuming 30% current ripple in buck mode, which gives the inductor to be:

$$L_{BUCK} > \frac{(V_{SUPMAX} - V_O) \times V_O}{f_{SW} \times I_{L\_MAX} \times \%\ \Delta I_{RIPPLE} \times V_{SUPMAX}} = 1.33\mu H$$

For a converter operating in boost mode, the inductor selection determines the RHP frequency and hence the stability of converter in deep boost mode. Calculate the RHP zero frequency in deep boost mode using the calculated inductor value:

$$\omega_{RHP} = \frac{R_L \times (1 - D)^2}{L \times 2\pi} = 31.93kHz$$

With RHP zero at 31.93kHz, the loop cutoff frequency for a stable operation must be less than 1/4 of the RHP zero frequency in deep boost mode.

Select L = 1.2µH, ω_{rhp} = 35.4kHz

Select a 1.2µH inductor to give a target crossover frequency of approximately 9kHz. Inductor current ripple in boost mode can now be verified using this value of the inductor:

$\%\Delta I_{RIPPLE(BOOST)} >$

$$\frac{(1-\frac{V_{SUPMIN}}{V_O})\times V_{SUP(MIN)}}{f_{SW}\times I_{L(MAX)}\times L}\times 100 = 7.4\ \%$$

Output Capacitor Design

Select the output capacitance to handle load transients in deep boost mode. t_{DELAY} is the delay for the PWM modulator to react after a load step. In PWM mode, the worst-case delay would be (1-D) x t_{SW} when the load step occurs right after a turn-on cycle.

$$C_{OUT} \geq \frac{L\times \Delta I_{LSTEP}^{2}}{2\times V_{SUP\_MIN}\times D_{MAX}\times V_{UNDER}} + \frac{(\Delta I_{LSTEP}\times \Delta t_{DELAY})}{V_{UNDER}} = 88.54\mu F$$

Slope Compensation

Select the slope-compensation resistor to have a worst-case Q_p value of approximately 0.6. Since the slope compensation is fixed once the resistor is selected, design for maximum input voltage:

For Q_p = 0.6, m_c = 3.12

$$S_n = \frac{(V_{SUP(MAX)} - V_O)\times G_{CS}}{L} = 3.525\times 10^5 V\Big/ s$$

For m_c = 3.12,

S_e = 7.05 x 10^5 V/s, V_{p2p} (external slope) = 360mV

Calculate R_{SLOPE} to achieve the desired peak-to-peak voltage for the external compensation as calculated above.

Select R_{SLOPE} = 18kΩ for $V_{P2P} \cong$ 390mV

Error-Amplifier Compensation Design

Start the compensator design by calculating the critical frequencies for the boost power stage at the minimum input voltage and maximum load.

$$f_{PBOOST} = \frac{2}{2\pi\times R_L\times C_{OUT}} = 1.3kHz$$

$$f_{ESR} = \frac{1}{2\pi\times R_C\times C_{OUT}} = 531kHz f_{RHP} = \frac{R_L\times (1-D)^2}{2\pi\times L} = 35kHz$$

With RHP zero at 35kHz, a target bandwidth for the closed-loop converter close to 9kHz is selected. The zero of the error amplifier must be placed well below the bandwidth to give enough phase boost at the crossover frequency. Typically, the zero is placed close to the low-frequency pole. In such a case, resistor (R_{ZERO}) of the compensation can be calculated using equation below:

$$R_{ZERO} = 2\pi f_{BW}\times \frac{G_{CS}\times C_{OUT}}{gm\times (1-D_{BOOST})}\times \frac{(R_{BOT}+R_{TOP})}{R_{BOT}}$$

Choosing:

f_{BW} = 9kHz; gives R_{ZERO} = 16kΩ

with:

f_{ZCOMP}=1.5 kHz;

$$C_{ZERO} = \frac{1}{R_{ZERO}\times 2\pi\times f_{ZCOMP}} = 6.58nF$$

C_{pole} decides the location of high-frequency pole. Select the high-frequency pole location higher than the bandwidth in buck mode so that it does not affect the phase margin and helps attenuate any high-frequency noises.

$$C_{POLE} = \frac{1}{R_{ZERO} \times 2\pi f_{p2COMP}}$$

For f_{p2COMP} = 200kHz, C_{POLE} = 50pF

Select R_{ZERO} = 16kΩ, C_{ZERO} = 5.6nF and C_{POLE} = 50pF

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1. Arrange the high-power components in a compact layout away from the sensitive signals such as the current-sense and gate-drive signals, etc., to avoid stray noise pickup.
2. Place the input capacitor and the input current-sense resistor close to the input MOSFETs (Qt1 and Qb1) to make a small input current AC loop. High-frequency AC currents flow in this loop in buck mode (Figure 3) and a small loop helps with the EMI and noise performance. Add high-frequency decoupling caps to improve the high-frequency performance.
3. Place the output capacitor and the output current-sense resistor close to the output MOSFETs (Q_{t2} and Q_{b2}) to make a small output-current AC loop. High-frequency AC currents flow in this loop in boost mode (Figure 3) and a small loop helps with the EMI and noise performance. Add high-frequency decoupling caps to improve the high-frequency performance.
4. The switching nodes (LX1 and LX2) carry high-frequency, high-current switching signals. Make LX1 and LX2 areas small to reduce parasitic inductance in the switching nodes. Since high currents flow through these nodes, a compromise must be made between thermal dissipation and noise mitigation.
5. Use a Kelvin sense connection for the current-sense resistors and route the sense traces close to each other to ensure a balanced measurement of the differential signal. Route these traces away from other noisy traces.
6. Use short and thick traces for gate connection to avoid any gate ringing.
7. Using internal PCB layers as a ground plane helps to improve the EMI functionality. A solid ground plane like the inner layer act as a shield against radiated noise. Have multiple vias spread around the board, especially near the ground connections, to have better overall ground connection.
8. Connect the PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.
9. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer.
10. Keep the bias capacitor (C_{BIAS}) close to the device to reduce the bias current loop. This helps to reduce noise on the bias for smoother operation.

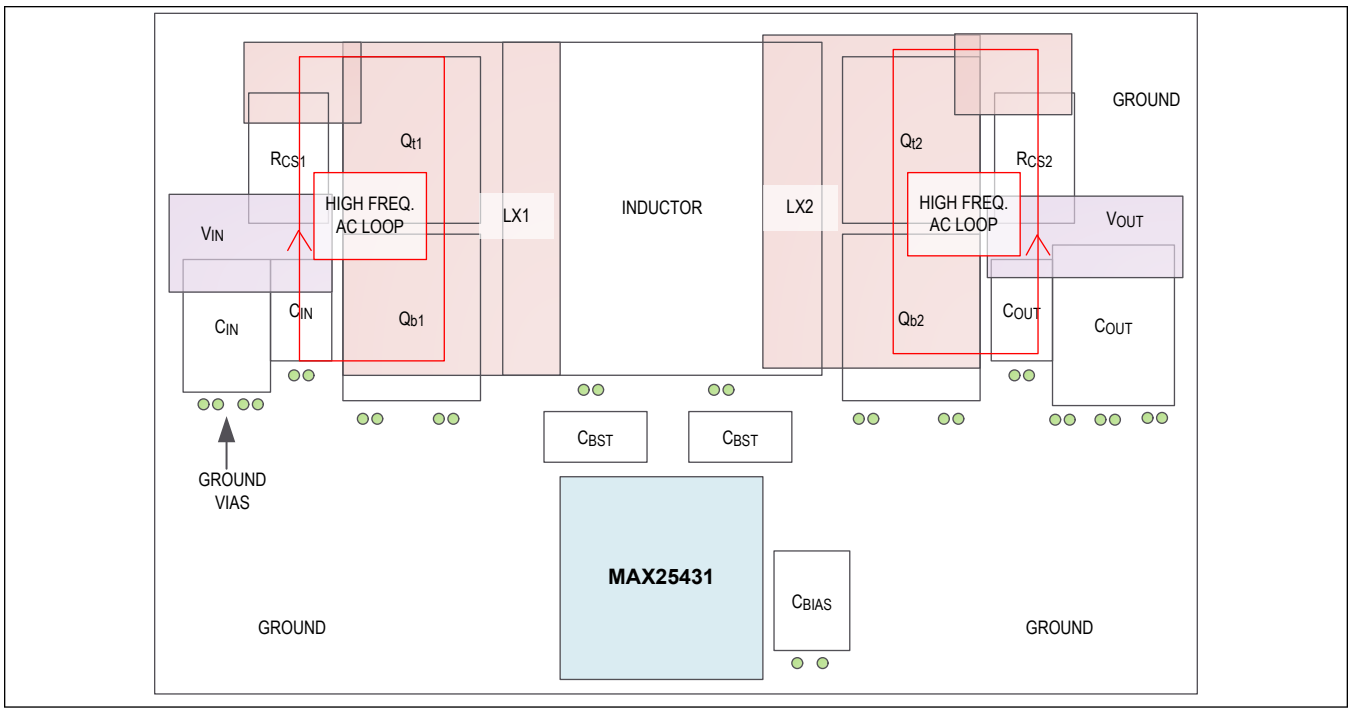
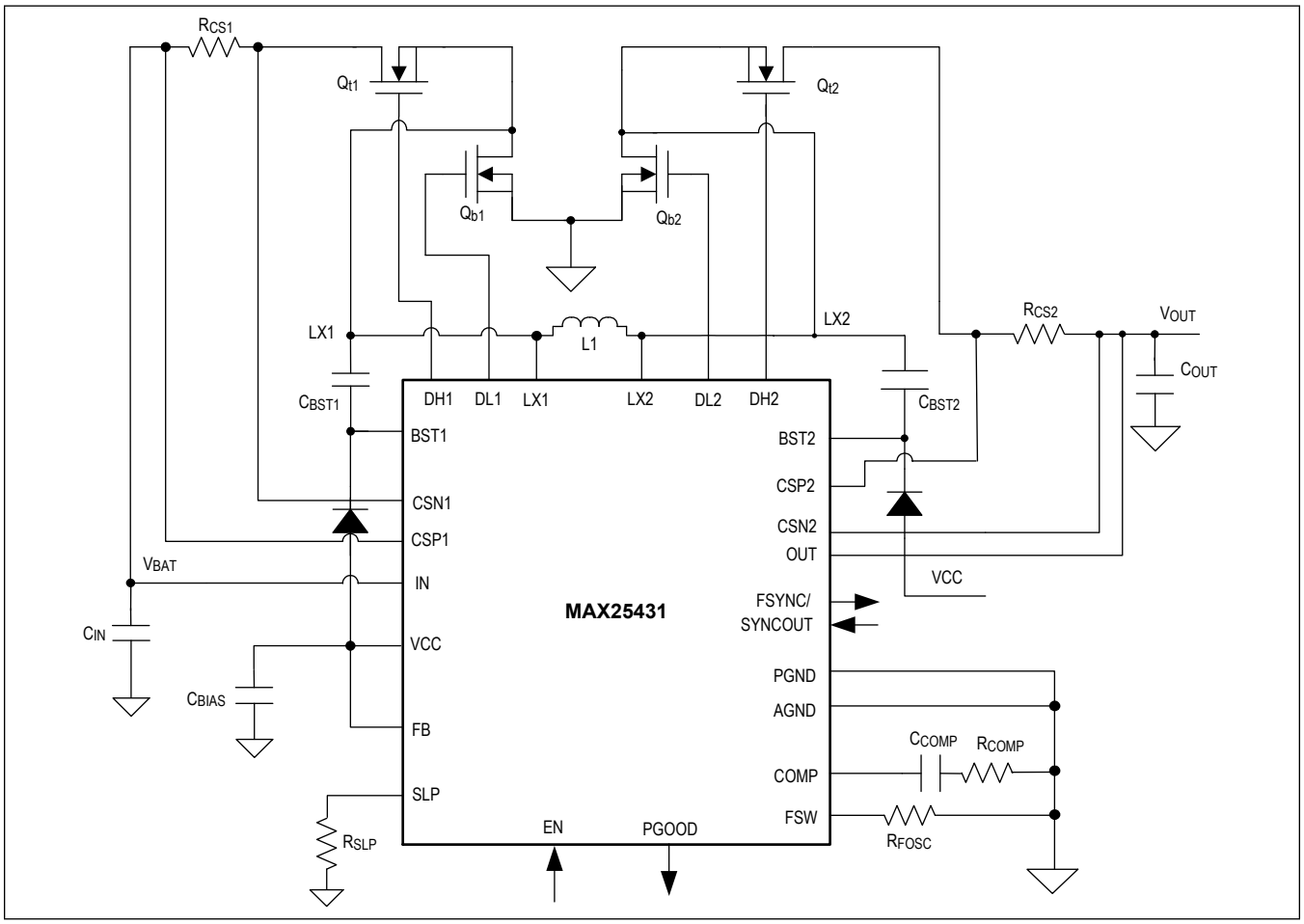


Figure 3. Recommended PCB Layout for the MAX25431.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT}	FSYNC/ SYNCOUT	SPREAD SPECTRUM
MAX25431ATGA/VY+	-40°C to +125°C	24 SWTQFN	5V (fixed), ADJ	FSYNC	ON
MAX25431ATGB/VY+	-40°C to +125°C	24 SWTQFN	5V (fixed), ADJ	SYNCOUT	ON

/V Denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Y Denotes a side-wettable package

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/19	Initial release	—
1	8/20	FSYNC/SYNCOUT corrected in Ordering Information, Junction-to-Ambient and Junction-to-Case thermals updated, Continuous Power Dissipation updated, Skip Mode details removed, FSYNC/SYNCOUT pin description updated, Functional Diagram removed skip blocks and switchover block, Light-Load Operation section removed, Inductor section updated, Input Capacitor Section updated, Output Capacitor Design section updated, Slope comp, QP and mc defined	1, 2, 6, 9, 10, 11, 12, 13, 14, 16, 20