ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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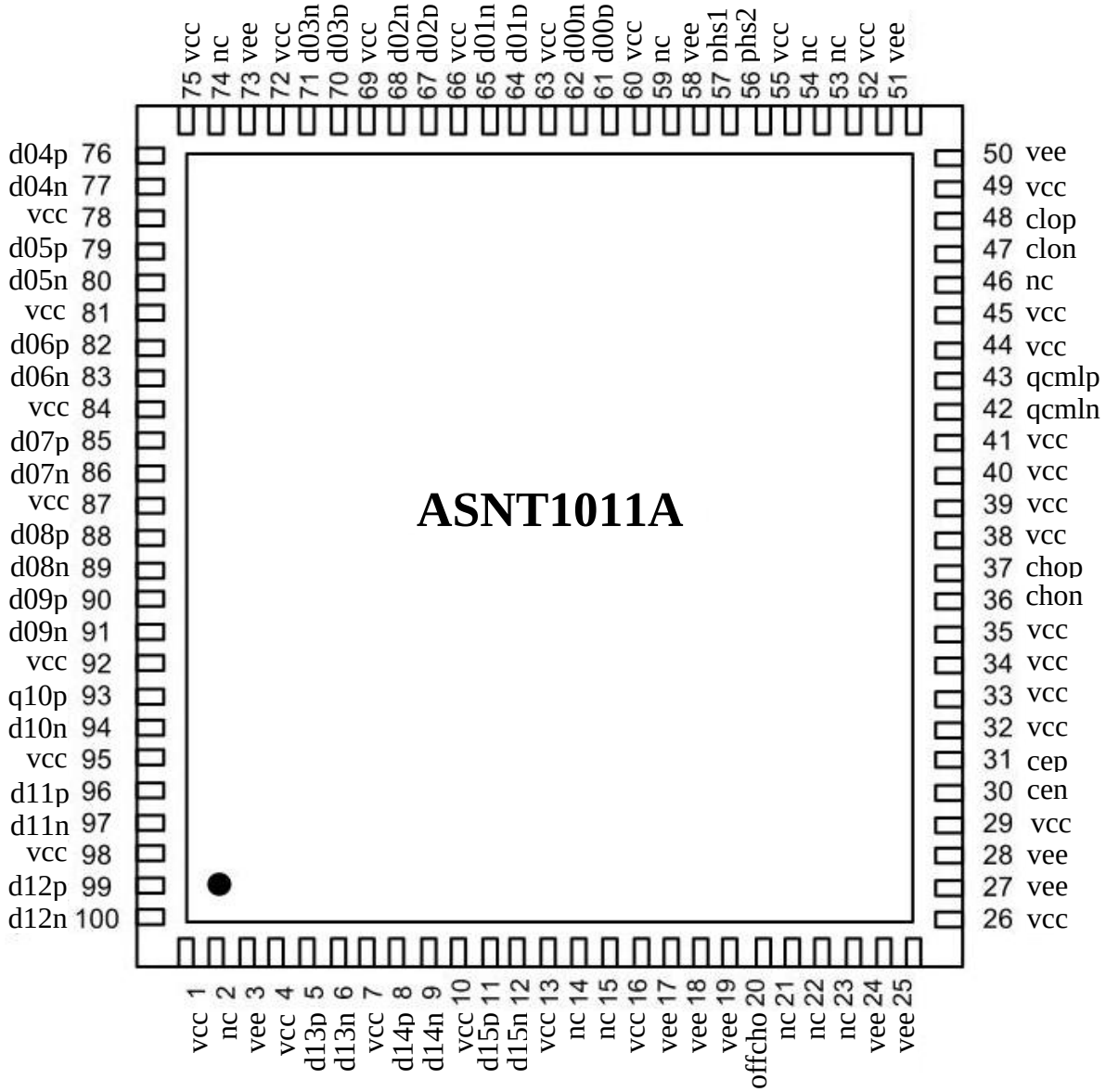
ASNT1011A-PQA
DC-to-17*Gbps* Digital Multiplexer 16:1 / Serializer

- Broadband digital serializer 16-to-1.
- LVDS compliant input data buffers.
- Full-rate clock output.
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 660*mW* at the maximum speed.
- Custom 100-pin QFN package (12*mm* x 12*mm*).



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DESCRIPTION

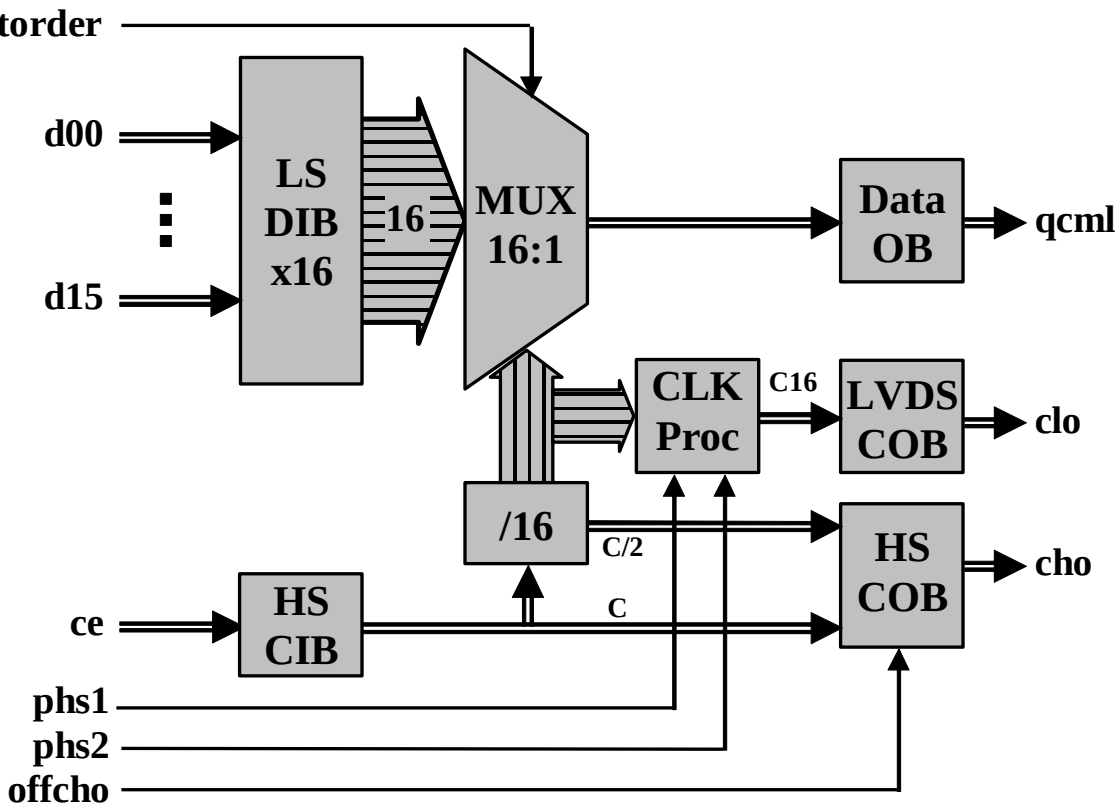

Fig. 1. Functional Block Diagram.

ASNT1011A-PQA is a low power and high-speed digital 16-to-1 multiplexer (MUX) / serializer IC. The IC shown in Fig. 1 functions seamlessly over data rates (f_{bit}) ranging from DC to 17*Gbps*.

The main function of the IC is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high speed serial bit stream running at f_{bit}. It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words "d00"-"d15" through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. A full rate clock must be provided by an external source ("ce") to the high-speed clock input buffer (HS CIB) where it is routed to the high speed clock output buffer (HS COB) and the internal divider-by-16 (/16). The divider provides signaling for MUX16:1 and produces clock divided-by-16 "C16" for the low speed LVDS compliant clock output buffer (LVDS COB). The phase of "clo" can be modified by 90° increments by utilizing pins "phs1" and "phs2" and the clock processing block (CLK Proc). By utilizing pin "bitorder", the serializer can designate either "d00" or "d15" as the MSB thus simplifying the interface between the multiplexer and a proceeding ASIC.

The serialized words are transmitted as 2-level signals "qcml" by a differential CML output buffer (Data OB). A full-rate clock is transmitted by HS COB in parallel with the high-speed data. The clock and data outputs are

well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. Both output stages are back terminated with on-chip 50*Ohm* resistors.

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that exceed the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative ("vee") and positive ("vcc") supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV*p-p and threshold voltages between "vee" and "vcc". The input termination impedance is set to 100*Ohm* differential.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can accept high-speed clock signals at its differential CML input port "cep/cen". It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to "vcc" for each input line.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock "C" is fed into the first divide-by-2 circuit that generates half rate clock "C2". "C2" is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. "C16" is passed on to LVDS COB to become the output low speed clock signal "clo".

MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the "C16" clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a single serial data stream running at a data rate up to 17*Gbps*. The latency of this circuit block is equal to roughly one period of "C16". The input MSB corresponds to "d00" when "bitorder"=0 (default), or to "d15" when "bitorder"=1.

Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into differential CML output signal "qcmlp/qcmln". The buffer requires 50*Ohm* external termination resistors connected between ""vcc" and each output to match its internal 50*Ohm* resistors.

HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 15*GHz* while producing a single-ended CML output swing of 600*mV*. The buffer can be enabled or disabled by the external 3-state (vcc, vee, not connected (n/c)) control signal "offcho". The

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n/c default state corresponds to a “C2” output signal. The logic “0” state provides a full-rate clock output signal while the logic “1” state disables the buffer completely to save power.

CLK Proc

By utilizing the CMOS control pins “phs1” and “phs2”, the phase of “clo” can be altered in accordance with Table 1.

Table 1. Output Clock Phase Selection.

“phs1”	“phs2”	C16 phase
“vee” (default)	“vee” (default)	270°
“vee”	“vcc”	180°
“vcc”	“vee”	90°
“vcc”	“vcc”	0°

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives “C16” and converts it into an LVDS output signal “clo”. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a nominal output current of 3.5*mA*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Output Timing

The phase relation between the output data “qcml” and the full rate output clock “cho” is specified in Table 2 and illustrated by Fig. 2.

Table 2. Output Data-to-Clock Phase Difference.

Junction temperature, *°C*	**τ**,*ps*	
	Min.	Max.
-25	77	80
50	82	86
125	87	91

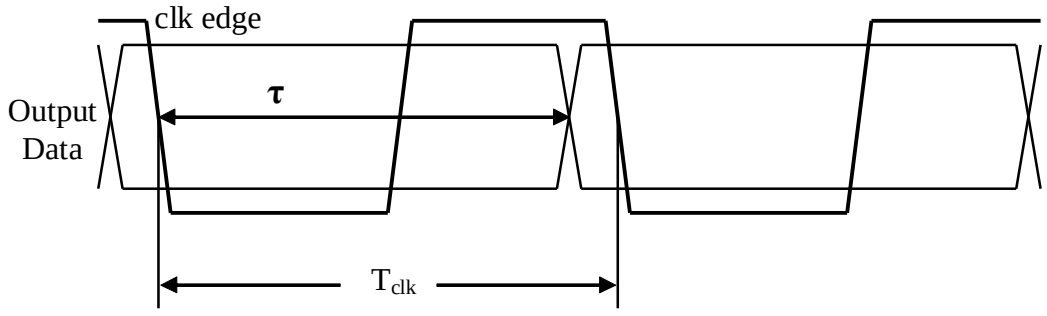

Fig. 2. Output Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed "vee").

Table 3. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Supply Voltage ("vee")		+3.6	*V*
Power Consumption		0.72	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Supply And Termination Voltages		
Name	Description	Pin Number
vcc	Positive power supply. (+3.3*V*)	1, 4, 7, 10, 13, 16, 26, 29, 32-35, 38-41, 44, 45, 49, 52, 55, 63, 66, 69, 72, 75, 78, 81, 84, 87, 92, 95, 98.
vee	Negative power supply. (GND or 0*V*)	3, 17-19, 24, 25, 27, 28, 50, 51, 58, 73.
nc	Not connected pins	2, 14, 15, 21-23, 46, 53, 54, 59, 74.

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cep	31	Input	CML differential external clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	30		
chop	37	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to "vcc".
chon	36		
qcmlp	43	Output	CML differential data outputs. Require external SE 50*Ohm* termination to "vcc".
qcmln	42		
Controls			
phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low).
phs2	56		
offcho	20	LS In., CMOS	HS COB control (active: high, buffer is disabled; default: low, full-rate output clock).
bitorder	60	LS IN., CMOS	Input bit order selection (active: high, d15 is serialized first; default: low, d00 is serialized first)

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TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
clop	48	Output	LVDS clock outputs. Can transmit four different clock phases as defined by “phs1” and “phs2”.
clon	47		
d00p	61	Input	LVDS data inputs.
d00n	62		
d01p	64		
d01n	65		
d02p	67		
d02n	68		
d03p	70		
d03n	71		
d04p	76		
d04n	77		
d05p	79		
d05n	80		
d06p	82		
d06n	83		
d07p	85		
d07n	86		
d08p	88		
d08n	89		
d09p	90		
d09n	91		
d10p	93		
d10n	94		
d11p	96		
d11n	97		
d12p	99		
d12n	100		
d13p	5		
d13n	6		
d14p	8		
d14n	9		
d15p	11		
d15n	12		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
Ivcc		200		*mA*	
Power consumption		660		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Data (d00p/d00n-d15p/d15n)					
Data Rate	0.0	937.5	1063	*Mbps*	
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	"vee"		"vcc"	*V*	
HS Input Clock (cep/cen)					
Frequency	0.0	15	17	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	"vcc"-0.8		"vcc"	*V*	
Duty Cycle	40%	50%	60%		
HS Output Data (qcmlp/qcmln)					
Data Rate	0.0	15	17	*Gbps*	
Logic "1" level		"vcc"		*V*	
Logic "0" level		"vcc"-0.6		*V*	
Jitter		12		*ps*	Peak-to-peak @12.5*Gb/s*
HS Output Clock (chop/chon)					
Frequency	0.0	15	17	*GHz*	
Logic "1" level		"vcc"		*V*	
Logic "0" level		"vcc"-0.6		*V*	
Jitter		6		*ps*	Peak-to-peak @12.5*GHz*
Duty Cycle		50%			
LS Output Clock (clop/clon)					
Frequency	0.0	937.5	1063	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS Control Inputs					
Logic "1" level	"vcc"-0.4			*V*	
Logic "0" level			"vee"+0.4	*V*	

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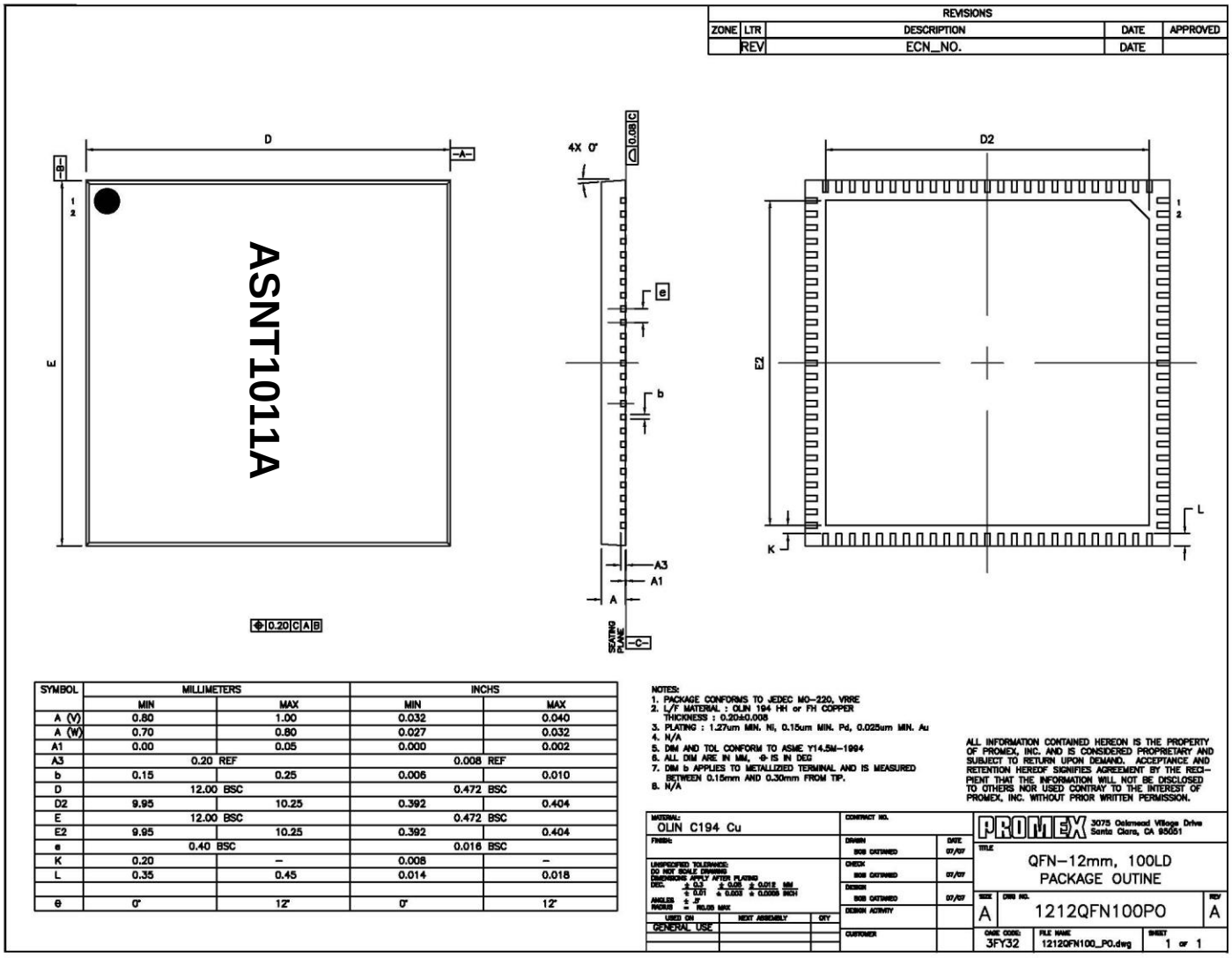
PACKAGE INFORMATION

The chip die is housed in a custom 100-pin QFN package shown in Fig. 3.



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A (V)	0.80	1.00	0.032	0.040
A (W)	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	12.00 BSC		0.472 BSC	
D2	9.95	10.25	0.392	0.404
E	12.00 BSC		0.472 BSC	
E2	9.95	10.25	0.392	0.404
e	0.40 BSC		0.016 BSC	
K	0.20	–	0.008	–
L	0.35	0.45	0.014	0.018
θ	0°	12°	0°	12°

NOTES:
1. PACKAGE CONFORMS TO JEDEC MO-220, VRRE
2. L/F MATERIAL : OLIN 194 HH or FH COPPER THICKNESS : 0.20±0.008
3. PLATING : 1.27um MIN. Ni, 0.15um MIN. Pd, 0.025um MIN. Au
4. N/A
5. DIM AND TOL CONFORM TO ASME Y14.5M-1994
6. ALL DIM ARE IN MM, ⌀ IS IN DEG
7. DIM b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TIP.
8. N/A

MATERIAL: OLIN C194 Cu	CONTRACT NO.	PROMEX 3075 Oakmead Village Drive Santa Clara, CA 95051	
FINISH:	DRAWN BOB CATANZARO 07/07	TITLE: QFN-12mm, 100LD PACKAGE OUTINE	
UNSPECIFIED TOLERANCE: DO NOT SCALE DRAWING. DIMENSIONS APPLY AFTER PLATING. DEC. ± 0.3 ± 0.05 ± 0.010 MM; ± 0.01 ± 0.002 ± 0.0008 INCH. ANGLES ± 2°. RADIUS = R0.05 MAX	CHECK BOB CATANZARO 07/07	SIZE: A	DWG NO.: 1212QFN100PO	REV: A
USED ON: GENERAL USE	DESIGN BOB CATANZARO 07/07	ORACLE CODE: 3FY32	FILE NAME: 1212QFN100_PO.dwg	SHEET: 1 or 1
NEXT ASSEMBLY	DESIGN ACTIVITY			
QTY	CUSTOMER			

Fig. 3. Package Drawing.

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to vcc plain that is power for the positive supply.

The part's identification label is ASNT1011A-PQA. The first 9 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
2.2.2	05-2020	Updated Package Information
2.1.1	09-2019	Updated Letterhead
2.0	06-2012	Revised Electrical Characteristics section. Corrected Terminal Functions. Revised Package Information section Added Absolute Maximums Rating table Added Pin Diagram
1.0	01-2011	First release