PCN Number:	20180319001	**PCN Date:**	March 22, 2018
Title:	Datasheet for LMX2595 and LMX2594		
Customer Contact:	PCN Manager	**Dept:**	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

LMX2595

SNAS736B – JUNE 2017 – REVISED MARCH 2018

Changes from Revision A (August 2017) to Revision B	Page
• Changed all the VCO Gain typical values in the *Electrical Characteristics* table. This is due to improved measurement methods and NOT a change in the device itself.	10
• Moved the high-level output voltage parameter V_{CC} – 0.4 value from the MAX column to the MIN	10
• Moved the high-level output current parameter 0.4 value from the MIN column to the MAX	10
• Changed data is clocked out on MUXout, not SDI pin	11
• Added comment that OSCin is clocked on rising edges of the signal. and reformatted with bulleted list	17
• Added description of the state machine clock	18
• Changed example from 200MHz/ 2^32 to 200 MHz/(2^32-1)	19
• Changed LD_DLY description in Table 4 and removed duplicated text in the *Lock Detect* section	19
• Changed name from VCO_AMPCAL to VCO_DACISET_STRT	21
• Added more programmable settings to Table 5	21
• Changed VCO Gain Table	22
• Added that OUTx_PWR states 32 to 47 are redundant and reworded section.	23
• Added term "IncludedDivide" for clarity	24
• Changed Fixed Diagram to show SEG0,SEG1,SEG2,and SEG3	25
• Changed included channel divide to IncludedDivide and 2 X SEG0 to 2 X SEG1. Also clarified IncludedDivide calculations	27
• Added more description on conditions for phase adust.	27
• Changed text from: (VCO_PHASE_SYNC=1) to: (VCO_PHASE_SYNC=0)	27
• Changed text so the user does not incorrectly assume that MASH_SEED varies from part ot part.	28
• Changed the RAMP_THRESH programming from: 0 to ± 2^{32} to: 0 to ± 2^{33} – 1	28
• Removed comment that RAMP_TRIG_CAL only applies in automatic ramping mode.	28
• Changed the RAMP_LOW and _HIGH programming from: 0 to ± 2^{31} to: 0 to ± 2^{33} – 1	28
• Changed description to be in terms of state machine cycles	29
• Changed RAMP_MODE to RAMP_MANUAL in the *Manual Pin Ramping* and *Automatic Ramping* sections	29

- Added that the RampCLK pin input is re-clocked to the phase detector frequency. ... 29
- Added that RampDir rising edges should be targeted away from rising edges of RampCLK pin. ... 29
- Changed programming enumerations for RAMP0_INC and RAMP1_INC ... 31
- Changed programming enumerations for RAMP_THRESH, RAMPx_LEN, and RAMP1_INC ... 32
- Changed Figure 30 ... 32
- Changed SysRef description ... 33
- Added divide by 2 to figure. ... 33
- Changed some entries in the table. ... 33
- Changed $f_{INTERPOLATOR}$ SYSREF setup equation in Table 19 ... 33
- Changed SysRef delay from: 224 and 225 to: 225 and 226 ... 34
- Changed "generator" mode to "master" mode. They mean the same thing. ... 34
- Changed description for SYSREF_DIV ... 34
- Changed Figure 32 ... 35
- Changed wording for repeater mode and master mode ... 36
- Changed description of a few of the steps. ... 37
- Changed typo in R17 and R19 ... 46
- Deleted reference to VCO_SEL_STRT_EN, this is always 1 ... 46
- Added VCO_SEL_STRT_EN reference. This is always 1. ... 46
- Changed the enumerations 0-3 and added content to the INPIN_LVL field description ... 48
- Added Divide by 1' to SYSREF_DIV_PRE register description. Also fixed mispelling its name ... 50
- Deleted redundant formula for Fout and also clarified SYSREF_DIV starts at 4 and counts by 2. ... 50
- Deleted reference to VCO_CAPCTRL_EN, which is always 1 and clarified. ... 52
- Changed text from: f_{MAX} to: f_{HIGH} ... 53
- Changed text from: RAMP_LIMIT_LOW=2^{32} - (f_{LOW} - f_{VCO}) / f_{PD} × 16777216 to: RAMP_LIMIT_LOW=2^{33} - 16777216 x (f_{VCO} - f_{LOW}) / f_{PD} ... 53
- Removed the *OSCin Configuration* table and added content to the *OSCin Configuration* section ... 57
- Changed pin 27 recommendation from 10 µF to 1 µF in Figure 52 ... 59

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The datasheet number will be changing.

Device Family	Change From:	Change To:
LMX2595	SNAS736A	SNAS736B
LMX2594	SNAS696A	SNAS696B

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/LMX2595

http://www.ti.com/product/LMX2594

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

LMX2595RHAR	LMX2595RHAT	LMX2594RHAR	LMX2594RHAT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
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Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com