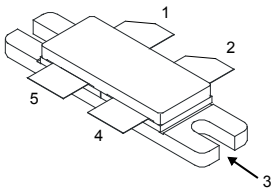
RF5L08350CB4

Datasheet

400 W, 50 V, 0.4 to 1 GHz RF power LDMOS transistor



B4E

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Product status link
RF5L08350CB4

Product summary	
Order code	RF5L08350CB4
Marking	5L08350
Package	B4E
Packing	Tape and reel 13"
Base/bulk quantity	120/120

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L08350CB4	860 MHz	50 V	400 W	19 dB	61%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European Directive 2002/95/EC

Applications

- Wideband lab amplifier from 0.4 to 1 GHz
- Digital UHF TV 470-860 MHz
- 650 MHz particle accelerator
- 915 MHz RF energy applications

Description

The RF5L08350CB4 is a 400 W, 50 V high-performance, internally matched LDMOS FET, designed for multiple applications over the frequency band 0.4 to 1 GHz.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	110	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC} (1)	Thermal resistance, junction-to-case	0.35	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	110	-		V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 50 V		-	1	µA
		V_{DS} = 0 V, V_{GS} = 90 V		-		
I_{GSS}	Gate-body leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_D = 600 µA	1	-	3	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS}= 1 V, I_D= 100 mA	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 5 A		-	1.4	V
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS}= 10 V, V_{DS}=100 mV		-	1	Ω
$I_{DS(on)}$	Static drain-source on-current			-	2.5	A

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		400		1000	MHz
P_{OUT}	Output power	f = 860 MHz at 1dB compression		400		W
G_{PS}	Power gain			19		dB
η_D	Drain efficiency			61		%
VSWR	Load mismatch	P_{OUT} = 400 W pulsed CW output power, all phases			10:1	

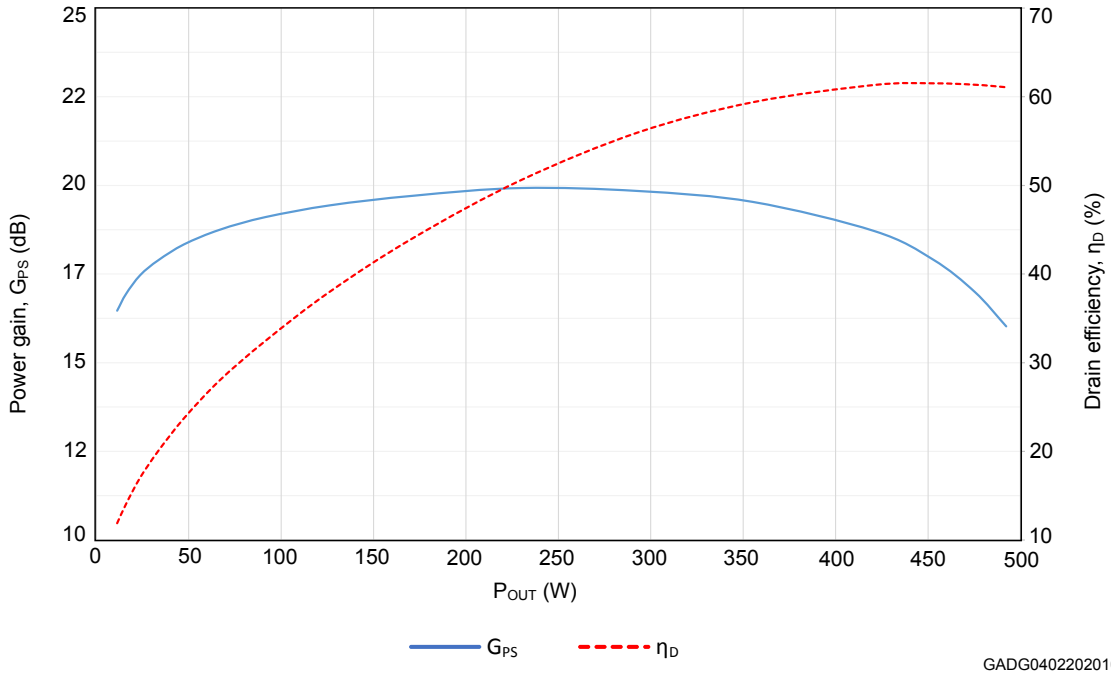
Note: V_{DD} = 50 V, I_{DQ} = 200 mA, pulsed CW, pulse width=100 µs, duty cycle=10%.

3 Typical performance

Table 6. Output power, power gain and drain efficiency vs input power (f = 860 MHz)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D(%)
24.1	40.5	11.3	1.9	16.5	11.9
25.1	42.1	16.1	2.3	16.9	14.1
26.3	43.8	23.8	2.8	17.5	17.0
27.4	45.3	33.6	3.4	17.9	20.0
28.4	46.8	47.5	4.0	18.3	23.7
29.5	48.3	66.9	4.8	18.8	28.0
30.5	49.6	91.6	5.6	19.1	32.5
31.6	51.0	126.6	6.7	19.4	38.0
32.6	52.4	172.0	7.8	19.7	44.1
33.7	53.6	230.2	9.1	19.9	50.6
34.8	54.7	293.5	10.5	19.8	56.0
36.0	55.5	355.3	12.0	19.5	59.4
37.5	56.3	421.1	13.7	18.7	61.3
38.7	56.6	452.8	14.7	17.9	61.5
39.8	56.8	475.4	15.5	17.0	61.4
40.9	56.9	492.3	16.1	16.0	61.1

Figure 1. Power gain and efficiency vs output power (f = 860 MHz)



Note: V_{DD} = 50 V, I_{DQ} = 200 mA, pulsed CW, pulse width = 100 µs, duty cycle = 10%

4 Test circuits

Figure 2. **Test circuit layout (f = 860 MHz)**

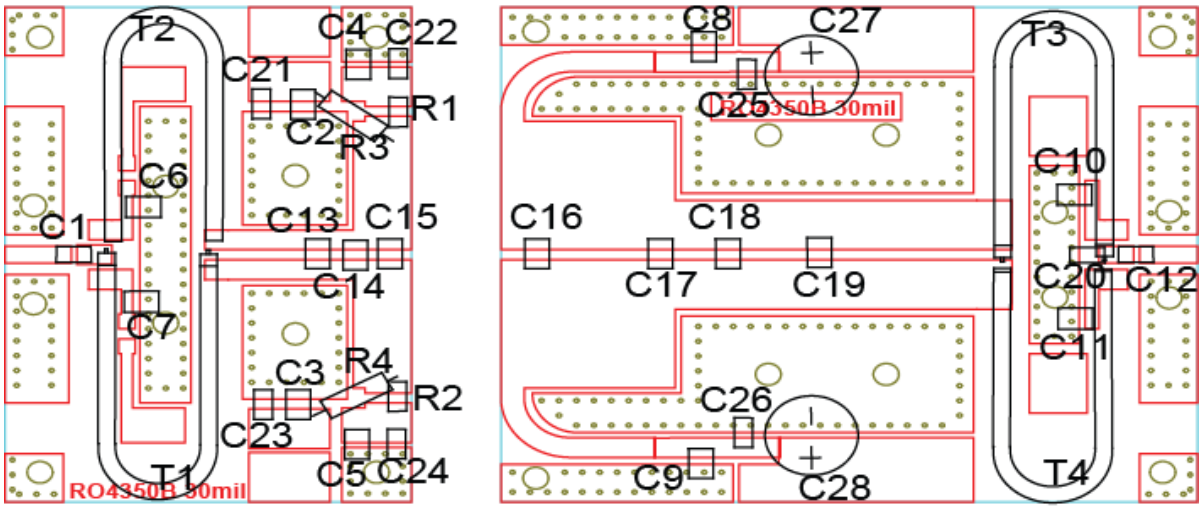


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Figure 3. **Test circuit photo (f = 860 MHz)**

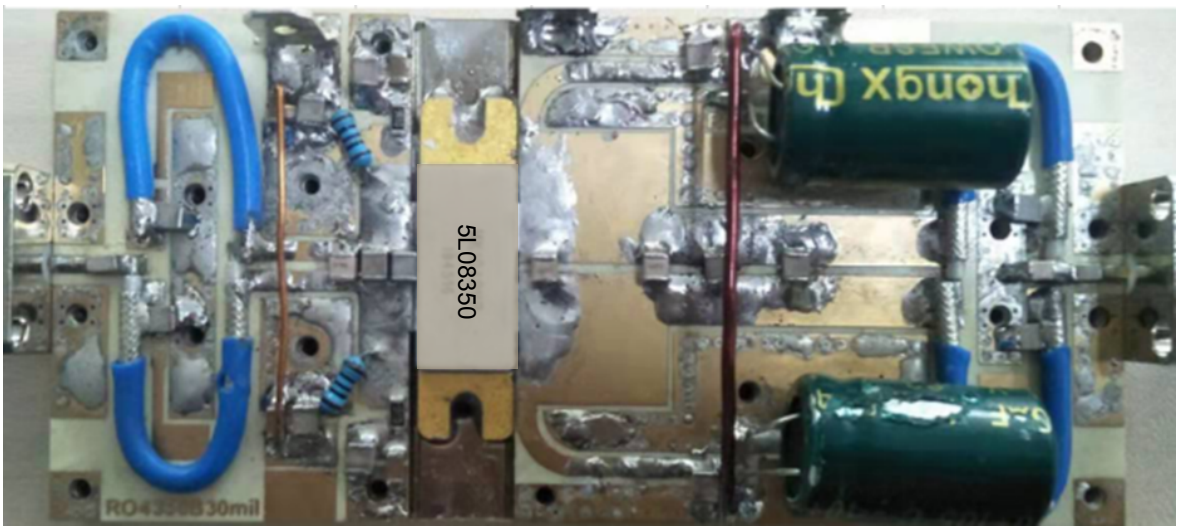

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Table 7. **Component list (f = 860 MHz)**

Component	Description	Reference
C1, C12	47 pF	ATC800B
C13	1.5 pF	DLC70B
C14, C19	6.8 pF	ATC800B
C15	10 pF	ATC800B
C16, C17, C20	2.2 pF	DLC70B
C18	4.7 pF	ATC800B
C21, C26	10 µF, 100 V	
C27, C28	470 µF, 63 V	
R1, R2	9.1 Ω	1206
R3, R4	100 Ω, 1 W	
T1, T2, T3, T4	25 Ω, 50 mm	SF-086-25

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 B4E package information

Figure 4. B4E package outline

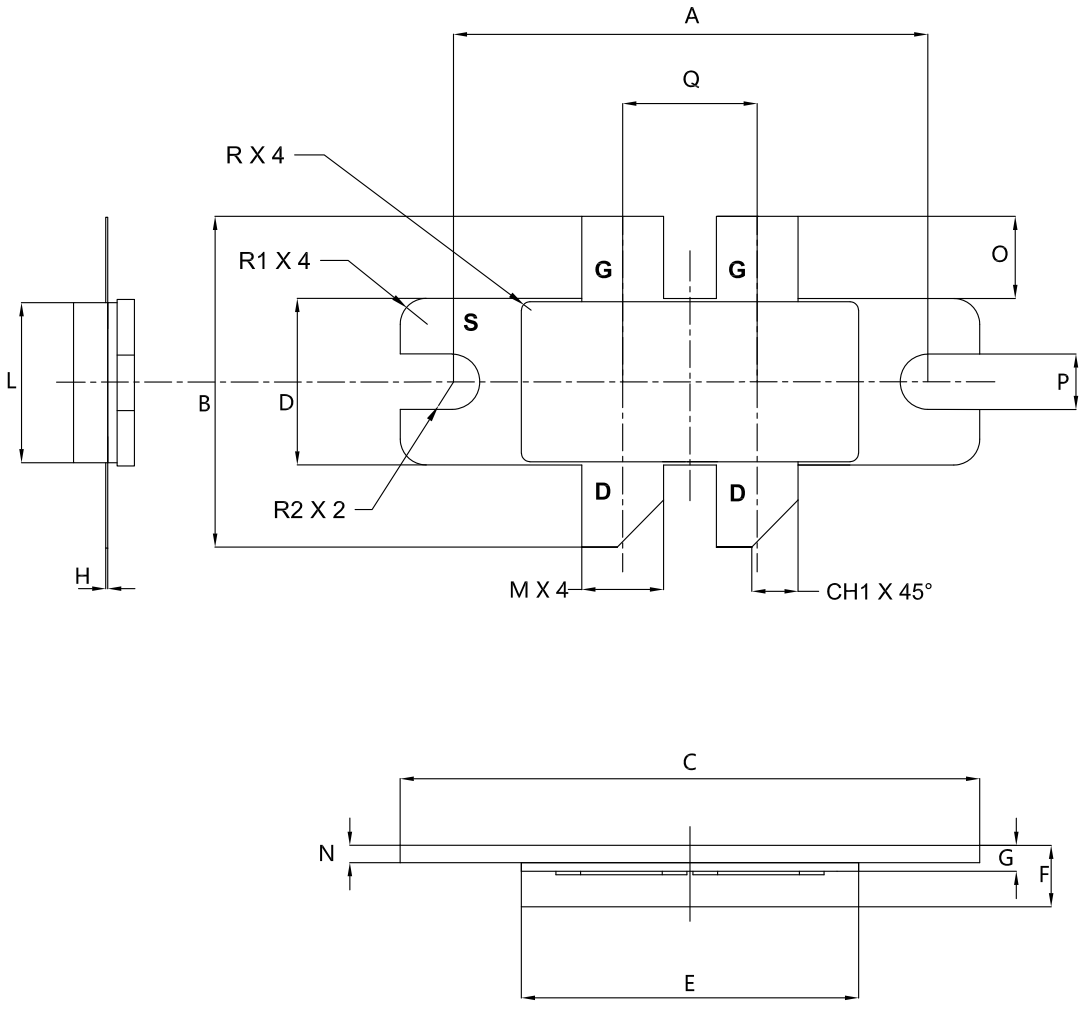

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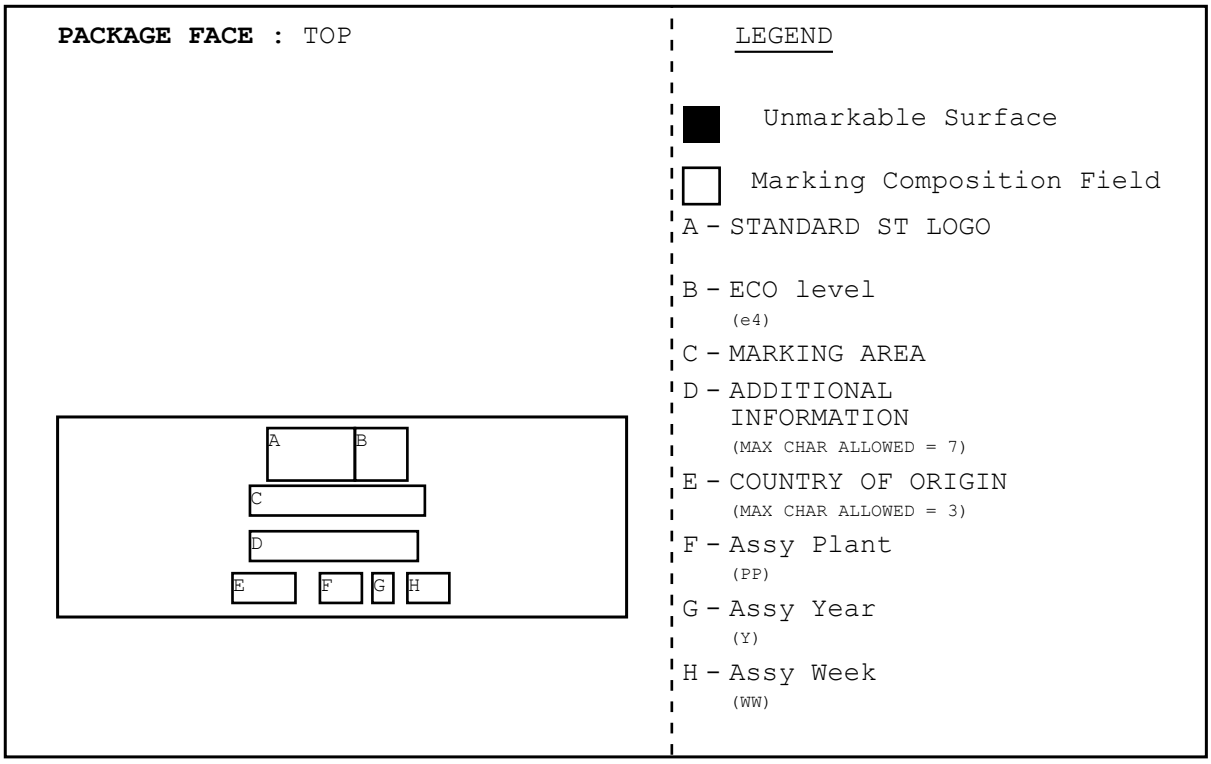
Table 8. **B4E package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	27.81	27.94	28.07
B	18.93	19.43	19.93
C	33.91	34.04	34.17
D	9.65	9.78	9.91
E	19.56	19.81	20.06
F	3.23	3.61	3.99
G	1.40	1.53	1.66
H	0.07		0.15
L	9.20	9.40	9.60
M	4.67	4.80	4.93
N	0.89	1.02	1.15
O	4.70	4.83	4.96
P	3.13	3.26	3.39
Q	7.77	7.90	8.03
R		0.50	
R1		1.52	
R2		1.63	
CH1		2.72	

5.2 Marking information

Figure 5. **Marking composition**



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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
25-May-2020	1	First release.
28-Sep-2021	2	Modified features and marking on cover page Modified Table 1. Absolute maximum ratings (T_C = 25 °C), Table 3. ESD protection, Table 4. Static (per side), Table 5. Dynamic, Figure 1. Power gain and efficiency vs output power (f = 860 MHz) and Figure 3. Test circuit photo (f = 860 MHz). Added Section 5.2 Marking information. Minor text changes.

Contents