zilog®

Z16F2800100ZCOG

ZNEO® Z16F Series Development Kit

User Manual

UM020205-0908

z i l o g

Warning: DO NOT USE IN LIFE SUPPORT

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Document Disclaimer

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
September 2008	05	Updated Introduction section.	1
September 2007	04	Updated Title, Schematics. Implemented Zilog Style Guide.	All
June 2006	03	Added note on the ZNEO development board 16-bit bus and programming external Flash memory.	5
May 2006	02	Updated all schematics.	12
Jan. 2006	01	Original Issue	All

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Introduction

Zilog's ZNEO® Z16F Series MCU is part of its microcontroller products. The ZNEO Z16F Series MCU Development Kit (Z16F2800100ZCOG) familiarizes with the hardware and software tools available with this product. This kit consists of the 128 KB version of the ZNEO development board that supports and presents the features of the ZNEO Z16F Series. This kit allows you to write application software and contains all supporting documents.

This User Manual acquaints you with the ZNEO Z16F Series MCU Development Kit, and provides instructions on setting up and using the tools to start building designs and applications.

Z16F2811AL20SG is the silicon used in the board. For more details, refer to *ZNEO Z16F Series Product Specification (PS0220)* available for download at www.zilog.com.

Safeguards

The following precaution must be observed when working with the devices described in this document.

⚠ **Caution:** *Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).*

Installation

For information on software installation and setup of the ZNEO Z16F Series development kit, refer to *ZNEO® Series of Microcontrollers Development Kit Quick Start Guide (QS0057).*

ZNEO Z16F Series Development Board

Introduction

The ZNEO Z16F Series development board is a development and proto-typing board for the ZNEO Z16F Series MCU. The board allows you to evaluate the features of ZNEO Z16F Series MCU, and to develop an application before building the hardware.
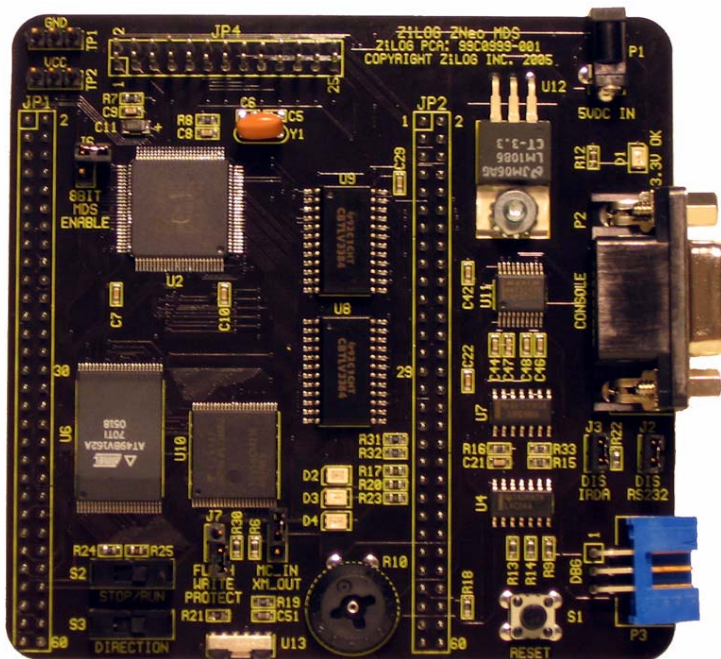
Figure 1. ZNEO Z16F Series Development Board

Features

The features of ZNEO Z16F Series of Microcontrollers include:

- ZNEO MCU (100-Lead LQFP package)

- 1 M x 16 External Flash memory

- 256 K x 16 External RAM

- 3 LEDs

- RS-232 interface

- On-Chip Debugger interface

- IrDA transceiver

- Electrical and mechanical compatibility with Zilog Modular Development System (MDS) architecture

- One RESET pushbutton (S1)

- Two SPST switches (S2-STOP/RUN and S3-DIRECTION)

- 5 V DC power connector

- 20 MHz Ceramic Oscillator (Y1)

- Header for Analog-to-Digital Converter (ADC) input

- External interface connectors JP1, JP2, and JP4

- 2.7 V to 3.6 V operating voltage with 5 V tolerant inputs

Development Kit Block Diagram

Figure 2 displays the block diagram of ZNEO Z16F Series development kit.
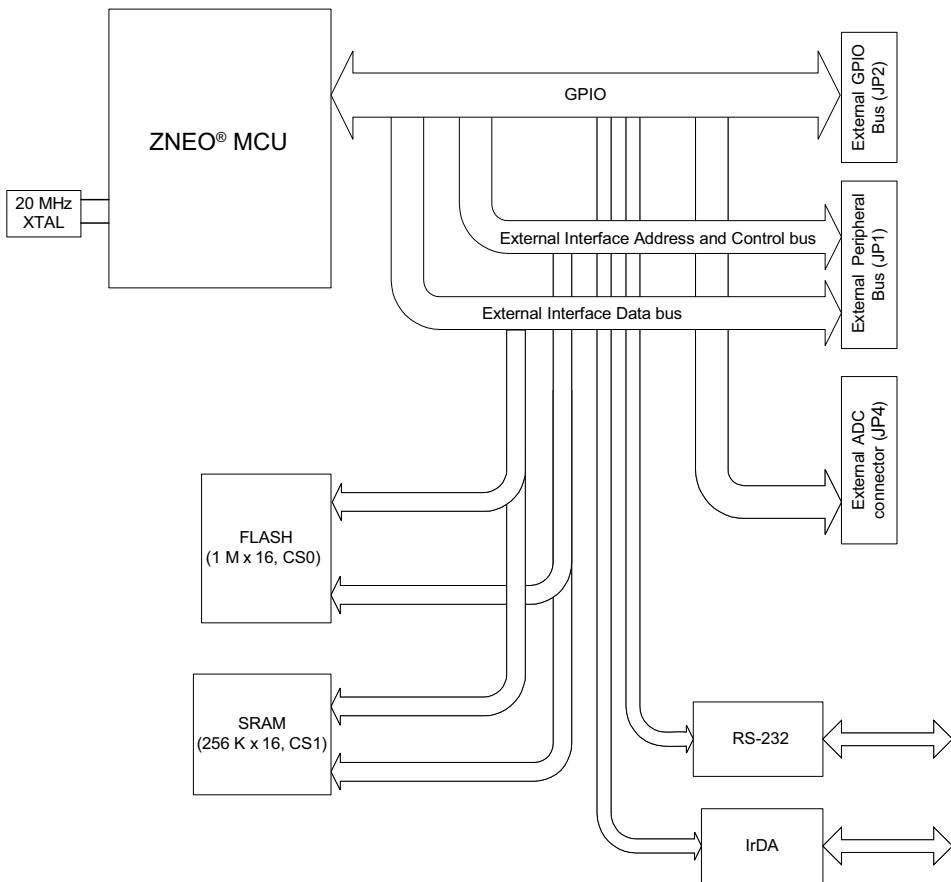

Figure 2. ZNEO Z16F Series Development Kit Block Diagram

ZNEO MEMORY LAYOUT

The ZNEO CPU has a unique memory architecture with a unified 24-bit physical address space, which is partitioned into several distinct memory areas. In terms of physical memory spaces, the overall address space includes the following:

- Internal non-volatile memory

- Internal RAM

- Internal I/O memory and special function registers (SFRs)

- External memory and memory mapped peripherals

The internal memory listed above are always present in ZNEO devices, while the external memory is optional. Every address space is defined as a specific range of addresses located at a given place in the framework of the unified 24-bit address space, and the address ranges of the different spaces do not overlap. To promote code efficiency, the ZNEO CPU supports shorter 16-bit addressing for the memory located in the address ranges `00_0000H-00_7FFFH` and `FF_8000H-FF_FFFFH`. Table 1 on page 6 displays the physical layout of memory spaces available in the ZNEO architecture.

> **Note:** *The external Flash memory on the ZNEO development board has a 16-bit bus. All Write operation to Flash Memory must be 16 bits at even addresses only. Attempts to Write 1 byte will result in the byte being replicated on both the upper and lower bytes of the 16-bit bus.*

Table 1. ZNEO Physical Memory Layout

Memory	Address	Chip Selects
Internal I/O Memory & SFRs	FF_FFFFH–FF_E000H	
External Memory Mapped Peripherals (optional)	FF_DFFFH–FF_C800H	CS3 – CS5
External Memory at CS2 (optional)	FF_C7FFH–FF_C000H	CS2
Internal RAM	FF_BFFFH–FF_8000H	
External Memory at CS2 (optional)	F0_0000H	CS2
External Memory at CS1 (optional)	80_0000H	CS1
External Memory at CS0 (optional)	02_0000H	CS0
Internal Non-Volatile Memory	01_FFFFH–00_0000H	

Each internal memory space has a distinct purpose. Internal non-volatile memory contains executable program code and constant data. ZNEO CPU based devices have internal non-volatile memory starting at address 00_0000H. For example, a device equipped with 128 K of Flash has internal non-volatile memory starting at address 00_0000H and ending at address 01_FFFFH.

Internal RAM contains non-constant data and the stack. Executable program code can also reside in internal RAM, if desired. ZNEO CPU based devices have internal RAM ending at address FF_BFFFH, while the beginning address (and hence the total extent of this space) is device dependent. For example, a device equipped with 4 K of RAM has internal RAM starting at address FF_B000H and ending at address FF_BFFFH. Since internal RAM is accessed using 16-bit addressing, the lowest possible starting address for internal RAM on any device is FF_8000H.

ZNEO CPU based devices support 8 K of internal I/O memory located at addresses FF_E000H–FF_FFFFH. This memory contains CPU control registers and other SFRs, on-chip peripherals, and memory-mapped I/O ports.

ZNEO CPU based devices also provide an external interface that allows seamless connection to external memory and/or peripherals. External memory can be non-volatile memory such as Flash, or RAM, or both. External non-volatile memory is used to store program code or constant data, while external RAM is available primarily for non-constant data.

The external interface supports multiple chip select signals (CSx), which are asserted by the CPU when an access to external memory is requested. These signals are used to access distinct ranges and devices in external memory. The boundaries between memory ranges selected by the chip select signals are at fixed addresses, and, in some cases, the ranges covered by chip selects might overlap. For example, there might be some addresses in the range of both the CS0 and CS1 signals. In this case, the ZNEO CPU uses a chip select priority scheme. It asserts only a single chip select with the highest priority among those that contain the addresses to be accessed, with CS0 having the lowest priority and CS5 the highest. Also, the chip selects can be individually enabled or disabled. On-chip memory has greater priority over external memory. CS0 starts at address `00_0000H`, and CS1 starts at address `80_0000H`. CS2 to CS5 start at addresses `F0_0000H` and beyond. For more information, refer to *ZNEO® CPU Core User Manual (UM0188)* and the individual device product specification.

MCU

The ZNEO Z16F Series Flash microcontrollers are based on Zilog's advanced ZNEO 16-bit CPU core. The ZNEO Z16F Series MCU family of devices sets a new standard of performance and efficiency with a 24-bit address bus and 16-bit data bus.

The ZNEO Z16F Series External Interface allows seamless connection to external memory and peripherals. A 24-bit address bus and selectable 8-bit or 16-bit data bus allows parallel access up to 16 MB.

The Development board contains circuitry to support and present all the features of the ZNEO Z16F Series. The key features of ZNEO Z16F Series include:

- 20 MHz ZNEO CPU Core

- Up to 128 KB internal Flash program memory with 16-bit access and in-circuit programming capability

- Up to 4 KB internal RAM with 16-bit access

- External Interface allows seamless connection to external data memory and peripherals with:
  - 6 chip selects with Programmable Wait states
  - 24-bit address bus supports up to 16 MB
  - Selectable 8-bit or 16-bit data bus widths
  - Programmable Chip Select signal polarity
  - ISA-compatible mode

- Up to 12 channels 10-bit ADC

- Operational Amplifier

- Analog Comparator

- 4-channel DMA controller supports internal or external DMA requests

- Two full-duplex 9-bit Universal Asynchronous Receiver/Transmitter (UARTs) with support for Local Interconnect Network (LIN) and Infrared Data Association (IrDA)

- Internal Precision Oscillator (IPO)

- I^2C Master-Slave controller

- Enhanced Serial Peripheral Interface (ESPI) controller

- 12-bit Pulse Width Modulator (PWM) module with three complementary pairs or six independent PWM outputs with dead-band generation and fault trip input

- Three standard 16-bit timers with capture, compare, and PWM capability

- Watchdog Timer (WDT) with internal RC oscillator

- Up to 76 I/O pins

- Up to 24 interrupts with programmable priority

- Single-pin on-chip debugger

- Power-on Reset (POR)

- Voltage Brownout Protection (VBO)

- 2.7 V to 3.6 V operating voltage with 5 V tolerant inputs

- 0 °C to +70 °C standard temperature, -40 °C to +105 °C extended temperature, and -40 °C to +125 °C automotive operating ranges

For more information, refer to *ZNEO® Z16F Series Product Specification (PS0220)* available for download at www.zilog.com.

UART with IrDA ENDEC

The ZNEO Z16F Series contains a fully-functional, high-performance UART with Infrared Encoder/Decoder (ENDEC). The Infrared ENDEC is integrated with an on-chip UART (component U13) allowing easy communication between the ZNEO Z16F Series and IrDA transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers, and other infrared enabled devices.

Switches and LEDs

The ZNEO development board contains the following LEDs and switches:

- Green LED D1, which when illuminated indicates the presence of 3.3 V DC on the board's VCC_3 V power bus

- Red LED D2, connected to chip port PA0_T0IN

- Yellow LED D3, connected to the chip port PA1_T0OUT

- Green LED D4, connected to the chip port PA2_DE0

- RESET switch S1, connected to the chip port $\overline{\text{RESET}}$

- SPST switch S2, connected to the chip port PA7_SDA

- SPST switch S3, connected to the chip port PC0_T1IN

Potentiometer R10 is reserved for future use.

Jumper Settings

Table 2 provides information on the shunt status, functions, and default settings of jumpers on the ZNEO Z16F Series development board.

Table 2. ZNEO Jumper Settings

Jumper	Status	Function	Default
J1	OUT (not installed)	Enables ZNEO MCU access to external 16-bit memory bus on development board.	X
J1	IN	Disables 16-bit external memory bus and makes ZNEO MCU analog ports available through connector JP4. Refer to schematic for JP4 pinouts.	
J2*	OUT	RS-232 interface enabled.	X
J2	IN	RS-232 interface disabled.	
J3*	OUT	IrDA interface enabled.	

Table 2. ZNEO Jumper Settings (Continued)

Jumper	Status	Function	Default
J3	IN	IrDA interface disabled.	X
J6	OUT	8-bit MDS interface disabled.	X
J6	IN	8-bit MDS interface enabled.	
J7	OUT	External Flash Write Protect disabled.	X
J7	IN	External Flash Write Protect enabled.	
Note: * These jumpers must not be OUT at the same time.			

External Interface Headers JP1, JP2, and JP4

External interface headers JP1, JP2, and JP4 are provided in Schematics on page 12.

Schematics

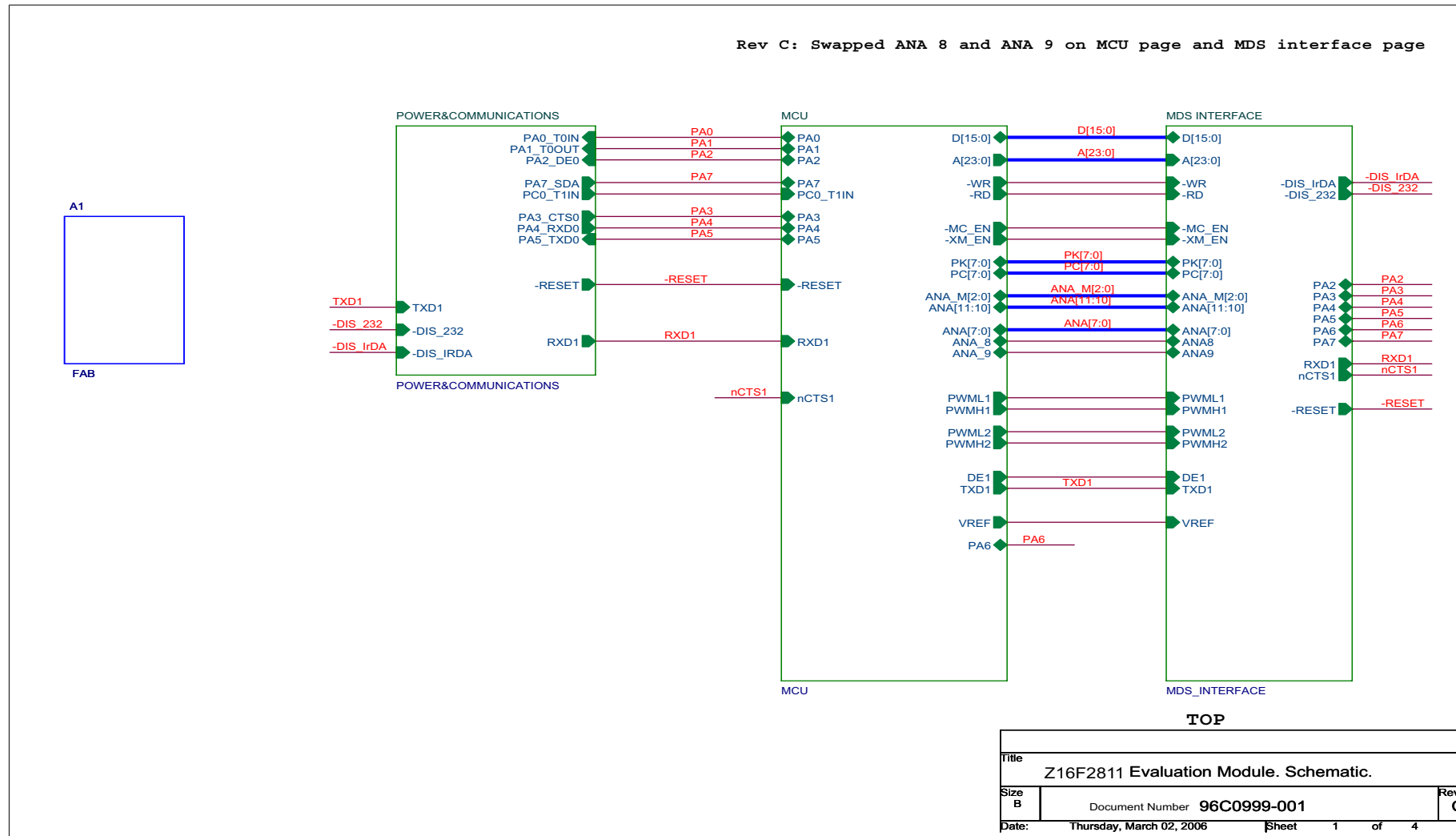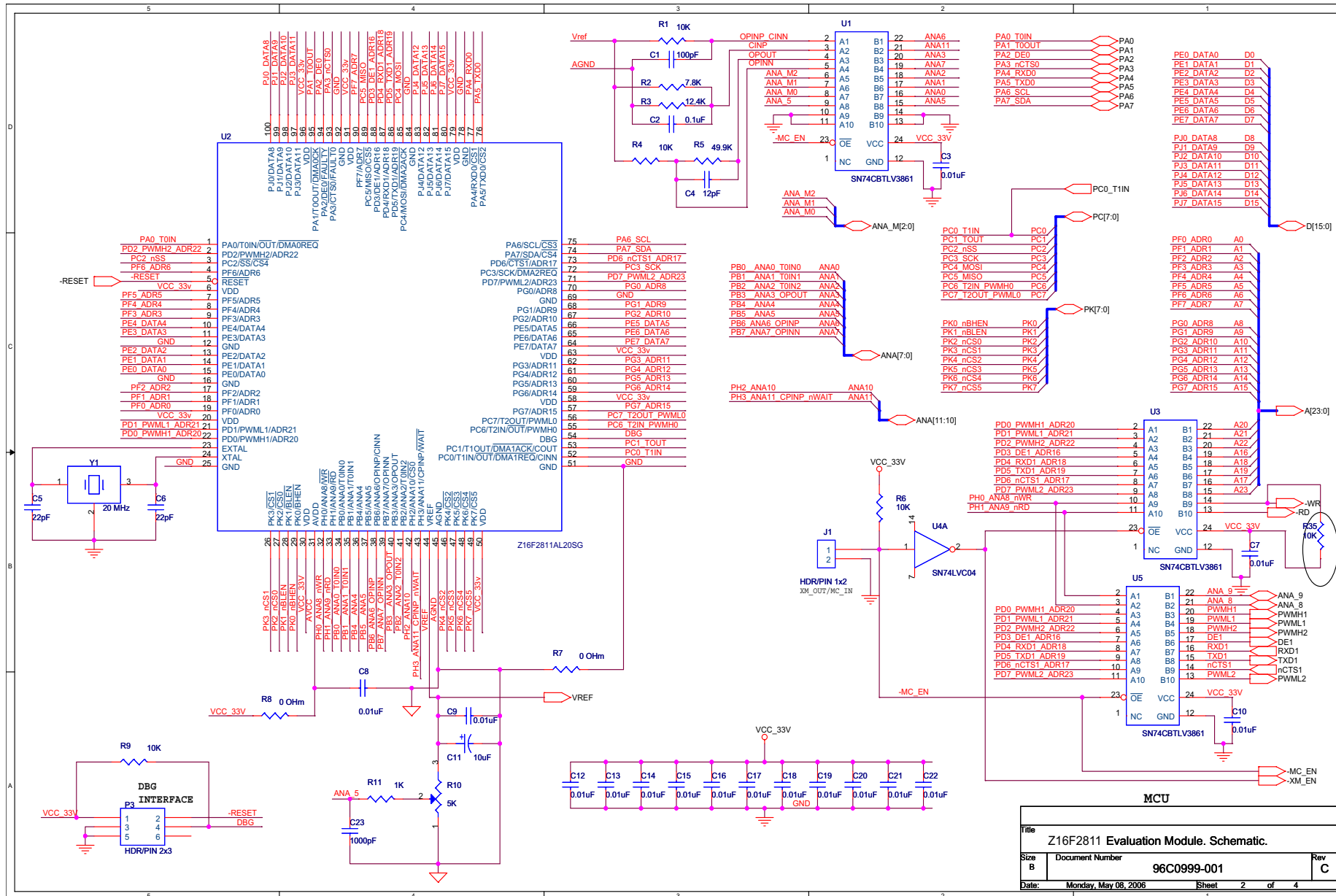Figure 3 through Figure 6 on page 15 display the schematics for the ZNEO Z16F Series Development Kit.

Figure 3. ZNEO Z16F Series MCU Development Kit

Figure 4. ZNEO Z16F Series MCU Development Kit

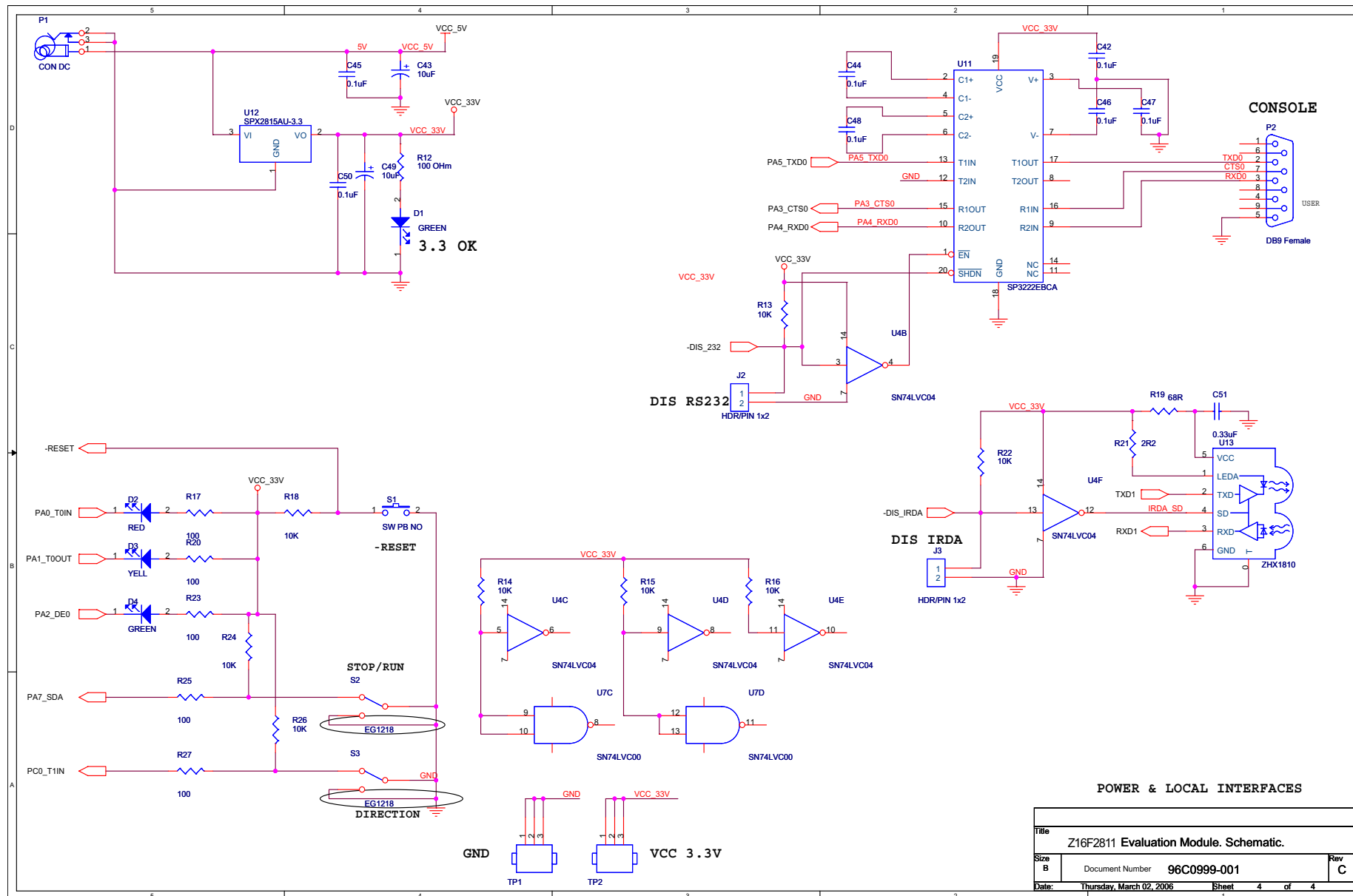Figure 5. ZNEO Z16F Series MCU Development Kit

Figure 6. ZNEO Z16F Series MCU Development Kit

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.