

IS32FL3726A

16-CHANNEL LED DRIVER

June 2021

GENERAL DESCRIPTION

The IS32FL3726A is a serial shift-register-plus latch-type LED driver operating from a 3V to 5V supply. It is comprised of 16 constant-current open drain sinks designed for driving common anode LEDs. The output current value can be set from 5mA to 60mA by using an external resistor. As a result, all outputs will have virtually the same current levels. This driver uses a high-speed 4-wire serial interface of up to 30MHz to drive 16 constant current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit. Serial input data appears at the output OUT_n channels after 16 clock cycles. Driving the Latch pin will load the 16-bit of shift-register data into the 16-bit output latch to drive the LEDs ON or OFF. The Enable pin can be used as a PWM input to adjust the LED brightness. The IS32FL3726A operates from a 3V to 5.5V supply, and is specified over the -40°C to $+125^{\circ}\text{C}$ temperature range.

APPLICATIONS

- Car display panel
- Ambient lighting
- Roof lighting
- Functional lighting

FEATURES

- Output current capability and number of outputs: 60mA \times 16 outputs
- Current set with external resistor
- Constant current range: 5mA to 60mA
 $I_{OUT_MAX} = 45\text{mA}$ @ $V_{CC} = 3.3\text{V}$
 $I_{OUT_MAX} = 60\text{mA}$ @ $V_{CC} = 5\text{V}$
- Current accuracy (All output on, $I_{OUT} = 25.2\text{mA}$)
 - Bit to bit: $< \pm 5\%$.
 - Device to device: $< \pm 5\%$.
- 200mV LED Dropout at 25mA
- For common-anode LEDs
- Power supply voltage range, $V_{CC} = 3.0\text{V}$ to 5.5V
- Serial and parallel data transfer rate: 30MHz (Max. cascade connection)
- Operating temperature range, -40°C ~ $+125^{\circ}\text{C}$
- Package: eTSSOP-24
- AEC-Q100 Qualified

TYPICAL APPLICATION CIRCUIT

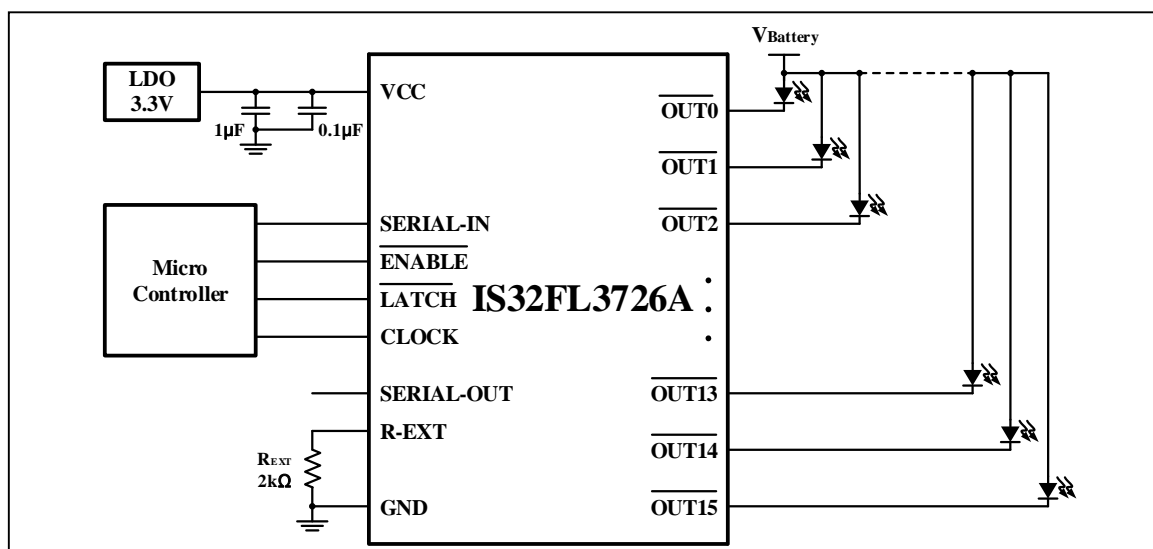


Figure 1 Typical Application Circuit

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TYPICAL APPLICATION CIRCUIT (CONTINUE)

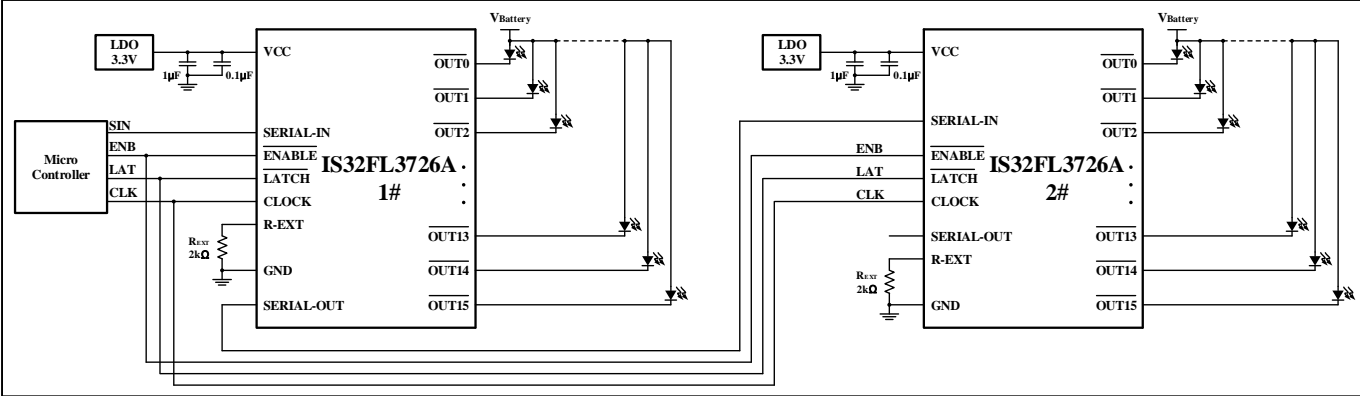
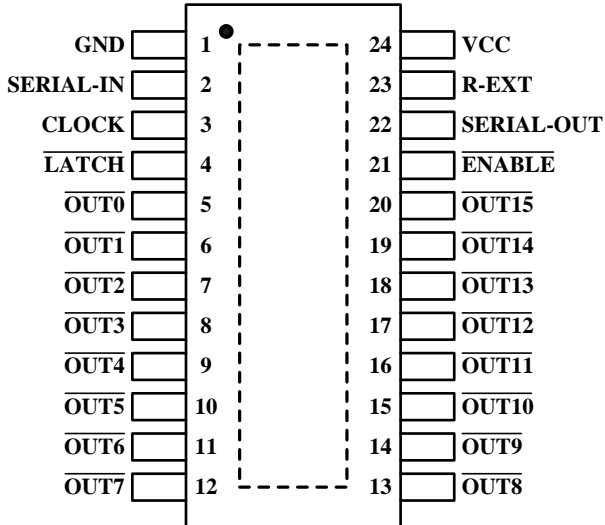


Figure 2 Typical Application Circuit (Serial Synchronization)

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PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-24	 <p>Diagram showing the pin configuration for the eTSSOP-24 package. The package is shown as a 24-pin component with pins numbered 1 to 24. The functions for each pin are listed as follows:</p> <ul style="list-style-type: none"> Pin 1: GND Pin 2: SERIAL-IN Pin 3: CLOCK Pin 4: $\overline{\text{LATCH}}$ Pin 5: $\overline{\text{OUT0}}$ Pin 6: $\overline{\text{OUT1}}$ Pin 7: $\overline{\text{OUT2}}$ Pin 8: $\overline{\text{OUT3}}$ Pin 9: $\overline{\text{OUT4}}$ Pin 10: $\overline{\text{OUT5}}$ Pin 11: $\overline{\text{OUT6}}$ Pin 12: $\overline{\text{OUT7}}$ Pin 13: $\overline{\text{OUT8}}$ Pin 14: $\overline{\text{OUT9}}$ Pin 15: $\overline{\text{OUT10}}$ Pin 16: $\overline{\text{OUT11}}$ Pin 17: $\overline{\text{OUT12}}$ Pin 18: $\overline{\text{OUT13}}$ Pin 19: $\overline{\text{OUT14}}$ Pin 20: $\overline{\text{OUT15}}$ Pin 21: $\overline{\text{ENABLE}}$ Pin 22: SERIAL-OUT Pin 23: R-EXT Pin 24: VCC

PIN DESCRIPTION

No.	Pin	Description
1	GND	GND pin for control logic.
2	SERIAL-IN	Input pin for serial data for data shift register.
3	CLOCK	Input pin for clock for data shift on rising edge.
4	$\overline{\text{LATCH}}$	Input pin for data strobe when the $\overline{\text{LATCH}}$ input is driven low, data is not latched. When it is pulled high, data is latched.
5~20	$\overline{\text{OUT0}}\sim\overline{\text{OUT15}}$	Constant-current sinks.
21	$\overline{\text{ENABLE}}$	Input pin for output enable. All current sinks ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ pin is driven High and are turned on, when this pin is driven Low.
22	SERIAL-OUT	Output pin for serial data input on SERIAL-IN terminal.
23	R-EXT	Input pin connect to an external resistor to regulate the output current.
24	VCC	Supply voltage pin.
	Thermal Pad	Connect to GND.

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ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3726A-ZLA3-TR	eTSSOP-24, Lead-free	2500

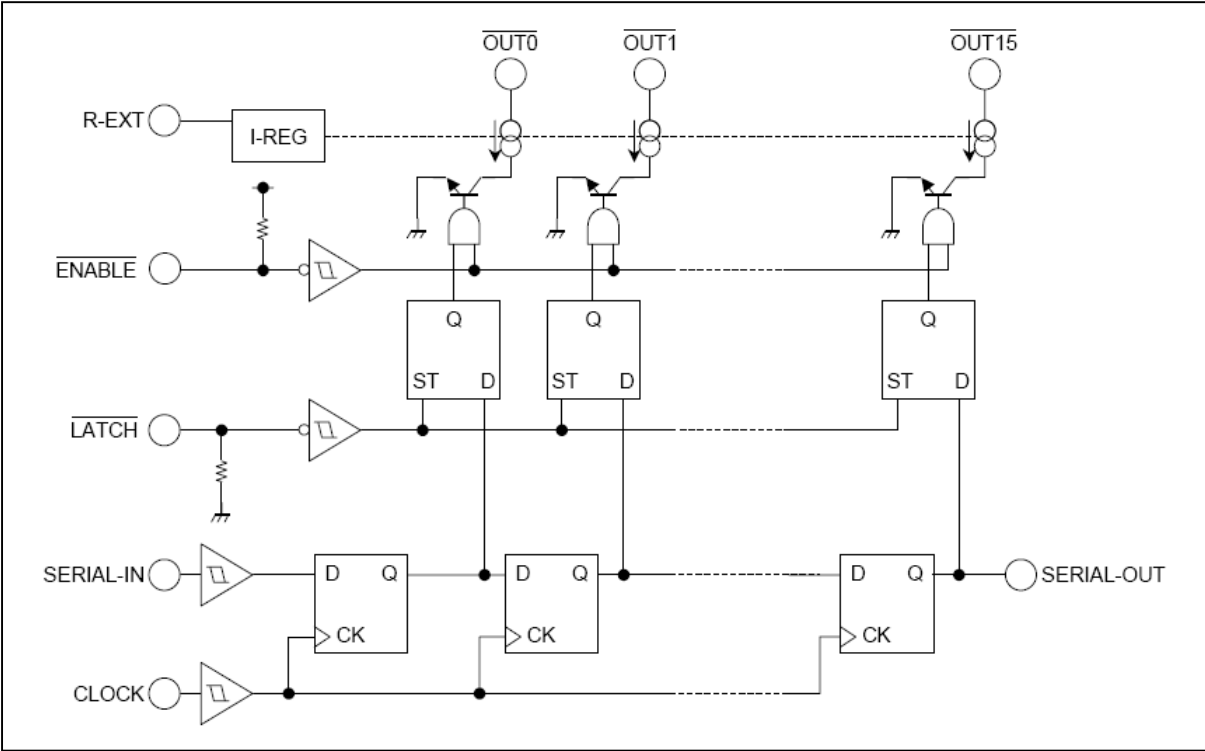
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FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.2V$
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A=T_J$	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	28.1°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JEDEC standard), θ_{JP}	8.55°C/W
Maximum power dissipation, P_{DMAX}	3.56W
ESD (HBM)	±2kV
ESD (CDM)	±750V

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

$V_{CC}= 5V$, $T_A= T_J= -40^\circ C \sim +125^\circ C$, unless otherwise noted.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
V_{OUT}	Output (headroom) voltage			0.7	5	V
f_{CLK}	Clock frequency	Cascade connected			30	MHz
t_{WLAT}	LATCH pulse width (Note 2)		20			ns
t_{WCLK}	CLOCK pulse width (Note 2)		20			ns
t_{WENA}	ENABLE pulse width (Note 2, 3)		70			ns
t_{SETUP1}	SERIAL-IN set-up time for CLOCK pin (Note 2)		8			ns
t_{HOLD1}	SERIAL-IN Hold time for CLOCK pin (Note 2)		8			ns
t_{SETUP2}	Set-up time for LATCH pin (Note 2)		8			ns
t_{HOLD2}	Hold time for LATCH pin (Note 2)		8			ns

Note 2: Guaranteed by design.

Note 3: When the pulse of the Low level is input to the ENABLE pin held in the High level.

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ELECTRICAL CHARACTERISTICS

$V_{CC}=5V$, $T_A=T_J=-40^{\circ}C \sim +125^{\circ}C$, unless otherwise noted.

Symbol	Characteristic	Condition		Min.	Typ.	Max.	Unit	
V_{CC}	Supply voltage	Normal operation		3.0		5.5	V	
I_{OUT}		$V_{OUT}=1V, V_{CC}=3.3V$	$R_{EXT}=750\Omega$	23.4	25.2	27	mA	
		$V_{OUT}=1V, V_{CC}=5V$	$R_{EXT}=750\Omega$	23.4	25.2	27		
ΔI_{MAT}	Output current error between bits (Note 5)	$V_{OUT}=1V$ $V_{CC}=3.3V$	$R_{EXT}=750\Omega$ $I_{OUT}=25.2mA$	-5		5	%	
		$V_{OUT}=1V$ $V_{CC}=5V$	$R_{EXT}=750\Omega$ $I_{OUT}=25.2mA$	-5		5	%	
ΔI_{OUT}	Output current error between ICs (Note 6)	$V_{OUT}=1V$ $V_{CC}=3.3V$	$R_{EXT}=750\Omega$ $I_{OUT}=25.2mA$	-5		5	%	
		$V_{OUT}=1V$ $V_{CC}=5V$	$R_{EXT}=750\Omega$ $I_{OUT}=25.2mA$	-5		5	%	
V_{HR}	Headroom voltage	$R_{EXT}=750\Omega, I_{OUT}=25.2mA$			0.4	0.55	V	
I_{OZ}	Output leakage current input voltage	$V_{OUT}=5.5V$				1	μA	
V_{IH}	Input voltage	Logic high level		$0.7V_{CC}$			V	
V_{IL}		Logic low level				$0.3V_{CC}$		
V_{OL}	SERIAL-OUT pin voltage	$I_{OL}=1.0mA, V_{CC}=3.3V$				0.4	V	
		$I_{OL}=1.0mA, V_{CC}=5V$				0.4		
V_{OH}		$I_{OH}=-1.0mA, V_{CC}=3.3V$			2.9			
		$I_{OH}=-1.0mA, V_{CC}=5V$			4.6			
$\%V_{CC}$	Output current supply voltage regulation	When V_{CC} is changed 3.3V to 5.5V, $I_{OUT}=25.2mA$				1.5	%	
$R_{(UP)}$	Pull-up resistor	ENABLE pin		250	500	750	k Ω	
$R_{(DOWN)}$	Pull-down resistor	LATCH pin						
$I_{DD(OFF)1}$	Supply current	$V_{OUT}=5V$	$R_{EXT}=OPEN$		0.3	0.6	mA	
$I_{DD(OFF)2}$		$V_{OUT}=5V$ All outputs off	$R_{EXT}=0.75k\Omega$		2.1	2.5		
			$R_{EXT}=1.8k\Omega$		1	1.2		
$I_{DD(ON)1}$		$V_{OUT}=0.7V$ All outputs on	$R_{EXT}=0.75k\Omega$		8.6	10		
		$R_{EXT}=1.8k\Omega$		4.5	6			

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SWITCHING CHARACTERISTICS (NOTE 4)

$V_{CC}=5V$, $T_A=T_J=-40^{\circ}C \sim +125^{\circ}C$, unless otherwise noted.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{pLH1}	Propagation delay	CLOCK - $\overline{OUT_n}$, $\overline{LATCH} = "H"$ $\overline{ENABLE} = "L"$		30	50	ns
t_{pLH2}		LATCH - $\overline{OUT_n}$, $\overline{ENABLE} =$		30	50	
t_{pLH3}		$\overline{ENABLE} - \overline{OUT_n}$, $\overline{LATCH} =$		50	70	
t_{pLH}		CLOCK - SERIAL-OUT		20	40	
t_{pHL1}		CLOCK - $\overline{OUT_n}$, $\overline{LATCH} = "H"$ $\overline{ENABLE} = "L"$		60	100	
t_{pHL2}		LATCH - $\overline{OUT_n}$, $\overline{ENABLE} =$		60	100	
t_{pHL3}		$\overline{ENABLE} - \overline{OUT_n}$, $\overline{LATCH} =$		70	100	
t_{pHL}		CLOCK - SERIAL-OUT		20	40	
t_{or}	Output rise time	10%~90% of voltage waveform		30	50	ns
t_{of}	Output fall time	90%~10% of voltage waveform		52	80	ns
t_r	Maximum CLOCK rise time	When not on PCB (Note 7)			500	ns
t_f	Maximum CLOCK fall time				500	ns

Conditions: (Refer to test circuit.)

$T_A=T_J=-40^{\circ}C \sim +125^{\circ}C$, $V_{CC}=V_{IH}=3.3V$ and $5V$, $V_{IL}=0V$, $R_{EXT}=750\Omega$, $V_L=3.0V$, $R_L=60\Omega$, $C_L=10.5pF$

Note 4: Guaranteed by design.

Note 5: I_{OUT} mismatch (bit to bit) ΔI_{MAT} is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn} (n = 0 \sim 15)}{\left(\frac{I_{OUT0} + I_{OUT1} + \dots + I_{OUT15}}{16} \right)} - 1 \right) \times 100\%$$

Note 6: I_{OUT} accuracy (device to device) ΔI_{OUT} is calculated:

$$\Delta I_{OUT} = \left(\frac{\left(\frac{I_{OUT0} + I_{OUT1} + \dots + I_{OUT15}}{16} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)} = 10.5mA$ when $R_{EXT} = 1800\Omega$, $I_{OUT(IDEAL)} = 25.2mA$ when $R_{EXT} = 750\Omega$.

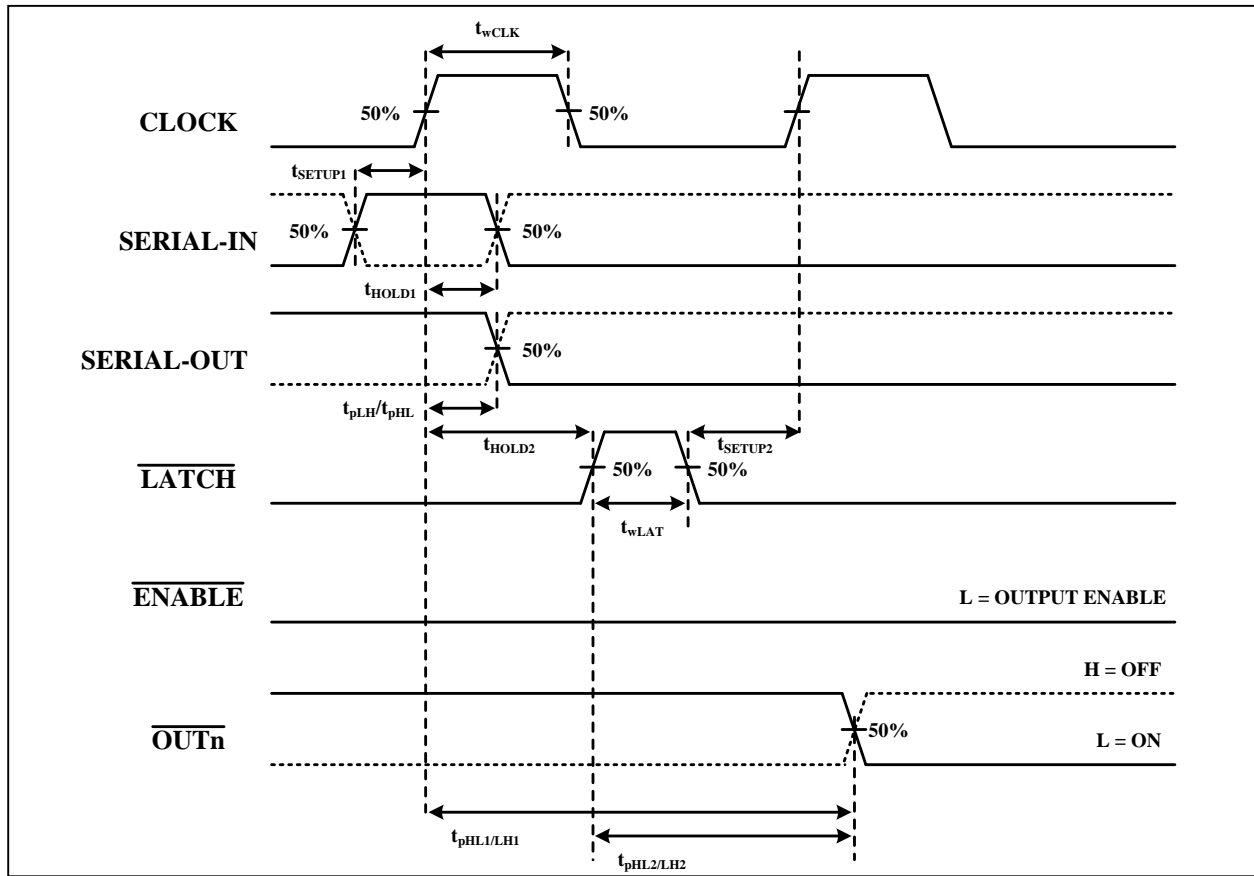
Note 7:

1. If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.
2. Delay between outputs. The IS32FL3726A has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), $\overline{OUT1}$ has 5ns delay, $\overline{OUT2}$ has 10ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before \overline{ENABLE} is low will still turn on and off at the determined delayed time regardless of the state of \overline{ENABLE} . Therefore, every LED will be illuminated for the amount of time \overline{ENABLE} is pulled high.

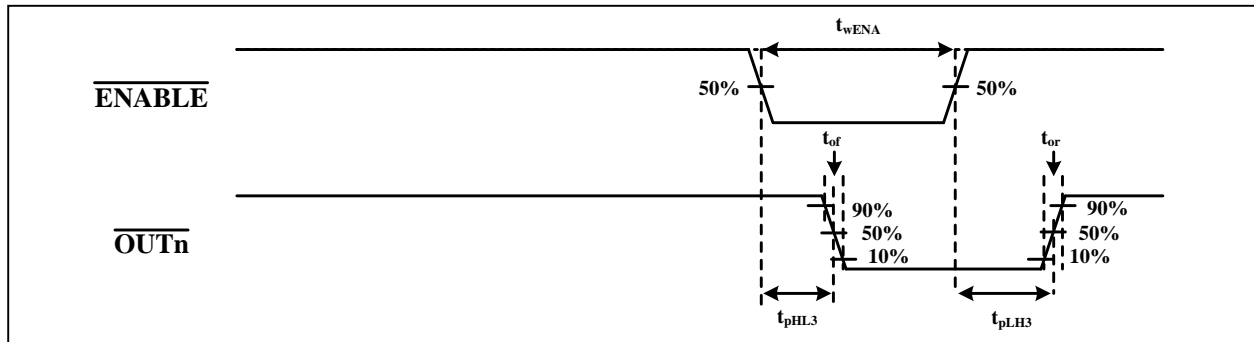
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TIMING WAVEFORM

1. CLOCK, SERIAL-IN, SERIAL-OUT, LATCH, ENABLE, OUTn



2. OUTn



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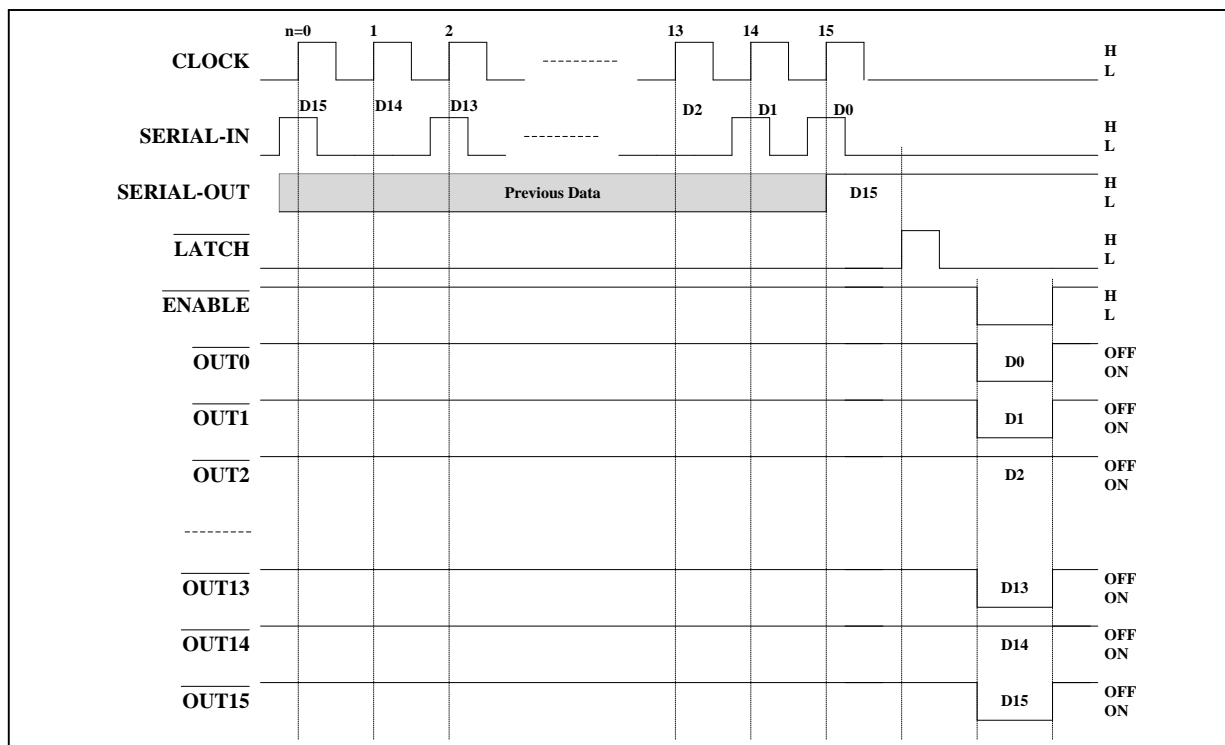


Figure 3 Timing Diagram

Warning: The Latch input is a logic level it is not an edge triggered latch circuit.

Note 8: The serial-in data (SERIAL-IN) will be clocked into a 16 bit shift register synchronized on the rising edge of the clock (CLOCK). The data "1" means the corresponding current output "ON" for output, the data "0" represents for "OFF". The data will be transferred into the 16 bit latch register when the signal (L A T C H) is 'H' (level trigger); otherwise, the data will be latched. The trigger timing of the serial-out data (SERIAL-OUT) will be shifted out on synchronization to the rising edge of the clock. All outputs are turned off while enable terminal (E N A B L E) is kept at high level. And they are active when E N A B L E turns to low.

Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ... OUT7 ... OUT15	SERIAL-OUT
↑	H	L	Dn	Dn ... Dn-7 ... Dn-15	Dn-15
↑	L	L	Dn+1	No change	Dn-14
↑	H	L	Dn+2	Dn+2 ... Dn-5 ... Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2 ... Dn-5 ... Dn-13	Dn-13
↓	X	H	Dn+3	OFF	Dn-13

Warning: The following conditions, $\overline{ENABLE}=0$, $\overline{LATCH}=1$, $\overline{SERIAL-IN}=1$, cannot be configured at the same time when power is on, or IS32FL3726A will behave unpredictably.

Note 9: $\overline{OUT0}$ to $\overline{OUT15}$ =On when $D_n = H$; $\overline{OUT0}$ to $\overline{OUT15}$ =Off when $D_n = L$. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

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TYPICAL TEST CHARACTERISTICS

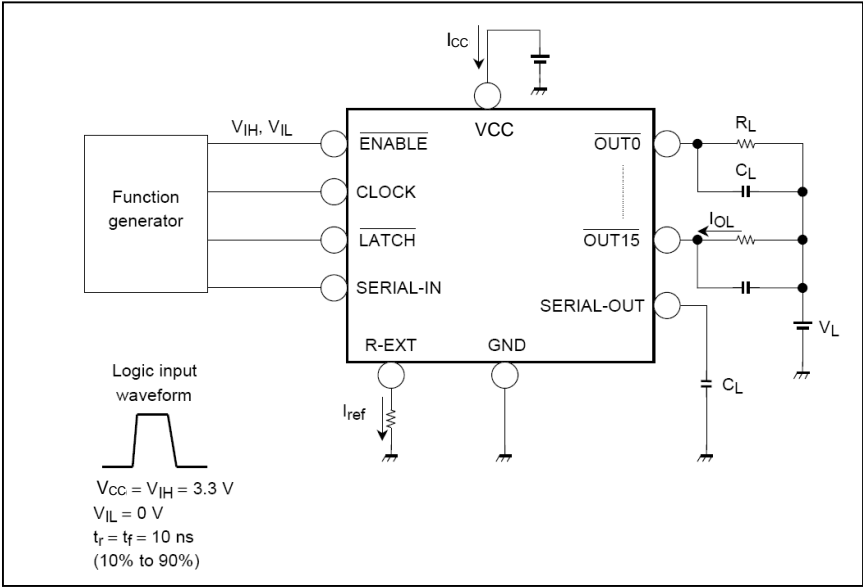


Figure 4 Test Diagram

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APPLICATION INFORMATION

ADJUSTING OUTPUT CURRENT

The output current of each channel is set by an external resistor R_{EXT} , the relationship between I_{OUT} and R_{EXT} is:

$$I_{OUT} = k \times \frac{V_{REXT}}{R_{EXT}}$$

Where V_{REXT} is 1.26V, k is 15, so I_{OUT} is calculated by Equation (1):

$$I_{OUT} = 15 \times \frac{1.26V}{R_{EXT}} \quad (1)$$

As show in the figure below:

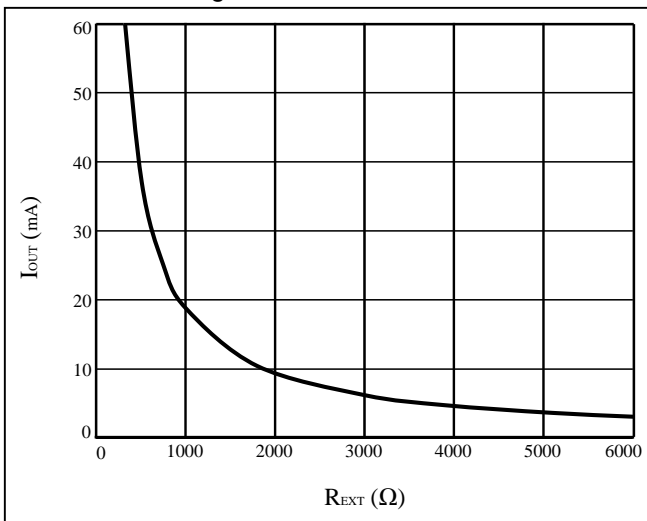


Figure 5 I_{OUT} vs. R_{EXT}

CONSTANT CURRENT OUTPUT

In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage below.

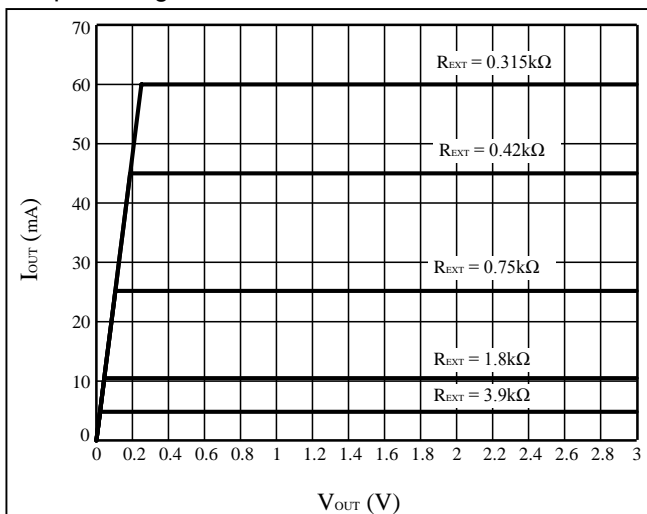


Figure 6 I_{OUT} vs. V_{OUT}

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA} , determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt ($^{\circ}C/W$).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (2):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (2)$$

$$\text{So, } P_{D(MAX)} = \frac{125^{\circ}C - 25^{\circ}C}{28.1^{\circ}C/W} \approx 3.56W$$

Figure 7 shows the power derating of the IS32FL3726A on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

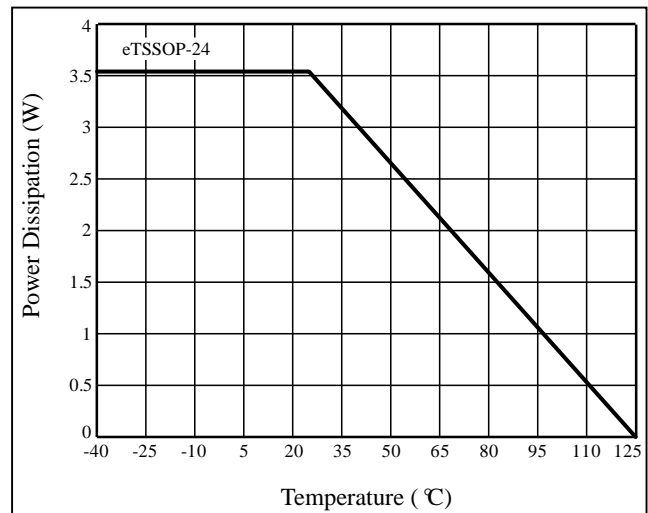


Figure 7 Dissipation Curve

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CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

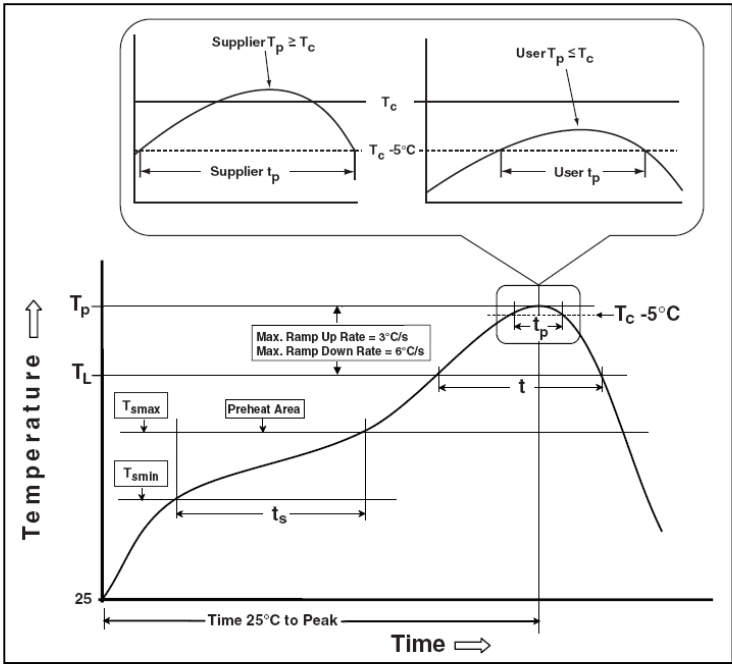
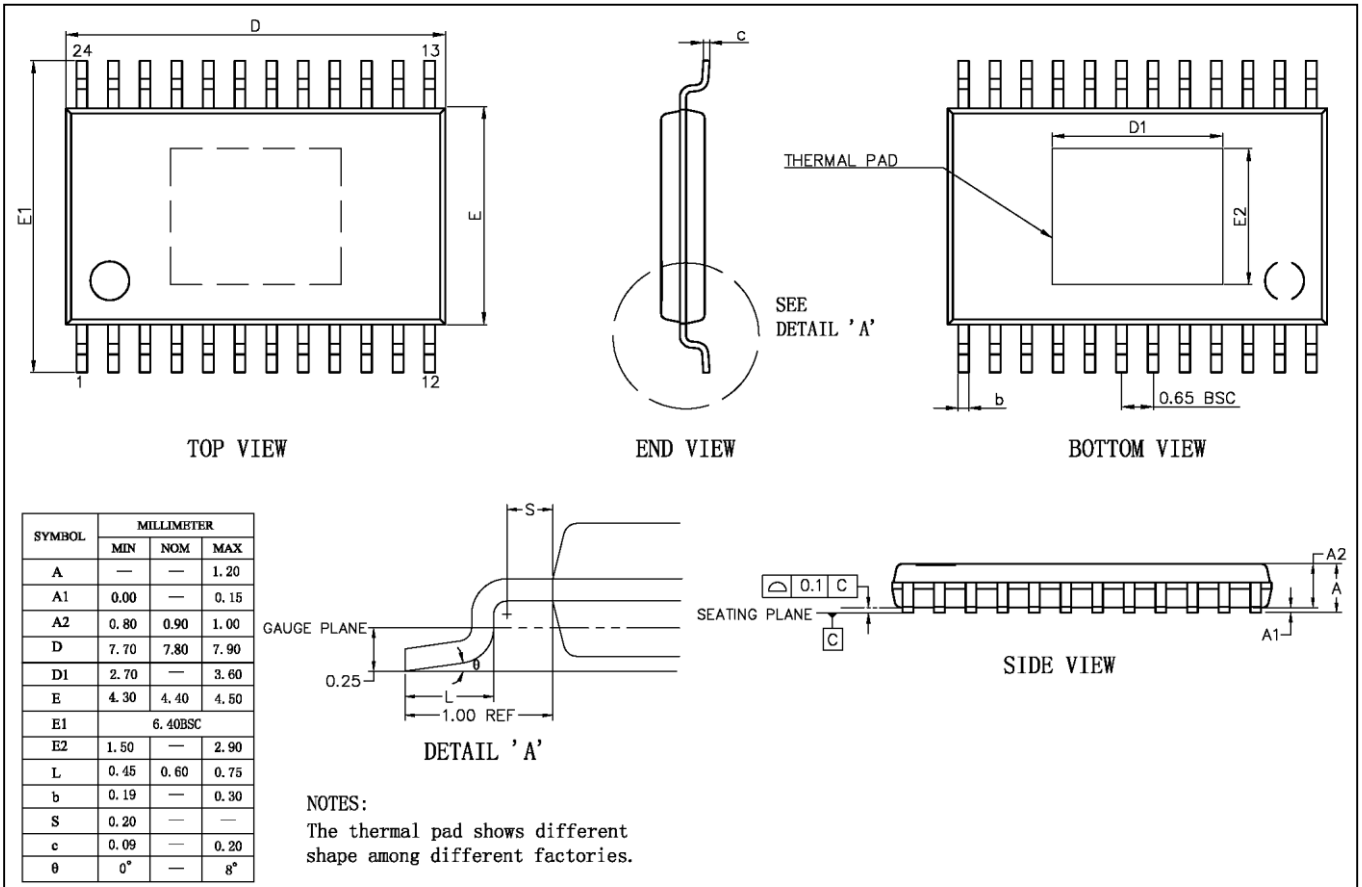


Figure 8 Classification Profile

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PACKAGE INFORMATION

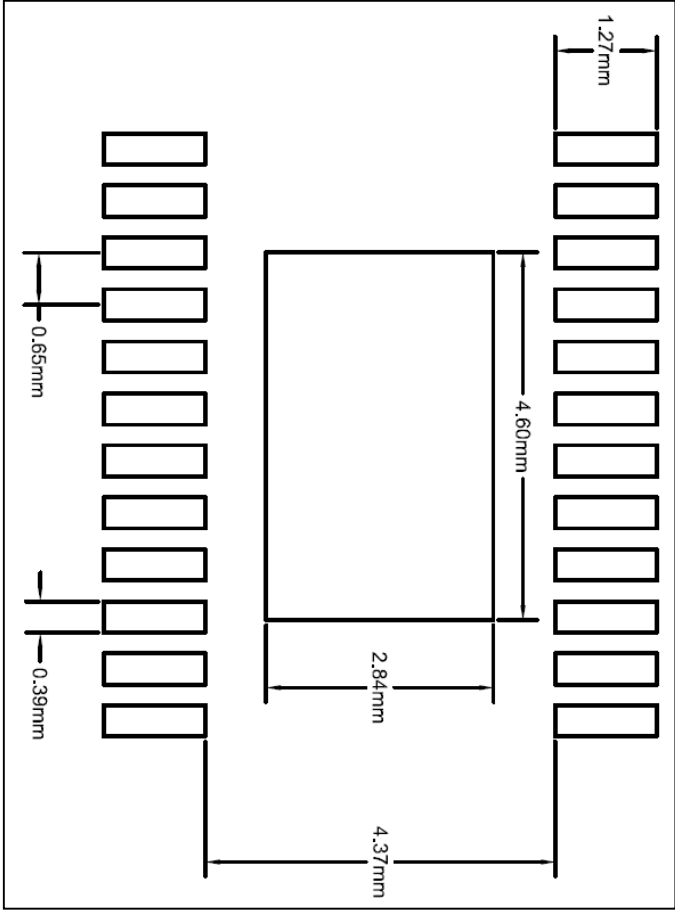
eTSSOP-24



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RECOMMENDED LAND PATTERN

eTSSOP-24



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2020.09.04
0B	Update EC table	2020.12.11
A	Release to mass production	2021.02.08
B	Update AEC-Q100 qualified	2021.06.18