NCP1612GEVB

160-W, Wide Mains, PFC Stage Driven by the NCP1612 Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

Housed in a SO-10 package, The NCP1612 is designed to drive PFC boost stages in so-called Current Controlled Frequency Fold-back (CCFF). In this mode, the circuit classically operates in Critical conduction Mode (CrM) when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1612 linearly decays the frequency down to about 20 kHz when the current is nearly zero. CCFF maximizes the efficiency throughout the load range. Incorporating protection features for rugged operation, it is furthermore ideal in systems where cost-effectiveness, reliability, low stand-by power and high-efficiency are the key requirements.

Extremely slim, the NCP1612 evaluation board is designed to be less than 13-mm high. This low-profile PFC stage is intended to deliver 160 W under a 390 V output voltage from a wide mains input. This is a PFC boost converter as used in Flat TVs, High Power LED Street Light power supplies, and all-in-one computer supplies. The demo board embeds the NCP1612 B-version which is best appropriate for the self-biased configuration. The board is also configurable to have the NCP1612 powered from an external power source. In this case, apply a V_{CC} voltage that exceeds the NCP1612B start-up level (18.2 V max) to ensure the circuit start of operation or solder the NCP1612A instead. The low V_{CC} start-up level of the A-version (11.25 V max.) allows the circuit powering from a 12-V rail. Both versions feature a large V_{CC} operating range (from 9.5 V up to 35 V).

Table 1. ELECTRICAL SPECIFICATIONS

Description	Value	Units
Input Voltage Range	90-265	Vrms
Line Frequency Range	45 to 66	Hz
Output Power	160	W
Minimum Output Load Current(s)	0	Adc
Number of Outputs	1	
Nominal Output Voltage	390	Vdc
Maximum Startup Time	< 3	s
Target Efficiency at Full Load (115 V_{rms})	95	%
Load Conditions For Efficiency Measurements (10%, 20%,..)	10-100	%
Minimum Efficiency At 20% Load, 115 V_{rms}	93	%
Minimum PF Over The Line Range At Full Load	95	%
Hold-Up Time (the output voltage remaining above 300 V)	> 10	ms
Peak To Peak Low Frequency Output Ripple	< 8	%

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THE BOARD

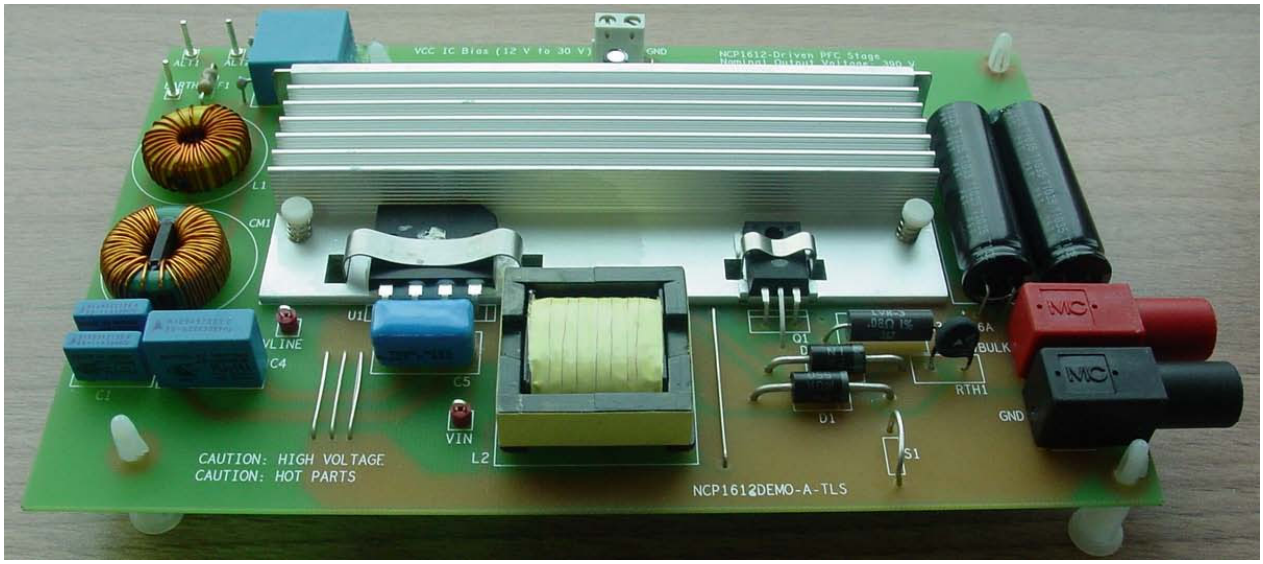


Figure 1. A Slim Board (Height < 13 mm)

APPLICATION SCHEMATIC

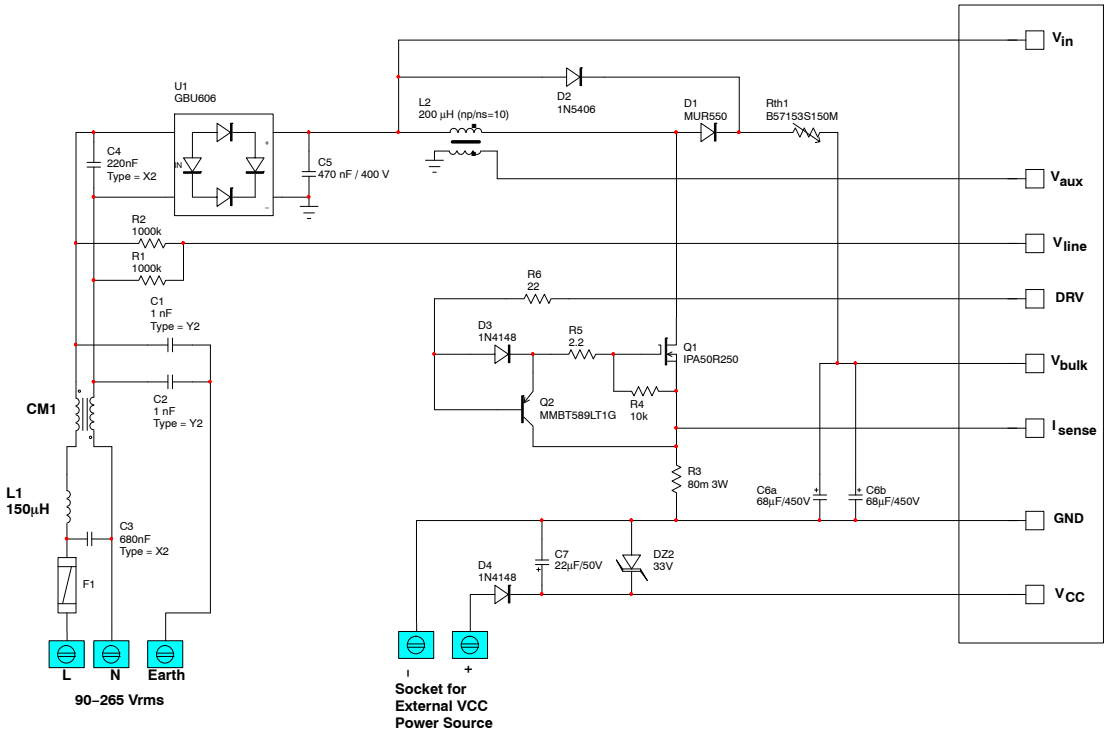


Figure 2. Application Schematic − Power Section

If an external V_{CC} voltage is applied to the board (as allowed by the socket for external V_{CC} power sourcing), it should be noted that the NCP1612 latches off if this voltage exceeds about 30 V (see pfcOK section). In this case, unplug the PFC stage to recover operation. In all events, do not apply more than 33 V to the V_{CC} socket not to exceed the DZ_2 reverse ZENER voltage (see Figure 2).

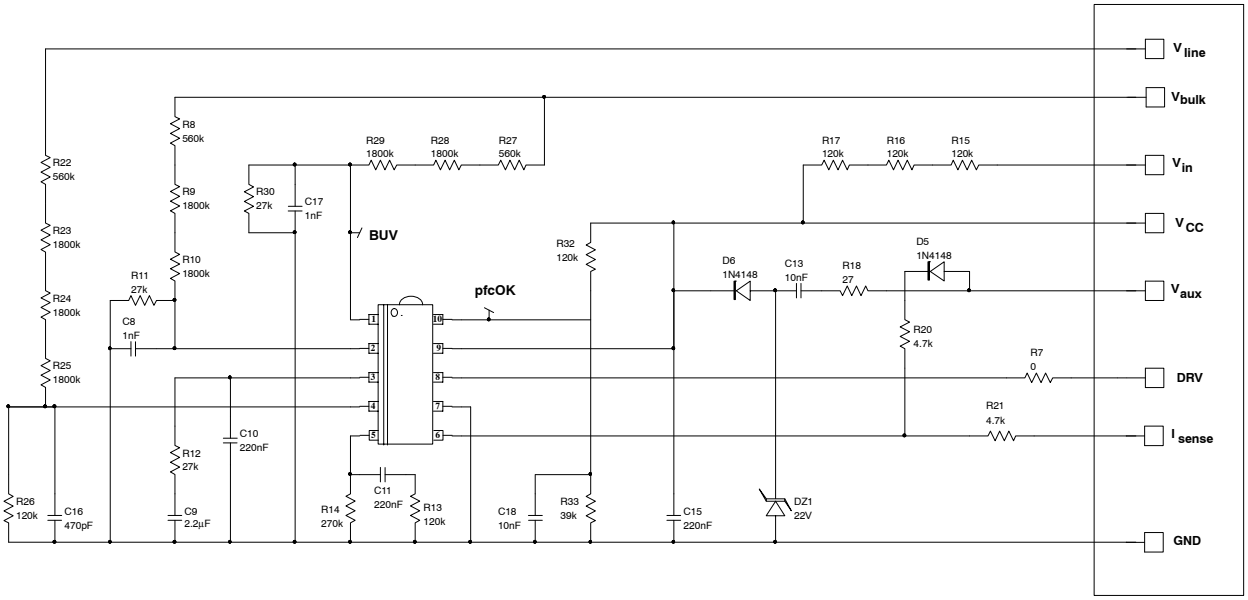
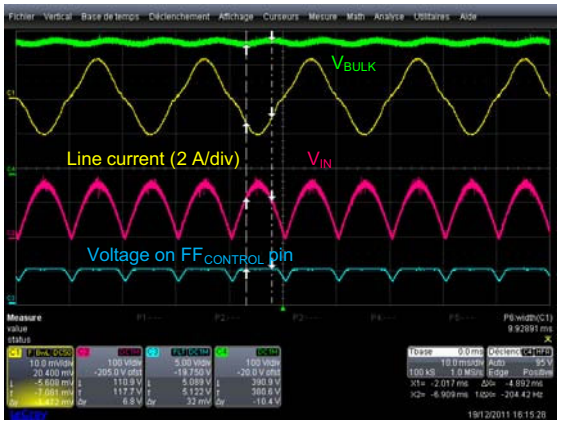
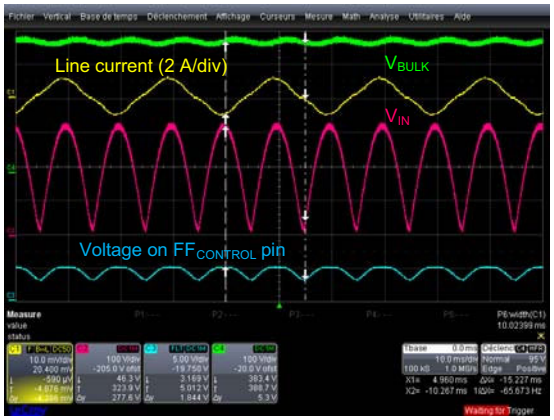


Figure 3. Application Schematic – Control Section

GENERAL BEHAVIOR – TYPICAL WAVEFORMS



a.) 115 V



b.) 230 V

Figure 4. General Waveforms at Full Load

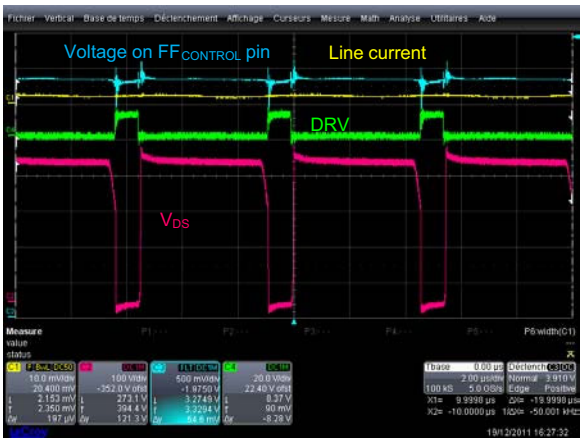
CCFF OPERATION

The NCP1612 operates in so called Current Controlled Frequency Fold-back (CCFF) where the circuit operates in Critical conduction Mode (CrM) when the instantaneous line current is medium or high. When this current is lower than a preset level, the frequency linearly decays to about 20 kHz. CCFF maximizes the efficiency at both nominal and light loads (*). In particular, stand-by losses are minimized.

To further optimize the efficiency, the circuit skips cycles near the line zero crossing where the power transfer is particularly inefficient. This is at the cost of some current distortion. If superior power factor is needed, forcing a minimum 0.75 V voltage on the “FFcontrol” inhibits this function.

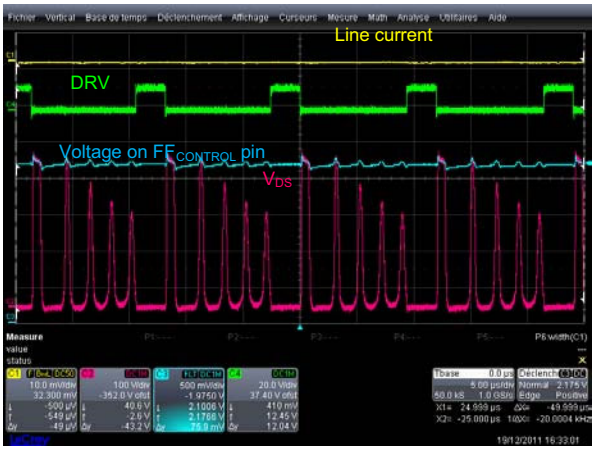
Practically, the FFcontrol pin of the NCP1612 generates a voltage representative of the instantaneous line current. When this voltage exceeds 2.5 V, the circuit operates in CrM. If the FFcontrol voltage is below 2.5 V, the circuit forces a delay (or dead-time) before re-starting a DRV cycle which is proportional to the difference between 2.5 V reference and the FFcontrol voltage. This delay is maximum when the FFcontrol voltage is 0.75 V (about 45 µs) so that a nearly 20 kHz operation is obtained. Below this 0.75 V level, the circuit skips cycles.

*Like in FCCrM controllers, internal circuitry allows near-unity power factor even when the switching frequency is reduced.



a) CrM operation at the top of the sinusoid

b) Reduced frequency at a lower level of the sinusoid



c) Low frequency near the line zero crossing

Figure 5. CCFF Operation (230 V, 0.2 A Load Current)

Figure 5 illustrates the CCFF operation at 230 V, 200 mA loading the PFC stage:

1. At the top of the sinusoid, the FFcontrol pin voltage (that is representative of the line current) exceeds 2.5 V and the circuit operates in critical conduction mode (see Figure 5a).
2. As the input voltage decays, so do the line current and the FFcontrol pin voltage. The FFcontrol being lower than 2.5 V, the circuit starts to reduce the frequency. (see Figure 5b).
3. Near the zero crossing the frequency is further decreased (see Figure 5c).

In all cases, the circuit turns on at a valley:

- At the first valley as classically done in CrM operation
- Or at the first valley following the completion of the dead-time generated by the CCFF function to reduce the frequency.
- The circuit nicely stays “locked” on to valley n until it needs to jump to either valley (n-1) or valley (n+1). In other words, there is no inappropriate transition between two valleys

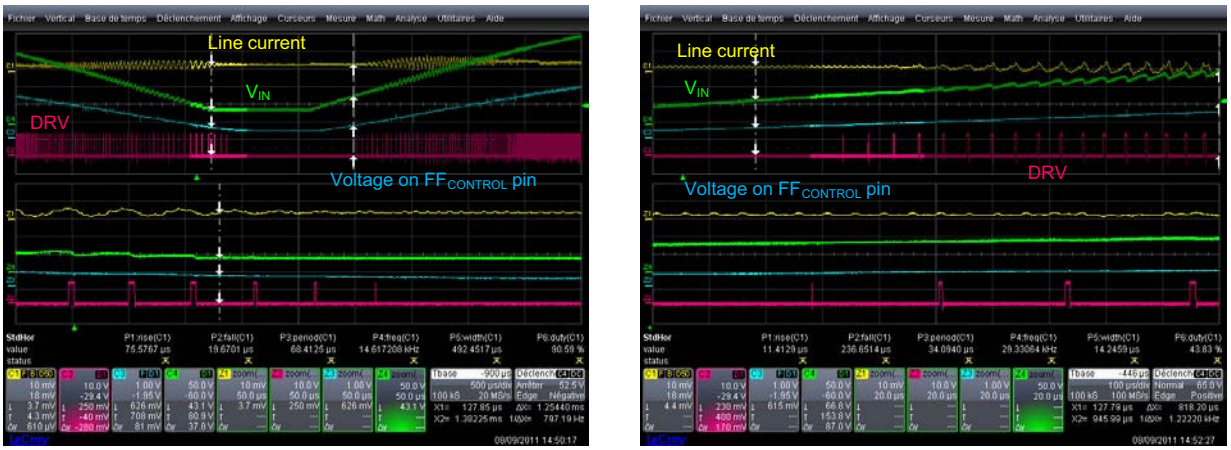
One can also note that the switching frequency being less when the line current is low, the frequency is particularly low at light load, high line, CrM operation being more likely to occur at heavy load, low line. Experience shows that this behavior helps optimize the efficiency in all conditions.

Similarly, the skipping period of time (near the line zero crossing) visible in Figure 9 (for the particular case of the operation at 265 V and 20% of the load):

- Is nonexistent or very short at low line, heavy load
- Is longer when the load diminishes and the line magnitude

Let us remind that the skip function optimizes the efficiency but this is at the cost of a limited current distortion. If superior power factor is needed, forcing a minimum 0.75 V voltage on the “FFcontrol” pin inhibits this function.

Refer to the data sheet for a detailed explanation of the CCFF operation and of its implementation in the NCP1612 [3].



a) Soft Skip Beginning

b) Soft Operation Recovery

Figure 6. The NCP1612 Enters and Leaves Skip Mode in a Soft Manner

As illustrated by Figure 6, the circuit does not abruptly interrupt the switching when it enters skip mode. Instead, the on-time is gradually decreased to zero in 3 to 4 switching periods typically. Similarly, the circuit recovers operation in a soft manner.

NO LOAD LOSSES

The input power is measured no load being connected. An external 15-V V_{CC} is applied.

Resistors R_{15}, R_{16} and R_{17} of Figure 3 that are implemented to charge the V_{CC} capacitor at start-up, draw a large bias current $\left(\frac{V_{in} - V_{cc}}{R_{15} + R_{16} + R_{17}}\right)$ from the input voltage. They are disconnected for this test.

In these conditions, we measured:

	115 V (60 Hz)	230 V (50 Hz)
Input power	92 mW	118 mW
I_{CC}	2.0 mA	1.9 mA

The V_{CC} consumption is almost constant over the V_{CC} range (e.g., 2.2 mA at 30 V, low line).

It must be noted that the input power mainly results from static losses:

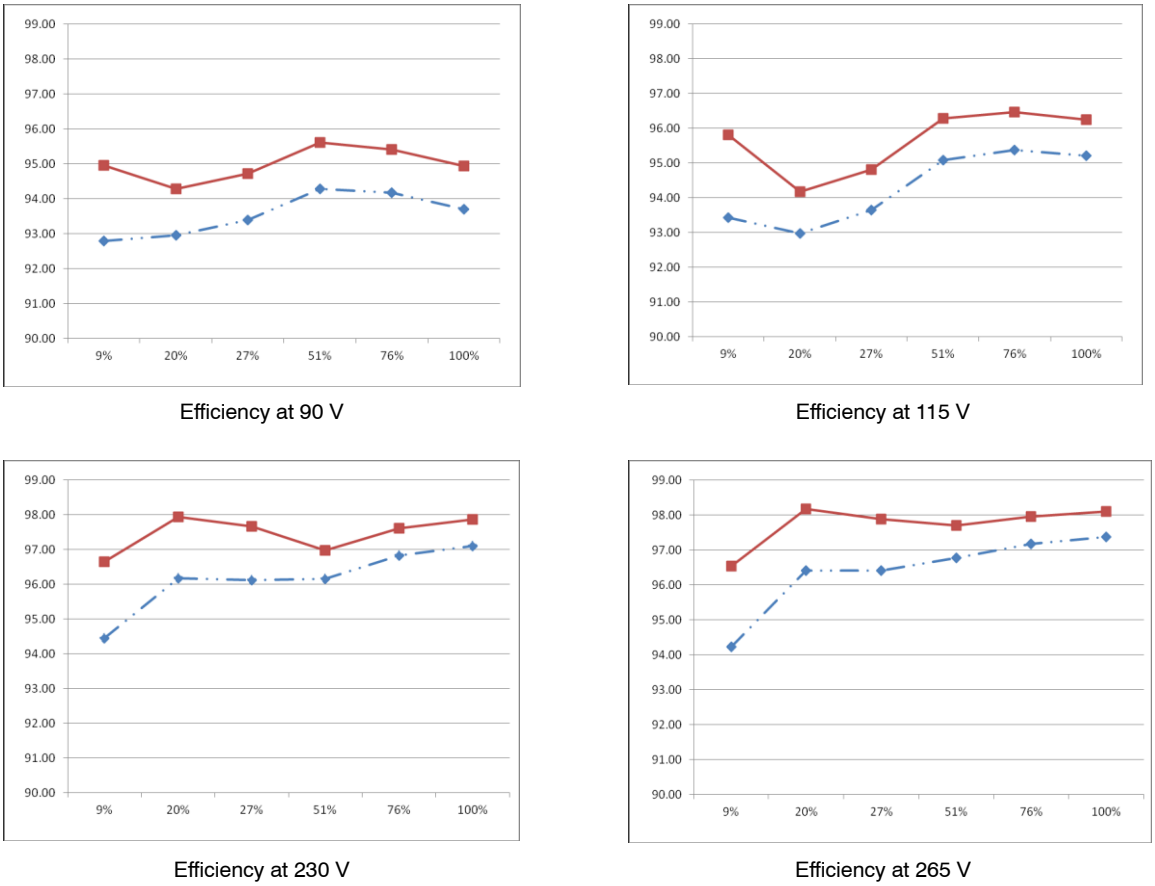
- Discharge resistors for X2 capacitors (R_1 and R_2 of Figure 2) consume $\left(\frac{V_{line,rms}^{2}}{R_1 + R_2}\right)$ that is about 7 mW at 115 V and 26 mW at 230 V.
- Two resistors sensing networks are implemented to sense the bulk voltage (redundant bulk voltage monitoring). At both line voltages, they consume $\left(\frac{V_{bulk}^{2}}{R_8 + R_9 + R_{10} + R_{11}} + \frac{V_{bulk}^{2}}{R_{22} + R_{23} + R_{24} + R_{25}}\right)$ that is about 72 mW. These losses can be easily reduced if needed by using one single resistors divider for pins 1 and 2 and/or by increasing the impedance of the sensing networks.

These static losses cost 79 mW at low line and 98 mW at high line. As a matter of fact, the losses linked to the PFC stage operation are very small.

The measurements were made at 25°C ambient temperature by means of a power meter CHROMA 66202 used in accumulation mode (W.h measurement over 6 minutes, the result being multiplied by 10 to obtain the averaged power).

POWER FACTOR AND EFFICIENCY

The NCP1612 evaluation board embeds a NTC to limit the in-rush current that takes place when the PFC stage is plugged in. The NTC placed in series with the boost diode. This location is rather optimum in term of efficiency since it is in the in-rush current path at a place where the rms current is less compared to the input side. However, this component still consumes some power. That is why the efficiency is given with the NTC and with the NTC being shorted.



Efficiency at 90 V

Efficiency at 115 V

Efficiency at 230 V

Efficiency at 265 V

Figure 7. Efficiency versus Load of the Evaluation Board (blue dotted line), of the Evaluation Board where the NTC is shorted (red solid line)

Figure 7 displays the efficiency versus load at different line levels. When considering efficiency versus load, we generally think of the traditional bell-shaped curves:

- At low line, the efficiency peaks somewhere at a medium load and declines at full load as a result of the conduction losses and at light load due to the switching losses.
- At high line, the conduction losses being less critical, efficiency is maximal at or near the maximum load point and decays when the power demand diminishes due to the increasing impact of the switching losses.

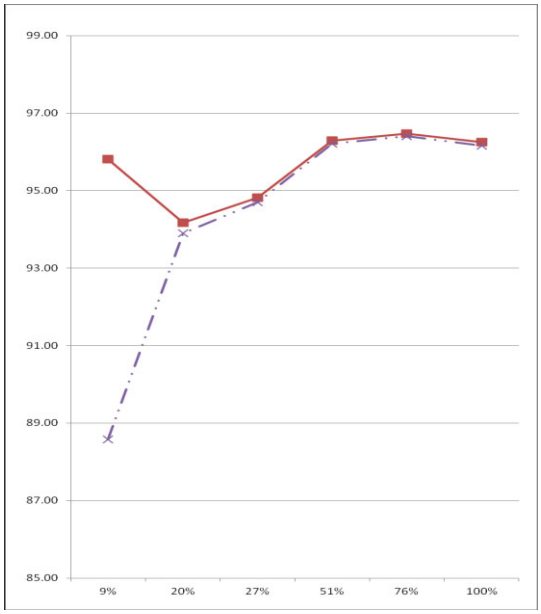
Curves of Figure 7 meet this behavior in the right-hand side where our demo-board resembles a traditional CrM PFC stage. In the left-hand side, the efficiency normally drops because of the switching losses until an inflection point where it rises up again as a result of the CCFF operation. As previously detailed, CCFF makes the switching frequency decay linearly as a function of the instantaneous line current when it goes below a preset level. As detailed in [1], the CCFF threshold is set to 17% of the line maximum current. Hence, the PFC circuit switching frequency is permanently reduced when the power is below 17% of its maximum level at 90 V and below about 50% at 265 V. That is why the aforementioned inflection point is around 20% of the load at low line and 50% of the load at high line, as confirmed by the curves of Figure 8.

Efficiency comparison to a traditional CrM operation.

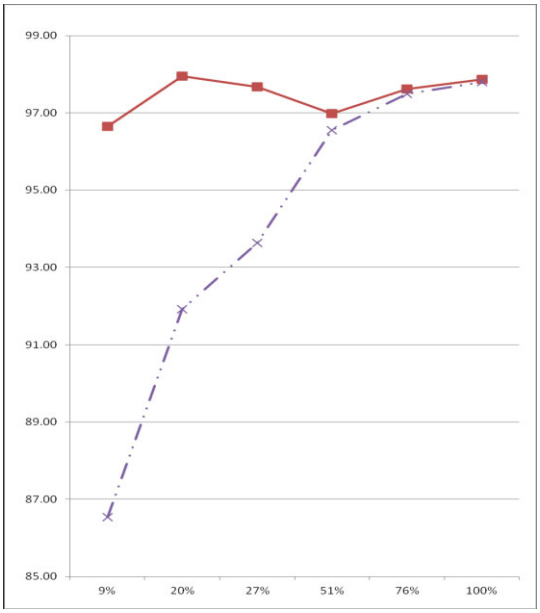
3 V have been forced on the FFcontrol pin of the NCP1612 so that the circuit CCFF function is disabled. Hence, the PFC stage operates in a traditional critical conduction mode (CrM) in all conditions. Figure 8 compares the efficiency with CCFF (evaluation board) to that without CCFF. Otherwise said, CCFF operation is compared to the traditional critical mode solution.

As expected, as long as the switching frequency is not significantly reduced by CCFF, that is above 20% load at low line and above 50% at high line (see previous section), the CCFF and CrM curves matches. At lighter loads, the efficiency is much improved with CCFF.

Let's remind that CCFF works as a function of the instantaneous line current: when the signal representative of the line current (generated by the FFcontrol pin) is lower than 2.5 V, the circuit reduces the switching frequency. This is the case near the line zero crossing whatever the load is. Hence, the switching frequency reduces at the lowest values of the line sinusoid even in heavy load conditions. That is why the efficiency is also improved when the load is high. This is particularly true at high line where CCFF has more effect than at low line since the line current is less.



Efficiency at 115 V



Efficiency at 230 V

Figure 8. Efficiency versus Load of the Evaluation Board (red solid line), of the Evaluation Board Operated in Full CrM (purple dotted line). In both Cases, the NTC is Shorted.

Skip Mode

When the instantaneous line current tends to be very low (below about 5% of its maximum level in our application – refer to [1]), the circuit enters a skip cycle mode. In another words, the circuit stops operating at a moment when the power transfer is particularly inefficient.

This improves the efficiency in light load as shown by Figure 10. The dotted line portrays the efficiency when skip mode is inhibited by forcing a 0.75 V minimum voltage on the FFcontrol pin. The efficiency is improved below 20 % of the load at low line while some benefit is visible starting from 50% of the load at 230 V.

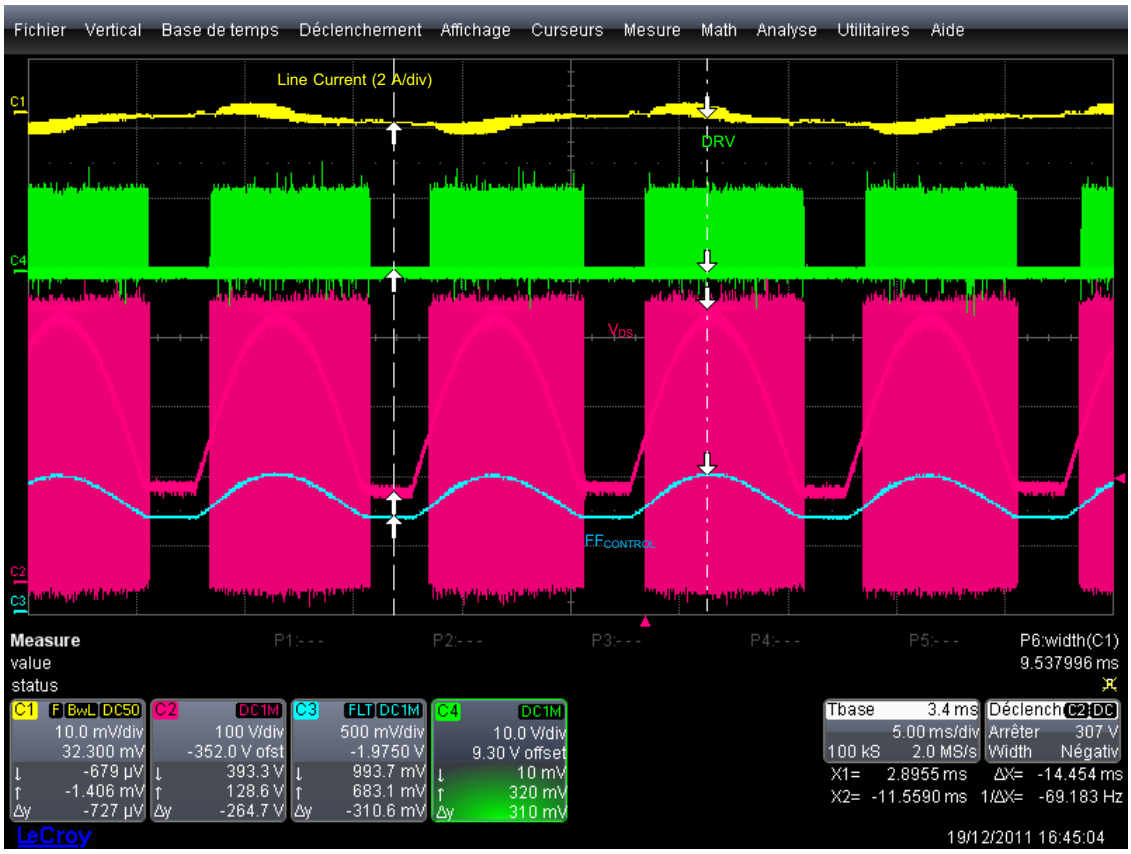
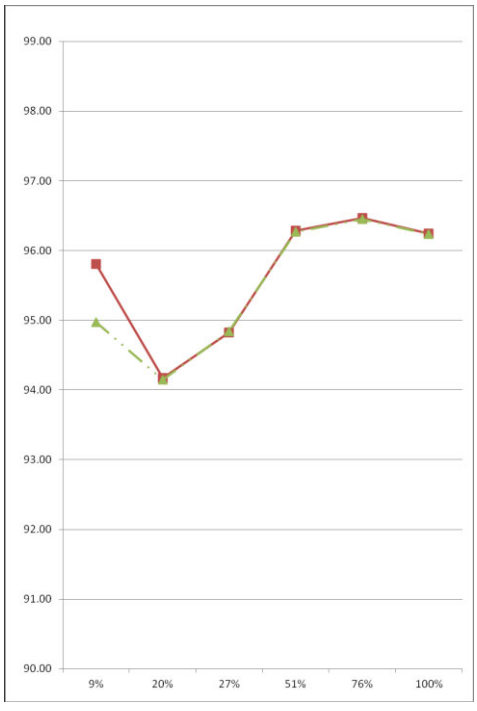
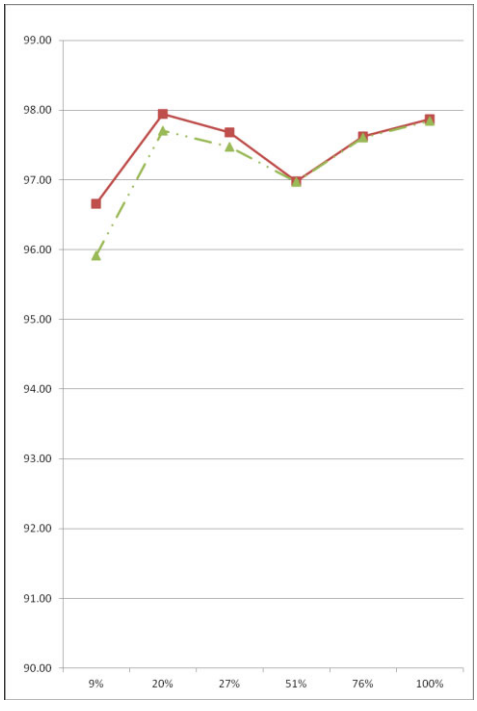


Figure 9. The Circuit Skips Cycle Near the Line Zero Crossing (265 V, 20% Load)



Efficiency at 115 V

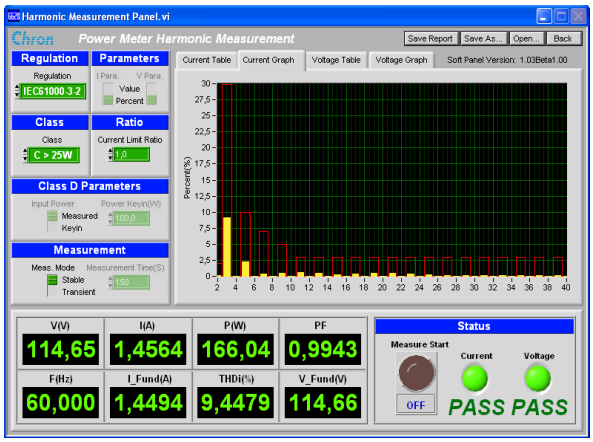


Efficiency at 230 V

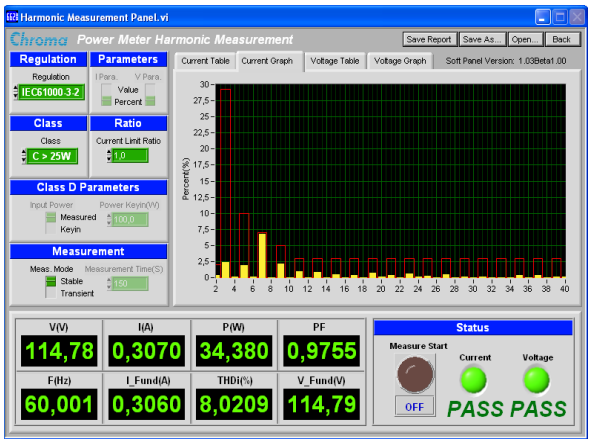
Figure 10. Efficiency versus Load of the Evaluation Board (red solid line) and of the Evaluation Board where Skip Mode is Disabled (green dotted line). In both Cases, the NTC is Shorted.

POWER FACTOR (PF) AND TOTAL HARMONIC DISTORTION (THD)

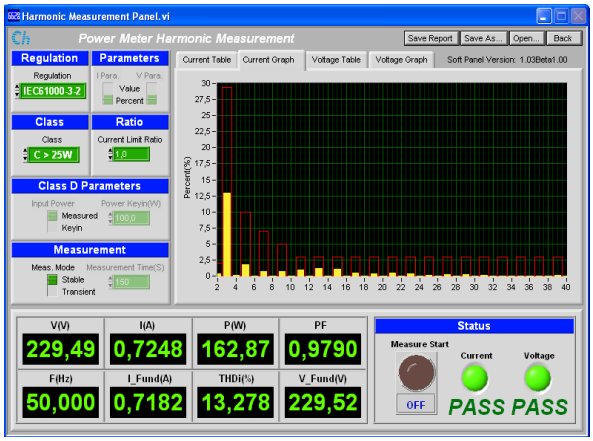
Figure 11 (Figure 12) reports the NCP1612 board performance with respect to the IEC61000-3-2 class C (class D) standards requirements. These results were obtained by means of a CHROMA 66202 Digital Power Meter. They were measured at low and high line, i.e., with respectively, 115 V / 60 Hz and 230 V / 50 Hz being applied to the board and at two power levels: full load and 20% of max. load (that could be considered as a worst case of this type of application).



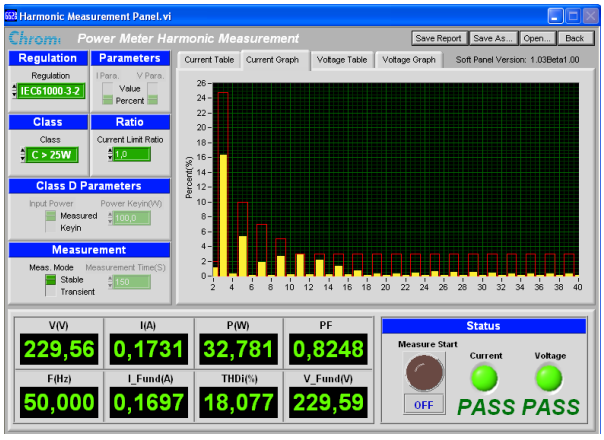
115 V / 60 Hz, full load



115 V / 60 Hz, 20% load

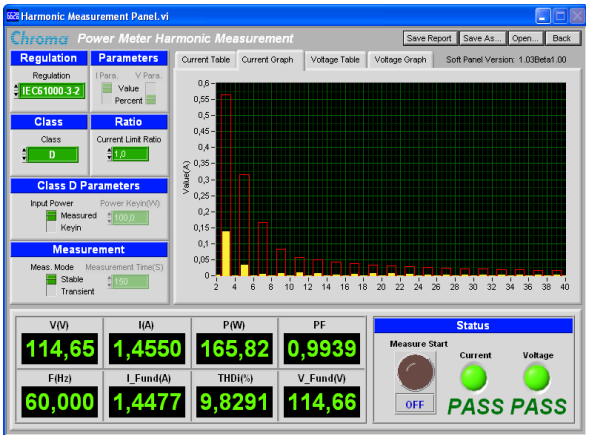


230 V / 50 Hz, full load

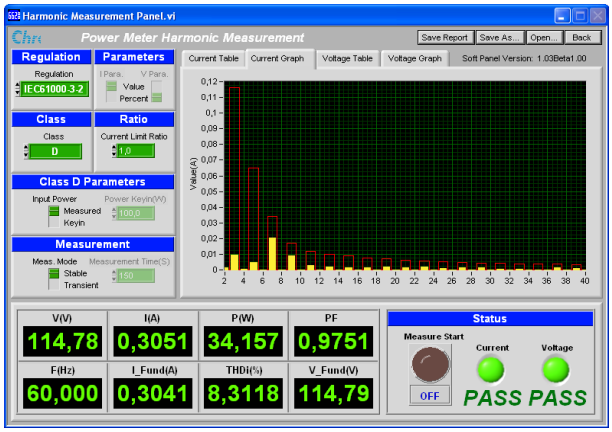


230 V / 50 Hz, 20% load

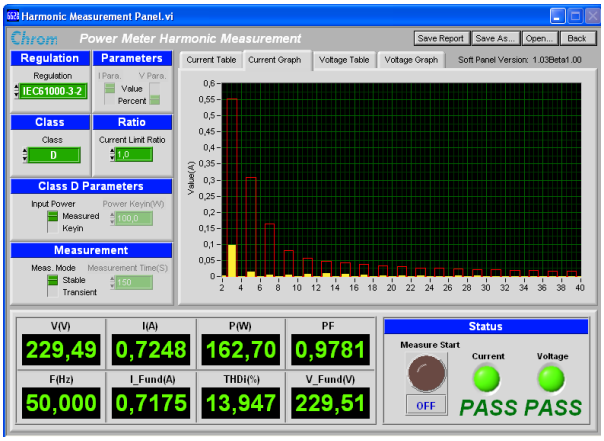
Figure 11. Performance with respect to IEC61000−3−2 Class C Requirements



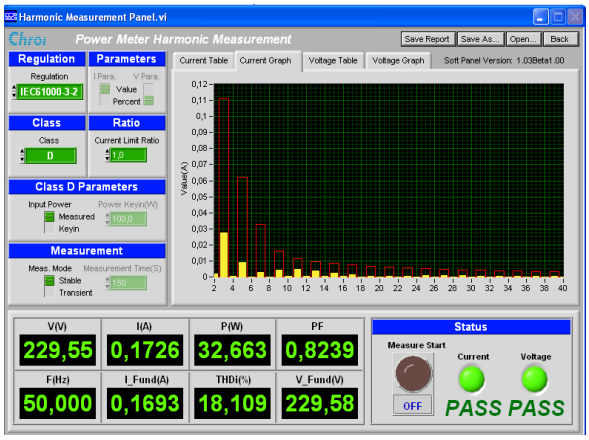
115 V / 60 Hz, full load



115 V / 60 Hz, 20% load



230 V / 50 Hz, full load



230 V / 50 Hz, 20% load

Figure 12. Performance with respect to IEC61000−3−2 Class D Requirements

In the light of Figure 11 and Figure 12, we can see that the NCP1612 board easily passes the standard requirements in the considered conditions. The least margin is observed at 230 V, 20% of the load for class C for which harmonic 11 is closed to the limit. We could check that inhibiting the skip mode (forcing a 0.75 V minimum voltage on the FFcontrol) significantly increases the headroom.

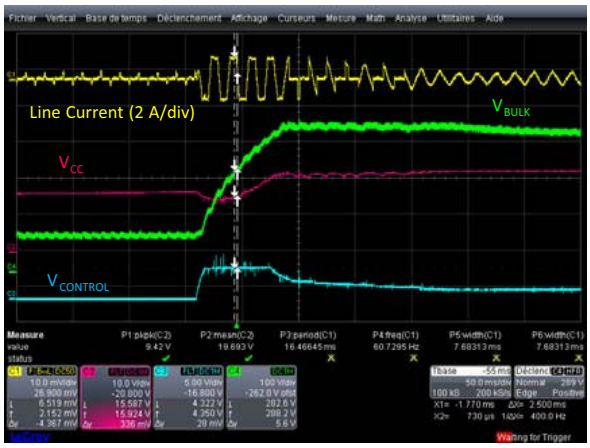
PROTECTION OF THE PFC STAGE

The NCP1612 protection features allow for the design of very rugged PFC stages

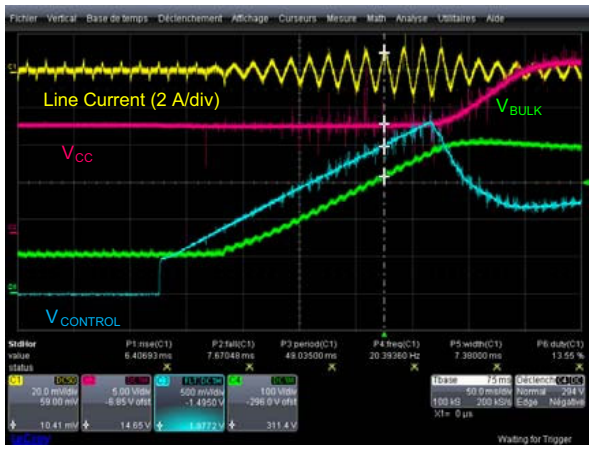
Brown-out

An external 15-V V_{CC} power source is applied to the board. The load is 100 mA. The rms input voltage is decreased with 0.1 V steps.

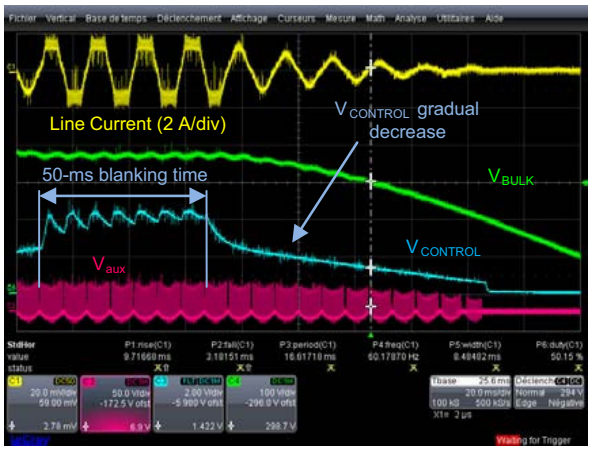
- $(V_{in,rms})_{BOL}$ = 71.3 V (rms line voltage below which the circuit stops operating)
- $(V_{in,rms})_{BOH}$ = 78.6 V (rms line voltage above which the circuit starts to operate)



a) Start of operation when $V_{in,rms}$ exceeds $(V_{in,rms})_{BOH}$ (NCP1612B)



b) Start of operation when $V_{in,rms}$ exceeds $(V_{in,rms})_{BOH}$ (NCP1612A)



c) Abrupt line drop (90 V to 70 V)

Figure 13. Brown−Out Operation

Figure 13a shows the re-start when the input voltage exceeds the 78.6 V BOH level with the NCP1612B. The circuit sharply restarts for a minimized recovery time

Figure 13b shows the same when the NCP1612A is used instead of the NCP1612B. In this case, the circuit smoothly recovers operation (soft start).

Figure 13c shows the NCP1612 behavior when the line voltage becomes too low (NCP1612A or NCP1612B). The line is abruptly changed from 90 V to 70 V at full load. As a line drop result, the bulk voltage decreases and in response, the circuit increases the control signal ($V_{CONTROL}$). This lasts for the 50 ms blanking time of the brown-out function.

At the end of the 50 ms delay, a brown-out situation is detected. $V_{CONTROL}$ is gradually reduced down to its bottom clamp value (0.5 V) leading the line current to steadily decay as well. When $V_{CONTROL}$ has reached 0.5 V, the circuit stops pulsing and grounds the $V_{CONTROL}$ pin to ensure a clean resumption (including soft-start with the NCP1612 A version) when the line is brought back to a level allowing operation.

Over−Current Protection (OCP)

The NCP1612 is designed to monitor the current flowing through the power switch. A current sense resistor (R_3 of Figure 2) is inserted between the MOSFET source and ground to generate a positive voltage proportional to the MOSFET current (V_{CS}). When V_{CS} exceeds a 500 mV internal reference, the circuit forces the driver low. A 200 ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on.

In our application, the theoretical maximal line current is $\left(\frac{1}{2} \times \frac{500\,mV}{80\,m\Omega}\right)$ that is about 3.1 A.

Figure 14 shows the line current when clamped. The over-current situation was obtained at 85 V with a 500 mA load. A 15-V V_{CC} power source was applied to the board.

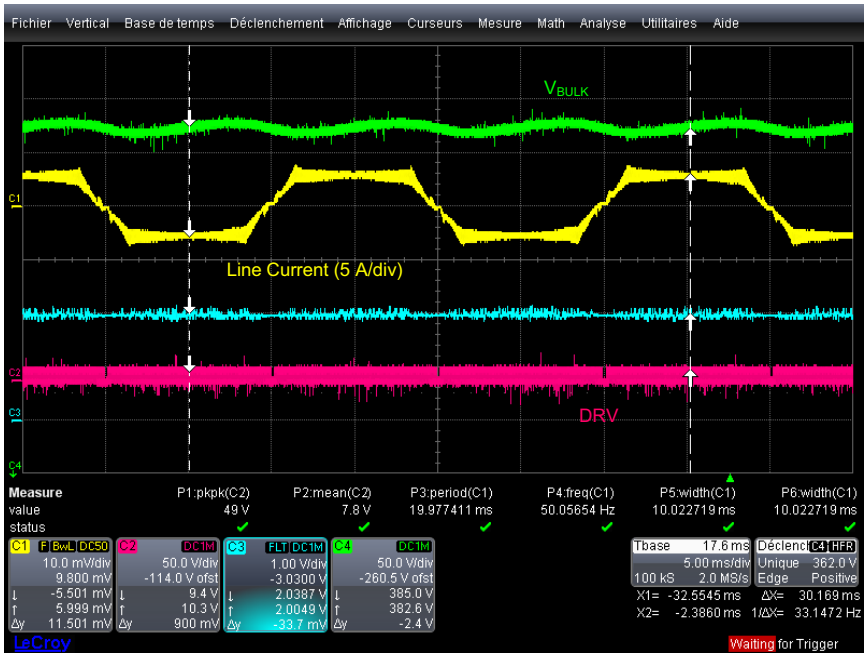


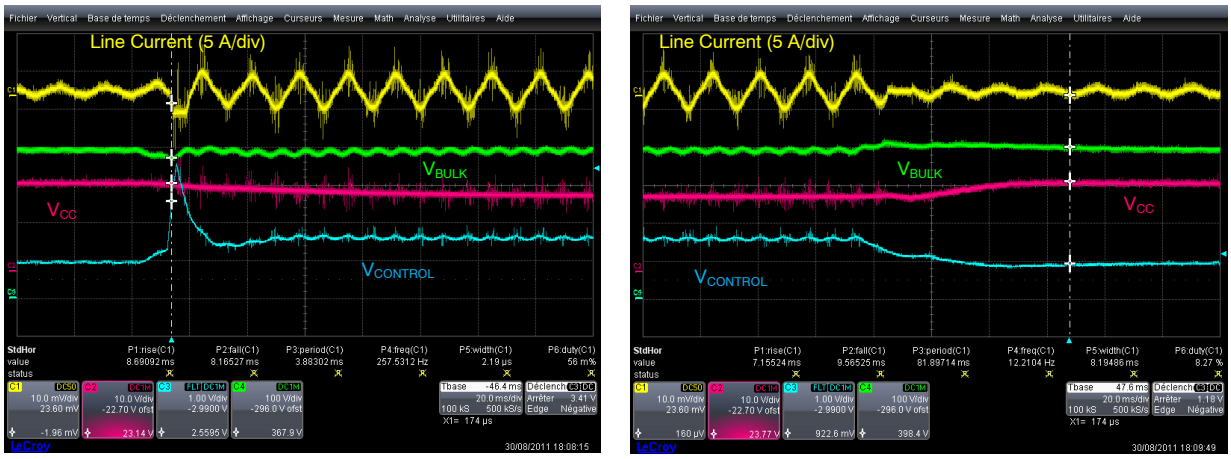
Figure 14. Over−Current Situation (85 V, 0.5 A Load Current)

DYNAMIC PERFORMANCE

The NCP1612 features the **dynamic response enhancer** (DRE) that increases the loop gain by an order of magnitude when the output voltage goes below 95.5% of its nominal level. This function dramatically reduces undershoots in case of an abrupt increase of the load demand.

As an example, Figure 15a illustrates a load step from 100 to 400 mA (2-A/μs slope) at 115 V. One can note that as a result of the DRE function, the control signal ($V_{CONTROL}$) steeply rises when the bulk voltage goes below 370 V, leading to a sudden increase of the line current (in our case, this is so sharp that the over-current protection trips to limit the line current to about 3 A). This sharp reaction dramatically limits the bulk voltage decay. V_{BULK} stays above 365 V and recovers within about 15 ms.

One can further note that the $V_{CONTROL}$ rapidly decreases back to its new steady state level. This is allowed by the use of a type-2 compensation: DRE leads to the charge of the C_{10} capacitor to the high $V_{CONTROL}$ level but C_9 is partly charged only. Our compensation reduces to nearly zero the overshoot that can follow the fast response to an under-voltage.



a) Load abrupt rise

b) Load abrupt decay

Figure 15. Bulk Voltage Variations when the Load Changes from 100 to 400 mA (2 A/μs slope)

Figure 15b shows the other transition from 400 mA to 100 mA. Again the bulk voltage deviation is very small: V_{BULK} remains below 410 V. This is because the soft Over Voltage Protection (softOVP) triggers when V_{BULK} exceeds 105% of its nominal voltage and prevents the DRV from pulsing until V_{BULK} has dropped down to a safe level (103% of its nominal voltage).

Figure 16 shows a magnified view of Figure 15b. It illustrates the gradual interruption of the drive pulses flow for a reduced acoustic noise. The circuit reduces the power delivery by smoothly decaying the on-time to zero within about 50 μs that is 2 to 10 switching periods according to the conditions of a typical application. If the output voltage rise is so fast that V_{BULK} still significantly increases during this braking phase, the fast OVP protection (FOVP) immediately disables the driver when the pin1 voltage exceeds 107% of the 2.5 V voltage reference. In other words, if as generally done, pin1 and the feedback pin receive the same portion of the bulk voltage, the FOVP comparator triggers when the bulk voltage is 107% above the regulation level.

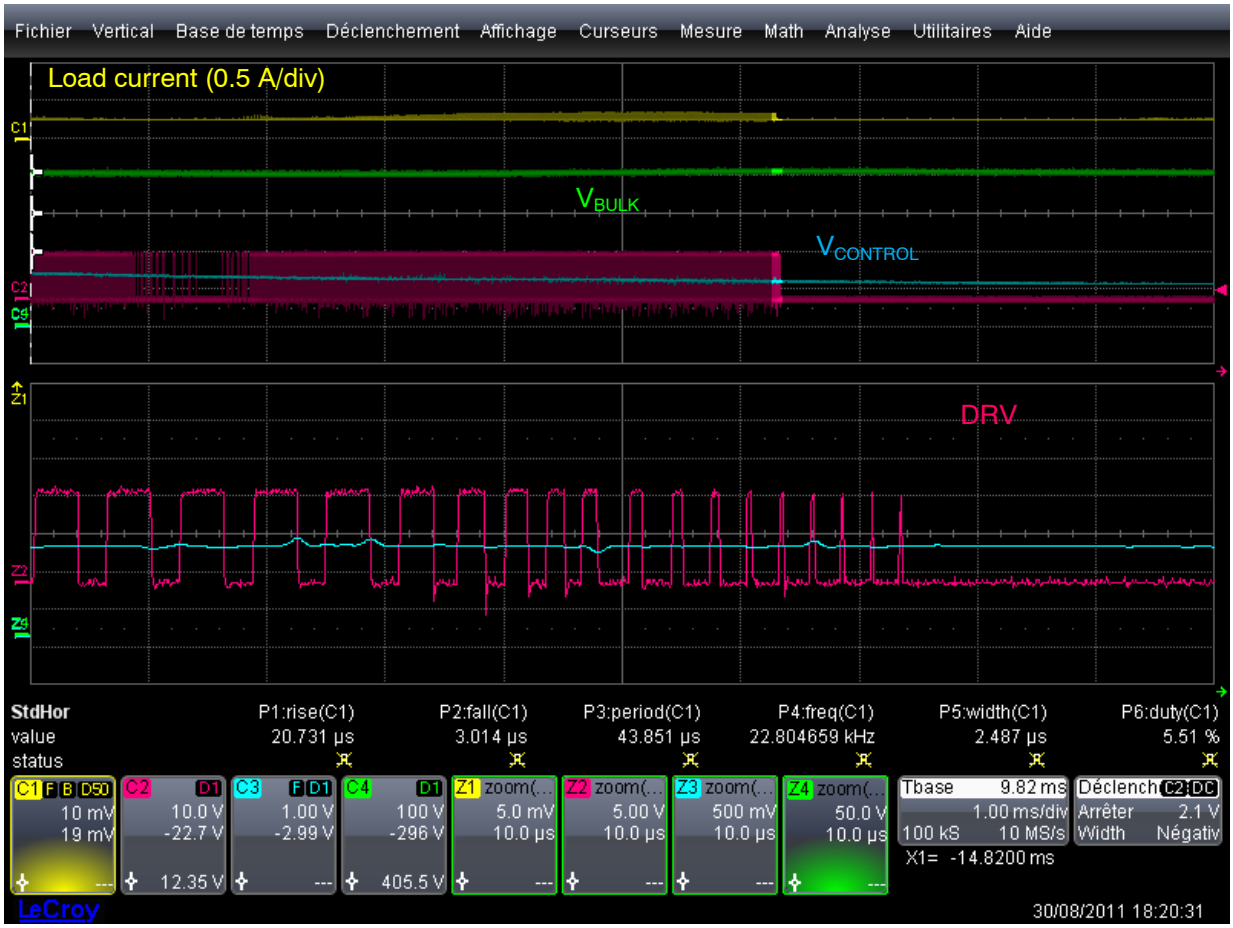


Figure 16. Soft Over−Voltage Protection

pfcOK FUNCTION

The NCP1612 is particularly interesting in applications where the downstream converter is of the forward or half-bridge type, i.e., a converter that takes advantage of a narrow input voltage range. As aforementioned, both the dynamic response enhancer and the soft OVP are of great help in this case by drastically minimizing the bulk voltage deviation under line/load changes. In addition, an optimum sequencing for this application type consists of having the PFC stage started first, the downstream converter entering operation afterwards when the bulk voltage is nominal. The pfcOK pin of the NCP1612 has been designed with the goal of controlling the downstream converter operation:

- The pfcOK pin is grounded when the downstream converter should be disabled
- The pfcOK pin is in high-impedance state otherwise. That is why a portion of V_{CC} is generally applied to this pin to fix the high-state level. In our application, the portion of V_{CC} is controlled by resistors R_{32} and R_{33} of Figure 3.

Typically, the pfcOK pin drives the feedback pin of the downstream converter controller or its brown-out pin when available.

It is recommended to protect the pfcOK pin from surrounding noise. This is the goal of C_{18} of Figure 3.

If the pfcOK pin is pulled up above 7.5 V, the NCP1612 latches off until a brown-out situation is detected or V_{CC} is dropped below its reset level (5 V typically).

In our application, the V_{CC} latched-off level is: $\frac{R_{33} + R_{32}}{R_{33}} \times 7.5\,V = \frac{39k + 120k}{39k} \times 7.5\,V \cong 30.6\,V$

Figure 17a shows the circuit latching off. An external V_{CC} power source was applied and V_{CC} was externally raised until the pfcOK signal exceeds 7.5 V. As a consequence, the NCP1612 stops operating (no drive pulse) and pfcOK pin voltage is grounded.

No operation recovery is possible until either a brown-out condition is detected or V_{CC} is decreased below the reset level (5 V typically). Figure 17b shows operation recovery. A 80 ms mains interruption was produced to trigger the brown-out protection (V_{CC} having been previously decreased below 30 V, that is, below the level leading the part to latch off). The pfcOK signal turns high back when the bulk voltage has reached its regulation level.

a) pfcOK being pulled−up above 7.5 V, the part latches off

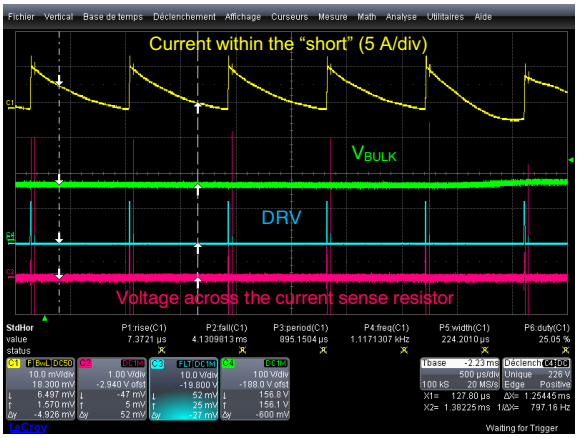
b) the part recovers operation as a result of a mains interruption

Figure 17. NCP1612 Latch−Off Function

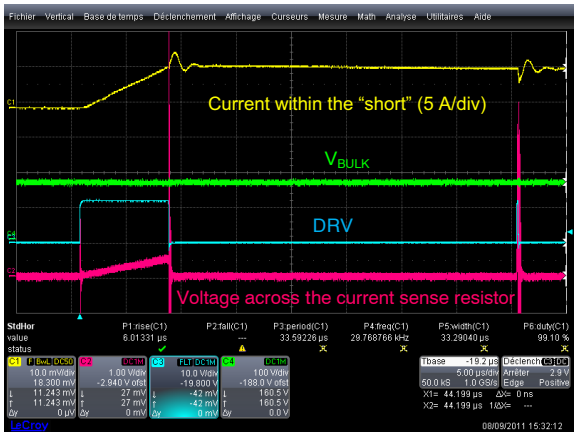
BEHAVIOR UNDER FAILURE SITUATIONS

Elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing incidents, of an excessive operating stress or of other troubles. In particular, adjacent pins of controllers can be shorted, a pin, grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1612 integrates functions that help meet this requirement, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode. Application note AND9079/D details the behavior of a NCP1612-driven PFC stage under safety tests [2].

As an example, we will illustrate here the circuit operation when the PFC bypass diode is shorted. When the PFC stage is plugged in, a large in-rush current takes place that charges the bulk capacitor to the line peak voltage. Traditionally, a bypass diode (D_2 in the application schematic of Figure 2) is placed between the input and output high-voltage rails to divert this inrush current from the inductor and boost diode. When it is shorted, the bulk voltage being equal to the input voltage, the inductor cannot demagnetize but only by virtue of the inductor and boost diode conduction losses. This is generally far insufficient to prevent a cycle-by-cycle cumulative rise of the inductor current and an unsafe heating of the inductor, of the MOSFET and of the boost diode.



a) General view



b) Magnified view

Figure 18. Shorting the Bypass Diode and the NTC

The NCP1612 incorporates a second over-current comparator that trips whenever the MOSFET current happens to exceed 150% of its maximum level. Such an event can happen when the current slope is so sharp that the main over-current comparator cannot prevent the current from exceeding this second level as the result of the inductor saturation for instance. In this case, the circuit detects an “overstress” situation and disables the driver for an 800 μs delay. This long delay leads to a very low duty-ratio operation to dramatically limit the risk of overheating.

Figure 18 illustrates the operation while the bypass diode and the NTC are both shorted at 115 V with a 0.1 A load current, the NCP1612 being supplied by a 15 V external power source. Two drive pulses occur every 800 μs. The first pulse is limited by the over-current protection. Since the input and output voltages are equal, the inductor has not demagnetized when the next pulse is generated and the MOSFET turns on while the boost diode is still conducting a large current (see Figure 18b). Hence, the MOSFET closing causes the second over-current comparator to trip and an “overstress” situation is detected. As the consequence, no DRV pulse can occur until an 800 μs delay has elapsed. The very low duty-ratio operation prevents the application from heating up.

Please note that we do not guarantee that a NCP1612-driven PFC stage necessarily passes all the safety tests and in particular the bypass diode short one since the performance can vary with respect to the application or the test conditions. The reported results are intended to illustrate the typical behavior of the part in one particular application, highlighting the protections helping pass the safety tests. The reported tests were made at 25°C ambient temperature.

BILL OF MATERIALS

Reference	Qty	Description	Value	Tolerance / Constraints	Footprint	Manufacturer	Part number
HS_1	1	Heatsink				COLUMBIA-STAVER	TP207ST,120,12.5, NA,SP,03
F_1	1	4-A fuse	4 A	250 V	through-hole	Multicomp	MCPEP 4A 250V
C_1, C_2	2	Y capacitors	1 nF	275 V	through-hole	EPCOS	B32021A3102
C_3	1	X2 capacitor	680 nF	277 V	through-hole	EPCOS	B32922C3684K
C_4	1	X2 capacitor	220 nF	277 V	through-hole	EPCOS	B32922C3224K
C_5	1	Filtering capacitor	470 nF	450 V	through-hole	EPCOS	B32592C6474K
C_{6a}, C_{6b}	2	Bulk capacitor	68 μF	450 V	through-hole	Rubycon	450QXW68M12.5X40
C_7	1	Electrolytic capacitor	22 μF	50 V	through-hole	various	various
U_1		Diodes Bridge	GBU406	4 A, 600 V	through-hole	LITE-ON	GBU406
L_1	1	DM Choke	117 μH	75 mΩ	through-hole	Pulse Engineering	PH9081NL
CM_1	1	Common Mode Filter	8.5 mH	85 mΩ	through-hole	Pulse Engineering	PH9080NL
L_2	1	Boost inductor	200 μH	6 Apk	through-hole	Wurth Elektronik	750370081 (EFD30)
Q_1	1	Power MOSFET	IPA50R250	550 V	TO220	Infineon	IPA50R250CP
D_1	1	Boost diode	MUR550	5 A, 520 V	Axial	ON Semiconductor	MUR550APFG
D_2	1	Bypass diode	1N5406	3 A, 600 V	Axial	ON Semiconductor	1N5406G
DZ_2	1	33 V ZENER diode	MMSZ33T2	33 V, 0.5 W	SOD-123	ON Semiconductor	MMSZ33T2
Rth_1	1	Inrush Current Limiter	15 Ω	1.8 Amax	through-hole	EPCOS	B57153S0150M000
D_3, D_4	2	Switching diode	D1N4148	100 V	SOD123	Vishay	1N4148W-V
R_1, R_2	2	X2 Capacitors discharge resistor	1 MΩ	1%, 500V	SMD, 1206	various	various
R_3	1	Current sense resistor	80 mΩ	1%, 3 W	through-hole	Vishay	LVR03R0800FE12
R_4	1	resistor	10 kΩ	10%, 1/4 W	SMD, 1206	various	various
R_5	1	resistor	2.2 Ω	10%, 1/4 W	SMD, 1206	various	various
R_6	1	resistor	22 Ω	10%, 1/4 W	SMD, 1206	various	various
R7	1	resistor	0 Ω	1%, 1/4 W	SMD, 1206	various	various
R9, R10, R23, R24, R25	5	resistor	1.8 MΩ	1%, 1/4 W	SMD, 1206	various	various
R8, R22	2	SMD resistor, 1206, 1/4 W	560 kΩ	1%, 1/4 W	SMD, 1206	various	various

Reference	Qty	Description	Value	Tolerance / Constraints	Footprint	Manufacturer	Part number
R11	1	resistor	27 kΩ	1%, 1/4 W	SMD, 1206	various	various
R12	1	resistor	22 kΩ	1%, 1/4 W	SMD, 1206	various	various
R14	1	resistor	270 kΩ	1%, 1/4 W	SMD, 1206	various	various
R13, R15, R16, R17, R26	5	resistor	120 kΩ	10%, 1/4 W	SMD, 1206	various	various
R18	1	resistor	27 Ω	10%, 1/4 W	SMD, 1206	various	various
R20, R21	2	resistor	4.7 kΩ	5%, 1/4 W	SMD, 1206	various	various
C8	1	Capacitor	1 nF	25 V, 10%	SMD, 1206	various	various
C9	1	Capacitor	2.2 μF	25 V, 10%	SMD, 1206	various	various
C10, C11, C15	3	Capacitor	220 nF	25 V, 10%	SMD, 1206	various	various
C16	1	Capacitor	470 pF	25 V, 10%	SMD, 1206	various	various
C13	1	Capacitor	10 nF	100 V, 10%	SMD, 1206	various	various
D5, D6	2	Switching diode	D1N4148	100 V	SOD123	Vishay	1N4148W-V
DZ1	1	22 V zener diode	MMSZ22T1	22 V, 0.5 W	SOD-123	ON Semiconductor	MMSZ22T1
U2	1	PFC Controller	NCP1612		SOIC-8	ON Semiconductor	NCP1612B

NOTE: Applications require the use of Y1 capacitors. In this case, CD12-E2GA102MYNSA from TDK or DE1E3KX102MA5B01 from muRata may be a good option for C1 and C2.

REFERENCES

[1] Joel Turchi, “5 key steps to design a compact, high-efficiency PFC Stage Using The NCP1612”, Application note AND9065/D, http://www.onsemi.com/pub_link/Collateral/AND9065-D.PDF.

[2] Joel Turchi, “Safety tests on a NCP1612-driven PFC stage”, Application note AND9079/D, http://www.onsemi.com/pub_link/Collateral/AND9079-D.PDF.

[3] NCP1612 Data Sheet, http://www.onsemi.com/pub_link/Collateral/NCP1612-D.PDF

[4] NCP1612 design worksheet, http://www.onsemi.com/pub/Collateral/NCP1612%20DWS.XLS

[5] NCP1612 evaluation board documents, http://www.onsemi.com/PowerSolutions/supportDoc.do?type=boards&rpn=NCP1612

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