

Si5518 Data Short

NetSync™ Low-Phase-Noise Jitter-Attenuating Clock for 5G/eCPRI/SyncE/IEEE 1588

The Si5518 utilizes fifth-generation DSPLL™ and MultiSynth™ technologies and integrates the functions of a low phase noise 5G/eCPRI wireless jitter attenuator supporting JESD204B/C with a SyncE/IEEE 1588 PTP network synchronizer clock into a single IC device.

The Si5518 may also be combined with optional AccuTime™ IEEE 1588 software offering a complete IEEE 1588v2 solution for phase and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that runs on the host processor.

The RFPLL generates high-performance, ultra-low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 18 clock outputs are configurable in any combination of DCLK, SYSREF, or other system clocks. The DSPLLs are fully featured network synchronization phase-locked-loops with adjustable DCO for IEEE 1588 Ethernet fronthaul synchronization.

Applications:

- LTE-A and 5G Remote Radio Units (RRU)
- JESD204B/C clock generation
- IEEE1588 slave clocks (T-TSC), Telecom Boundary Clocks (T-BC)
- IEEE1588 Assisted Partial Timing support clocks (T-BC-A, T-TSC-A), Partial Timing Support (T-BC-P, T-TSC-P)
- IEEE 1588 Grandmaster clocks (T-GM)
- Remote Access Networks (RAN), picocells, small cells
- Remote Radio Heads (RRH), wireless repeaters, mobile fronthaul and backhaul

KEY POINTS

Si5518

- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs with IEEE 1588/ SyncE
- Optional AccuTime™ IEEE 1588 software
- Integer output frequencies up to 3.2 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/ SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Phase Noise:
 - Noise floor –164 dBc/Hz at 491.52 MHz
 - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Low-Power Mode
- Support IEEE1588 with DCO adjustable at 1 ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), G.8262.1 (eEEEC), G.8273.1 (T-GM), and G.8261 (TC12-17)
- 72 QFN 10x10 mm, 6 inputs, 18 outputs
- AccuTime™ IEEE 1588 Software
 - Field tested and proven with compliance reports available
 - Demonstration Platform Support
 - O-RAN compatible
 - IEEE 1588 servo loop and protocol stack software runs on host processor

1. Feature List

- RFPLL (RF DSPLL)
 - Supports JESD204B/C Subclass 0, 1, and 2 Clocking
 - Ultra-low Phase Noise (example at 491.52 MHz carrier):
 - –164 dBc/Hz noise floor
 - –145 dBc/Hz at 800 kHz offset
 - Ultra-low jitter performance:
 - <50 fs typ XO (12 kHz–20 MHz at 491.52 MHz)
 - <45 fs typ VCXO (12 kHz–20 MHz at 491.52 MHz)
 - Selectable jitter attenuation bandwidth: 10 Hz to 4 kHz, 30 Hz to 4 kHz Dual Reference JA
- DSPLL A, DSPLL B
 - Independent network synchronization DSPLLs
 - Supports ITU-T G.8273.2 (T-TSC, T-BC) and ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A)
 - Programmable loop bandwidth: 1 mHz to 4 kHz
 - Automatic Free-Run, Holdover, and Locked modes
 - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
 - Instant lock for 1PPS/PP2S
 - Programmable loop bandwidth 1 mHz to 25 mHz
 - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 18 Programmable Clock Outputs:
 - JESD204B/C DCLK or SYSREF. Up to nine DCLK/SYSREF pairs
 - Integer Q dividers: PP2S/1PPS to 3.2 GHz
 - JESD204B/C SYSREF pulser mode
 - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
 - Output-to-Output Static Delay: ± 10 ns
 - Output-output skew: ± 50 ps
 - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, Slew Rate Limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Zero Delay Mode for all PLLs
- 4/6 clock inputs:
 - Differential: 8 kHz to 1 GHz
 - CMOS: 1 PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I²C or SPI (3 or 4-wire)
- ClockBuilder Pro™ software tool simplifies device configuration
- Package: 72-Lead QFN, 10x10 mm
- Extended temperature range:
 - –40 to +95 °C ambient
 - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications given on this page are for reference only. Please refer to for device performance.

2. Package Outline

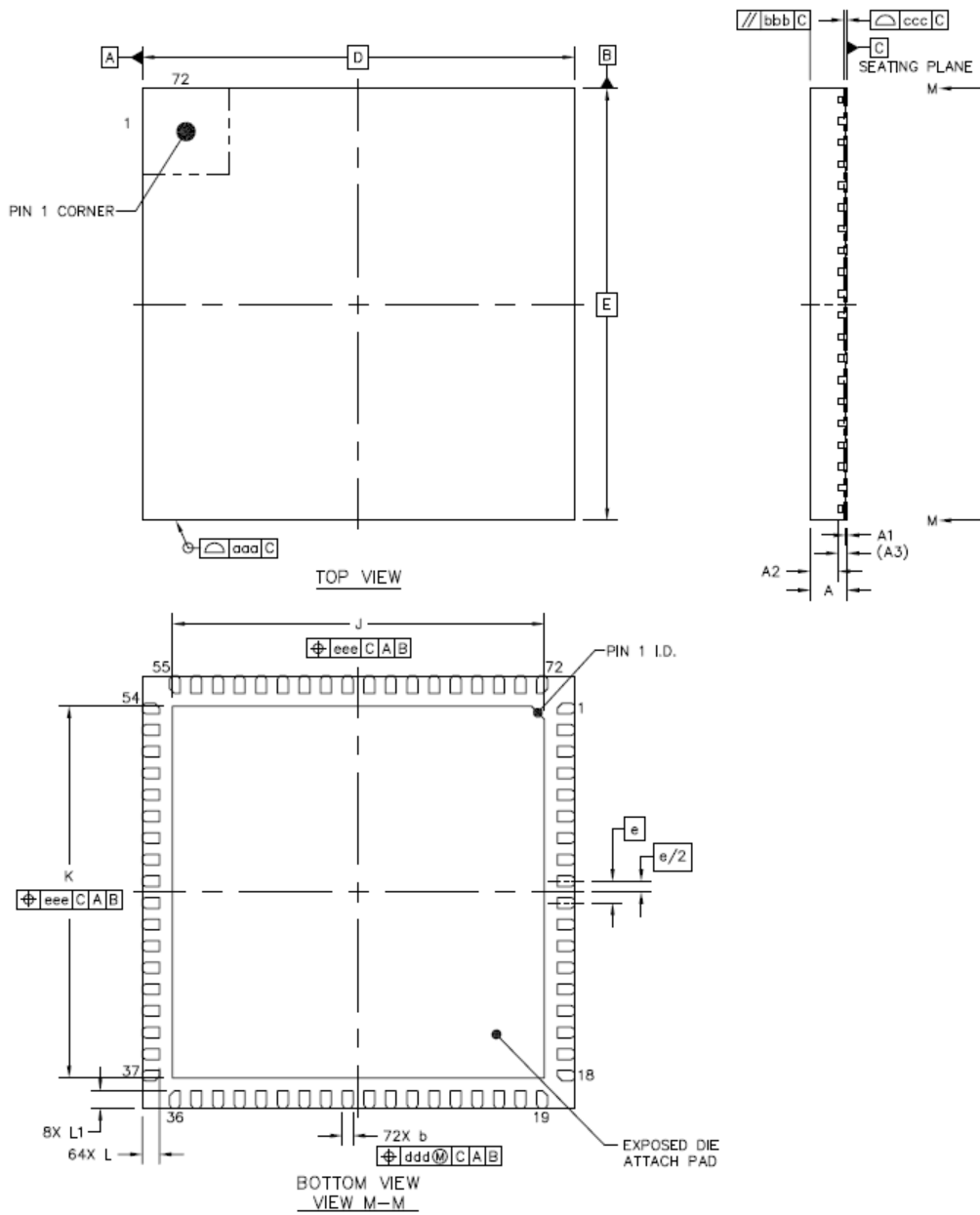


Figure 2.1. 72-QFN Package Diagram

Table 2.1. Package Dimensions

	Symbol	Min	Typ	Max
Total Thickness	A	0.8	0.85	0.9
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	–	0.65	–
L/F Thickness	A3	0.203 REF		
Lead Width	b	0.2	0.25	0.3

		Symbol	Min	Typ	Max
Body Size	X	D	10 BSC		
	Y	E	10 BSC		
Lead Pitch		e	0.5 BSC		
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		
Weight		N/A	—	0.35g	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

3. PCB Land Pattern

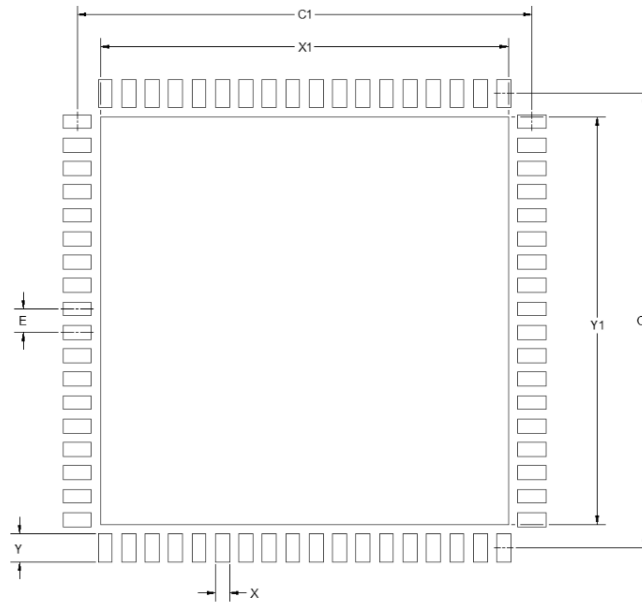


Figure 3.1. PCB Land Pattern

Table 3.1. PCB Land Pattern Dimensions

Dimension	mm
C1	9.70
C2	9.70
E	0.50
X	0.30
Y	0.60
X1	8.70
Y1	8.70

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.*

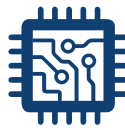


**Connecting Everyone
and Everything,
All the Time**



Portfolio

skyworksinc.com



Quality

skyworksinc.com/quality



Support & Resources

skyworksinc.com/support

Copyright © 2022 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWOKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWOKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5[®], SkyOne[®], SkyBlue[™], Skyworks Green[™], ClockBuilder[®], DSPLL[®], ISOmodem[®], ProSLIC[®], and SiPHY[®] are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com

USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540