

# C1206C222K1GECAUTO

ESD SMD Auto C0G, Ceramic, 2200 pF, 10%, 100 VDC, C0G, SMD, MLCC, Temperature Stable, Electro Static Discharge, Automotive Grade, 1206



Click [here](#) for the 3D model.

## Dimensions

Chip Size 1206

L 3.2mm +/-0.2mm

W 1.6mm +/-0.2mm

T 1.1mm +/-0.10mm

### Dimensions

B 0.5mm +/-0.25mm

### Packaging Specifications

Packaging T&R, 180mm, Plastic Tape

Packaging Quantity 2500

### General Information

Series ESD SMD Auto C0G  
Style SMD Chip  
Description SMD, MLCC, Temperature Stable, Electro Static Discharge, Automotive Grade  
Features Temperature Stable, Automotive Grade  
RoHS Yes  
Termination Tin  
Marking No  
Qualifications AEC-Q200  
AEC-Q200 Yes  
Component Weight 25 mg  
Shelf Life 78 Weeks  
MSL 1

### Specifications

Capacitance 2200 pF  
Measurement Condition 1 kHz 1.0Vrms  
Capacitance Tolerance 10%  
Voltage DC 100 VDC  
ESD Level per AEC-Q200 16,000 V ESD Level  
Dielectric Withstanding Voltage 250 VDC  
Temperature Range -55/+125°C  
Temperature Coefficient C0G  
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC) 30 ppm/C, 1kHz 1.0Vrms  
Dissipation Factor 0.1% 1 kHz 1.0Vrms  
Aging Rate 0% Loss/Decade Hour  
Insulation Resistance 100 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

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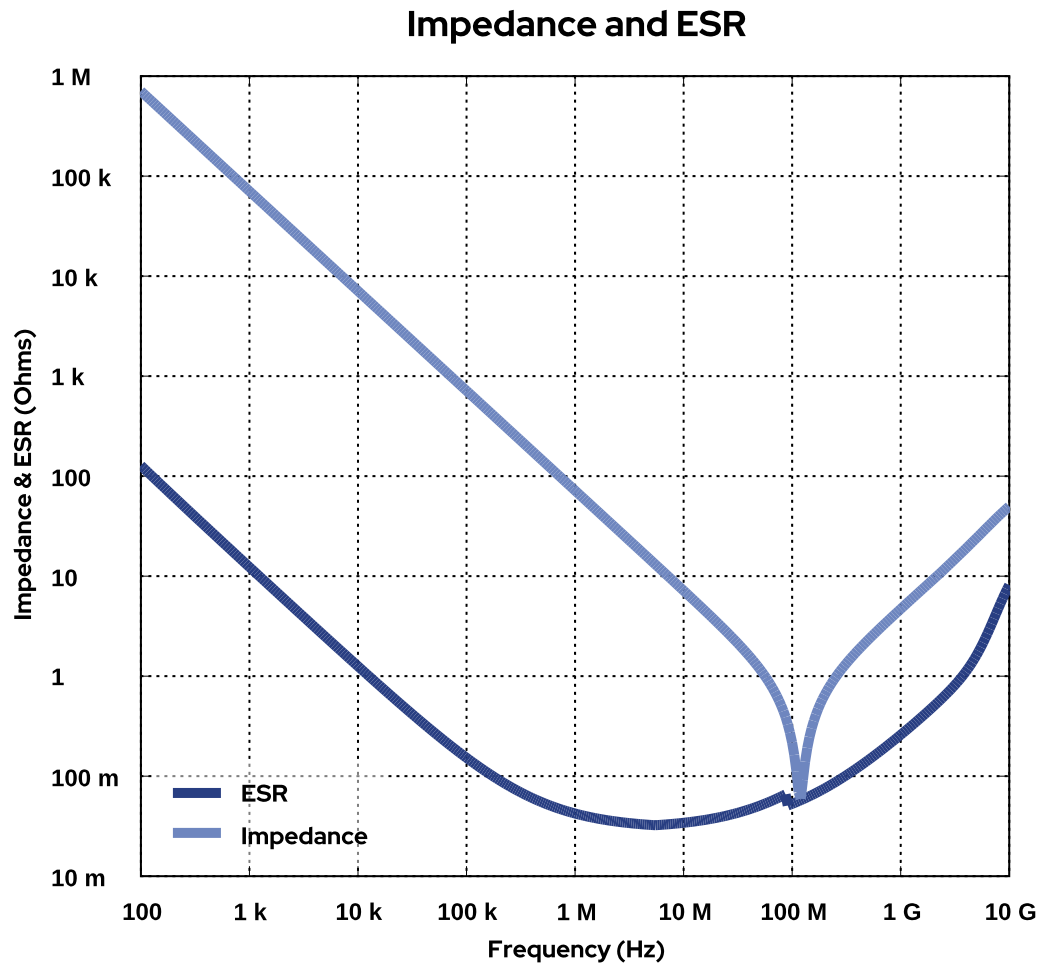
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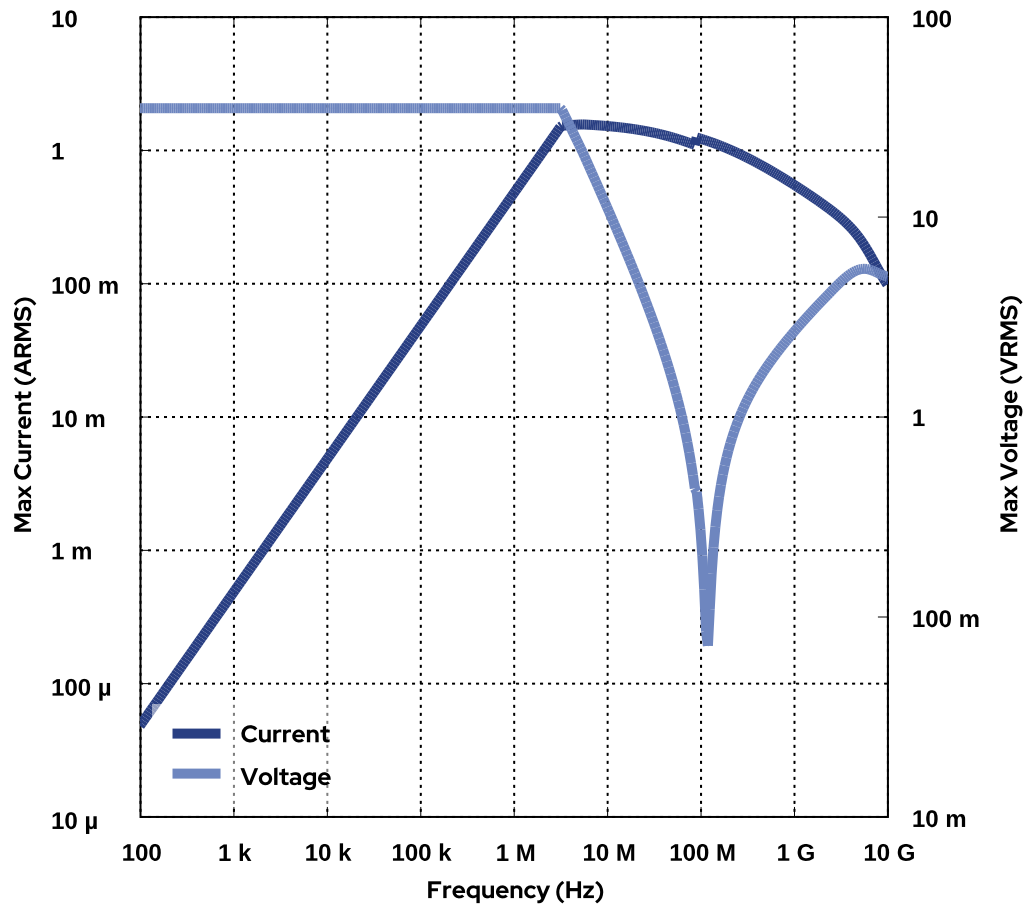
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# Simulations

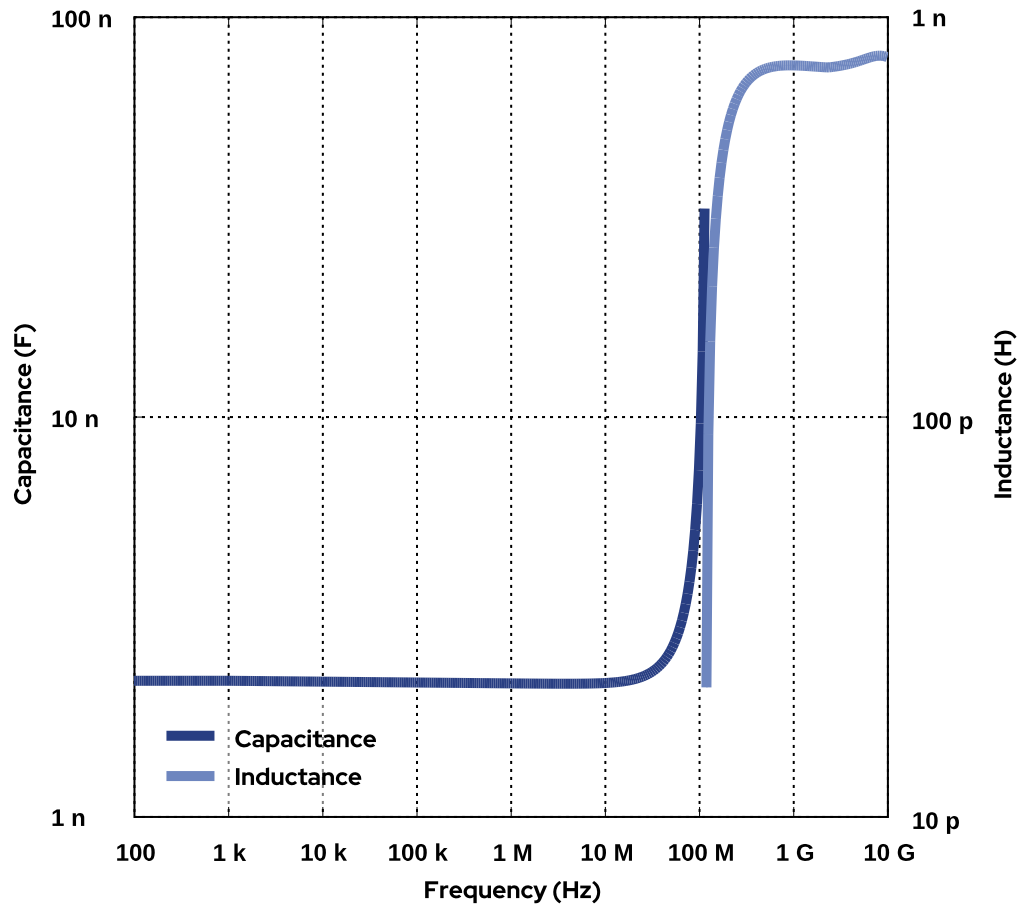
For the complete simulation environment please visit [K-SIM](#).



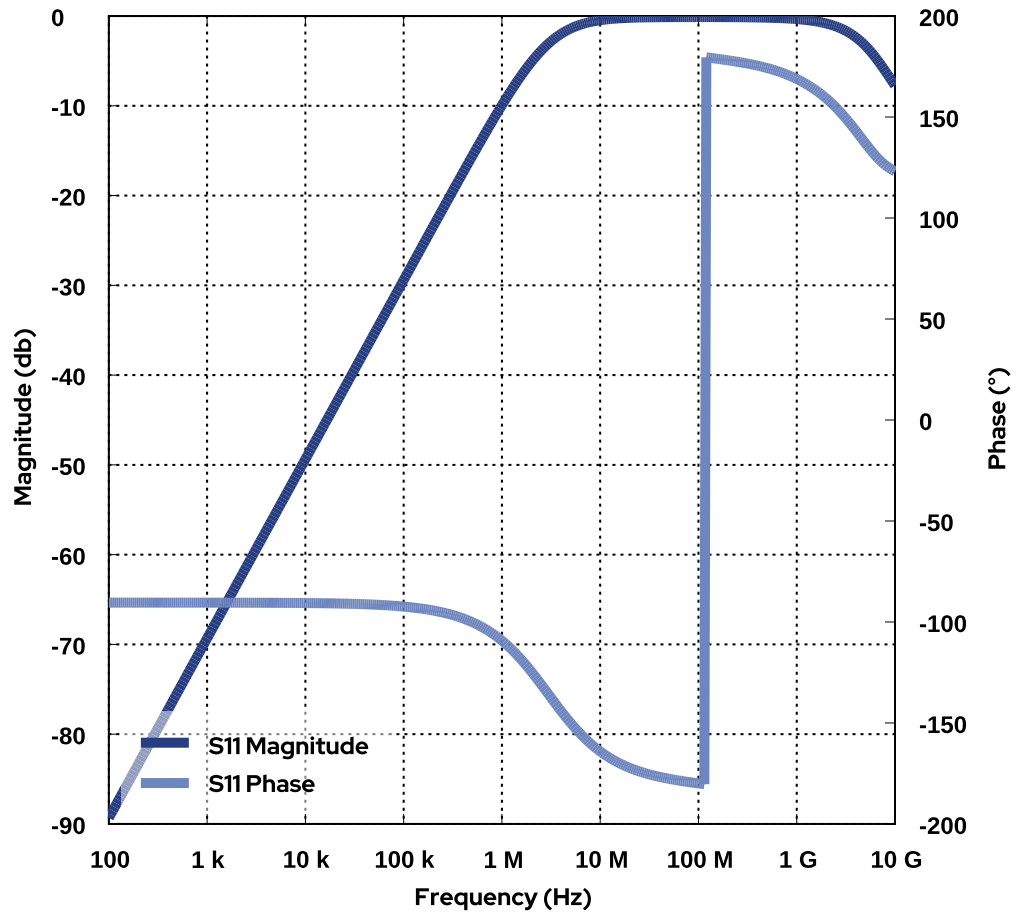
# Current and Voltage

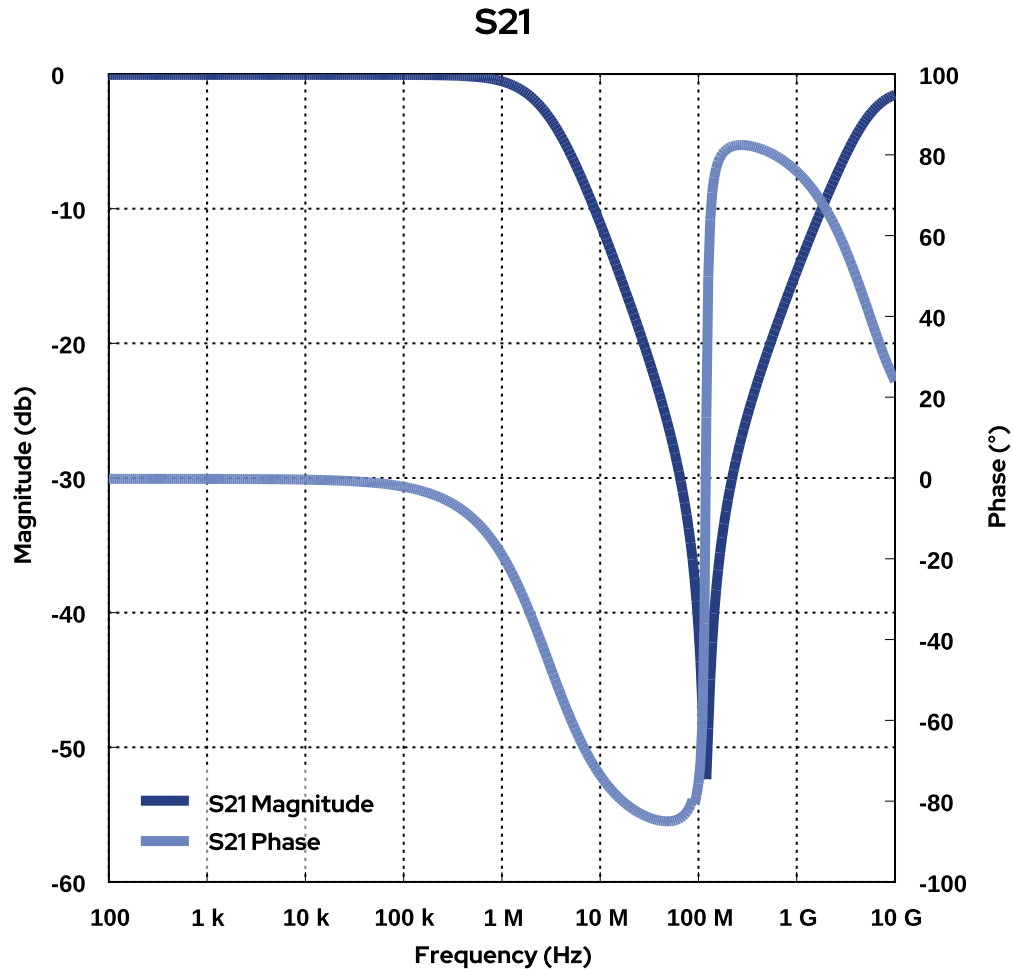


# Capacitance and Inductance



# S11





**These are simulations.**

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple “Ripple Current/Voltage vs. Frequency” plots is the ESR at ambient temperature.
- The ESR in the “Temperature Rise vs. Ripple Current” plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the “Temperature Rise vs. Combined Ripple Currents” plot are

- calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the “Information”) are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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