HV2070

No High-Voltage Bias, 32-Channel, High-Voltage Analog Switch with L-Switch Architecture

Features

- 32-Channel High-Voltage Analog Switch
- No High-Voltage Bias Required
- ±100V Analog Signal Voltage Range
- L-Switch™ Architecture
- Ultra-Low Switch on Resistance - 4.5Ω, typ.
- Low Parasitic Capacitance
- 32-Channel Single-Pole-Single-Throw (SPST) Individual Switching or Bank Switching
- Standby Mode for Low Power Dissipation
- 3.3V CMOS Input Logic Level
- 66 MHz Data Shift Clock Frequency
- Silicon-on-Insulator (SOI) HVCMOS Technology for High Performance
- DC to 100 MHz Analog Small-Signal Frequency
- 100 kHz to 50 MHz Large-Signal Frequency
- Cascadable Serial Data Register with Latches

Application

- Medical Ultrasound Imaging
- NDT Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

HV2070 is an L-Switch™ architecture, low harmonic distortion, low charge injection, 32-channel, high-voltage analog switch without high-voltage bias. It is intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

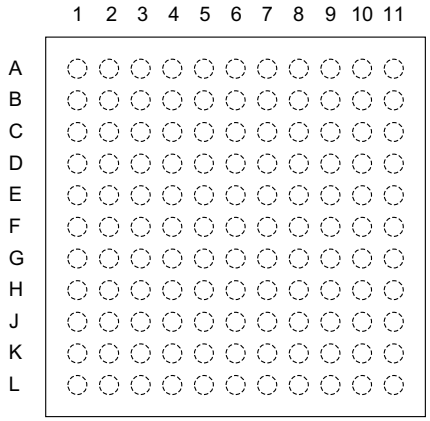
Using the L-Switch™ architecture, the switch on-resistance and parasitic capacitance of the high-voltage switches are greatly reduced. The typical on resistance is 4.5Ω and switch-to-ground on/off capacitances are 20 pF and 11 pF, respectively. The low parasitic capacitance and low on-resistance make HV2070 ideal for applications such as shear wave elastography and High Intensity Focused Ultrasound (HIFU), which require high power dissipation.

The HV2070 has two modes of operation determined by the MODE pin logic input. MODE input high enables individual switching mode of 32-channel SPST switches and MODE input low enables bank switching mode of 16-Pole-Double-Throw (16PDT) switches to support bank switching for probe selection.

The device requires only ±6V or ±5V low-voltage supplies and no high-voltage supplies such as ±100V. However, all of the analog switches can transmit ±100V high-voltage pulses.

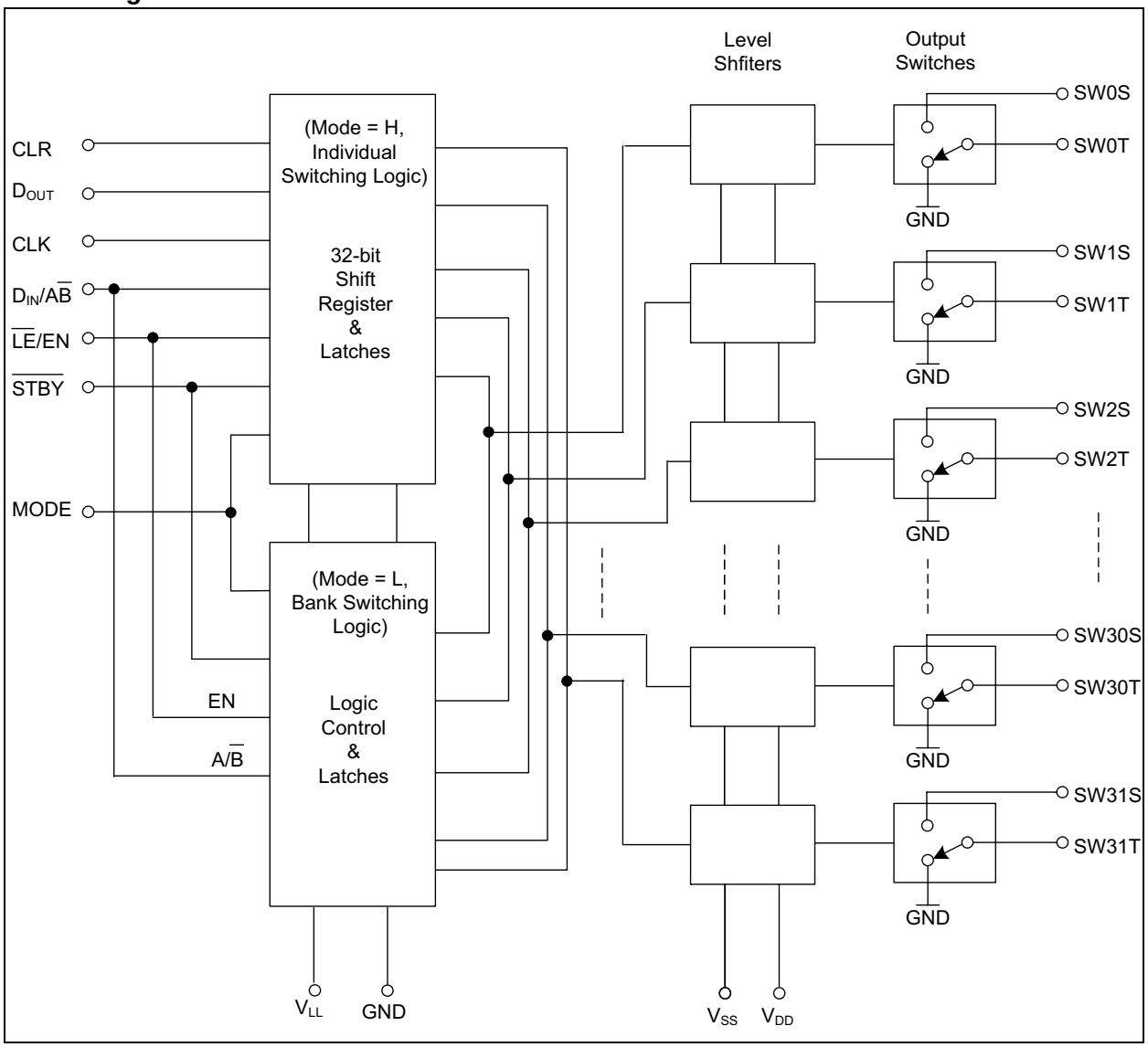
Package Type

10 x10 x 1.1 mm TFBGA (Top View*)



See Table 2-1 for pin information.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Logic Supply Voltage (V_{LL})..... –0.5V to +6.6V
Positive Supply Voltage (V_{DD})..... –0.5V to +6.6V
Negative Supply Voltage (V_{SS}) ..... +0.5V to –6.6V
Logic Input Voltage (V_{IN})..... –0.5V to V_{LL} +0.3V
DGND to GND ..... –0.3V to +0.3V
Analog Signal Range (V_{SIG})..... –110V to +110V
Peak Analog Signal Current/Channel (I_{PK})..... +3.7A

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	3.6	V	
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
Negative Supply Voltage	V_{SS}	–6.3	—	–4.5	V	
High-Level Input Voltage	V_{IH}	$0.9V_{LL}$	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	$0.1V_{LL}$	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	–100	—	100	V	

Note 1: Power up sequence is V_{SS}, V_{DD} and then V_{LL}. Power down sequence is reverse of power-up.
2: V_{SIG} must be $V_{SS} \le V_{SIG} \le V_{DD}$ or floating during power-up/down transition.
3: Rise and fall times of power supplies, V_{LL}, V_{DD} and V_{SS} should be greater than 1 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 6V, V_{SS} = –6V, V_{LL} = 3.3V, T_A = 25°C, **Boldface** specifications apply over the full operating temperature range of T_A = 0°C to 70°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Small Signal Switch ON-Resistance	R_{ONS}	—	4.5	**8**	Ω	I_{SIG} = 5 mA
		—	4.7	—	Ω	V_{DD} = +5V, V_{SS} = –5V I_{SIG} = 5 mA (**Note 1**)
		—	4.5	**8**	Ω	I_{SIG} = 200 mA
Small Signal Switch ON-Resistance Matching	ΔR_{ONS}	—	5	**20**	%	I_{SIG} = 5 mA
Large Signal Switch ON-Resistance	R_{ONL}	—	4	—	Ω	V_{SIG} = 90V 1 µs pulse (**Note 1**)
Switch Off SWT Shunt Resistance	R_{ST}	—	7	**12**	Ω	I_{RST} = 100 mA
Switch Off Bias per SWS	I_{SOB}	—	—	**10**	µA	V_{SIG} = +100V 400 µs pulse. See Figure 3-1
		—	—	**4**	mA	V_{SIG} = –100V 12s pulse. See Figure 3-1

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

Unless otherwise specified, V_{DD} = 6V, V_{SS} = –6V, V_{LL} = 3.3V, T_A = 25°C, **Boldface** specifications apply over the full operating temperature range of T_A = 0°C to 70°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Offset Switch OFF	V_{OS}	—	1	**10**	mV	R_{LOAD} = 25 kΩ See Figure 3-2
DC Offset Switch ON		—	1	**10**		
Quiescent V_{DD} Supply Current	I_{DDQ}	—	1	**5**	mA	All switches off.
Quiescent V_{SS} Supply Current	I_{SSQ}	—	0.5	**4**	mA	
Quiescent V_{DD} Supply Current	I_{DDQ}	—	1	**5**	mA	All switches on V_{SW} = 1V.
Quiescent V_{SS} Supply Current	I_{SSQ}	—	1.2	**5**	mA	
Quiescent V_{LL} Supply Current	I_{LLQ}	—	0.3	**10**	µA	All logic inputs are static.
Standby V_{DD} Supply Current	I_{DDS}	—	50	**100**	µA	$\overline{STBY}$ = 0V
Standby V_{SS} Supply Current	I_{SSS}	—	13	**100**	µA	$\overline{STBY}$ = 0V
Standby V_{LL} Supply Current	I_{LLS}	—	—	**2**	uA	$\overline{STBY}$ = 0V
Switch Output Peak Current	I_{SW}	**2.5**	3.7	—	A	V_{SIG} duty cycle < 0.1% (**Note 1**)
Output Switching Frequency	f_{SW}	—	—	**50**	kHz	Duty cycle = 50% (**Note 1**)
Average V_{DD} Supply Current	I_{DD}	—	7.5	**20**	mA	All output switches are turning ON and OFF at 50 kHz with no load V_{SIG} = 0V
Average V_{SS} Supply Current	I_{SS}	—	6.1	**16**	mA	
Average V_{LL} Supply Current	I_{LL}	—	1.4	**6**	mA	f_{CLK} = 5.0 MHz
Data Out Source Current	I_{SOR}	**10**	—	—	mA	V_{OUT} = V_{LL} - 0.7V
Data Out Sink Current	I_{SINK}	**10**	—	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	8	—	pF	Note 2

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = 6V, V_{SS} = –6V, V_{LL} = 3.3V, T_{AMB} = 25°C, **Boldface** specifications apply over the full operating temperature range of T_A = 0°C to 70°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Setup Time Before LE Rises	t_{SD}	**25**	—	—	ns	Note 1
Time Width of $\overline{LE}$	t_{WLE}	**12**	—	—	ns	Note 1
Clock Delay Time to Data Out	t_{DO}	—	—	**13.5**	ns	
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	Note 1
Setup Time Data to Clock	t_{SU}	**1.5**	—	—	ns	Note 1
Hold Time Data from Clock	t_H	**1.5**	—	—	ns	Note 1
Clock Frequency	f_{CLK}	—	—	**66**	MHz	50% duty cycle f_{DIN} = (1/2) * f_{CLK} C_{DOUT} = 20 pF, (**Note 1**)
Clock Rise and Fall Times	t_R, t_F	—	—	**50**	ns	
Turn ON Time	t_{ON}	—	—	**5**	µs	V_{SIG} = 5V R_{LOAD} = 550Ω. See Figure 3-3
Turn OFF Time	t_{OFF}	—	—	**5**	µs	
Input Large Signal Pulse Width	t_{PW}	—	—	**2.5**	µs	V_{PULSE} = 0V to ± 100V. Measured at 90% amplitude. See Figure 3-4 (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

Unless otherwise specified, V_{DD} = 6V, V_{SS} = –6V, V_{LL} = 3.3V, T_{AMB} = 25°C, **Boldface** specifications apply over the full operating temperature range of T_A = 0°C to 70°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Wake-Up Time from Standby to Digital Logic Normal Operation	t_{WU}	—	—	**10**	µs	Bank switching mode (MODE = L)
		—	—	**10**	µs	Individual switching mode (MODE = H) (**Note 1**)
Maximum V_{SIG} Slew Rate	dV/dt	—	—	20	V/ns	Note 1
Analog Small Signal Frequency	f_{BWS}	—	100	—	MHz	Note 1
OFF Isolation SWS to SWT	K_O	—	–56	–51	dB	f = 5.0 MHz,1.0 kΩ//15 pF load. See Figure 3-5 (**Note 1**)
		—	–66	–61		f = 5.0 MHz, 50Ω load. See Figure 3-5 (**Note 1**)
OFF Isolation SWT to SWS		—	–56	–51	dB	f = 5.0 MHz,1.0kΩ//15 pF load. See Figure 3-6 (**Note 1**)
		—	–58	–53		f = 5.0 MHz, 50Ω load. See Figure 3-6 (**Note 1**)
Switch Crosstalk	K_{CR}	—	–66	–61	dB	f = 5.0 MHz, 50Ω load. See Figure 3-7 (**Note 1**)
Off-Capacitance SW to GND	$C_{SG(OFF)}$	—	11	—	pF	V_{SIG} = 50 mV@1 MHz, no load (**Note 1**)
On-Capacitance SW to GND	$C_{SG(ON)}$	—	20	—		
Output Voltage Spike at SWS	$+V_{SPK}$	—	—	150	mV	R_{LOAD} = 50Ω. See Figure 3-8 (**Note 1**)
	$–V_{SPK}$	–150	—	—	mV	
Charge Injection	QC	—	310	—	pC	See Figure 3-9 (**Note 1**)
Second Harmonic Distortion	HD2	—	–70	–55	dBc	V_{SIG} = 1.5 V_{PP}@5 MHz, 50Ω load (**Note 1**)
		—	–70	–56	dBc	V_{SIG} = 1.5 V_{PP}@5 MHz, 1 kΩ//15 pF load (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_A	–65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, TFBGA	Θ_{JA}	—	+20	—	°C/W	

TABLE 1-1: TRUTH TABLE

$\overline{\text{STBY}}$	MODE	D0	D1	...	D15	D16	...	D31	Din/$\overline{\text{AB}}$	$\overline{\text{LE}}$/EN	CLR	SW0	SW1	...	SW15	SW16	...	SW31
H	H	L	-		-	-		-	X	L	L	OFF	-		-	-		-
H	H	H	-		-	-		-	X	L	L	ON	-		-	-		-
H	H	-	L		-	-		-	X	L	L	-	OFF		-	-		-
H	H	-	H		-	-		-	X	L	L	-	ON		-	-		-
H	H	-	-		-	-		-	X	L	L	-	-		-	-		-
H	H	-	-		-	-		-	X	L	L	-	-		-	-		-
H	H	-	-		L	-		-	X	L	L	-	-		OFF	-		-
H	H	-	-	...	H	-	...	-	X	L	L	-	-	...	ON	-	...	-
H	H	-	-		-	L		-	X	L	L	-	-		-	OFF		-
H	H	-	-		-	H		-	X	L	L	-	-		-	ON		-
H	H	-	-		-	-		-	X	L	L	-	-		-	-		-
H	H	-	-		-	-		-	X	L	L	-	-		-	-		-
H	H	-	-		-	-		L	X	L	L	-	-		-	-		OFF
H	H	-	-		-	-		H	X	L	L	-	-		-	-		ON
H	H	X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
H	H	X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						
H	L	X	X	X	X	X	X	X	L	H	X	EVEN SWITCHES OFF & ODD SWITCHES ON						
H	L	X	X	X	X	X	X	X	H	H	X	EVEN SWITCHES ON & ODD SWITCHES OFF						
H	L	X	X	X	X	X	X	X	X	L	X	ALL SWITCHES OFF						
L	X	X	X	X	X	X	X	X	X	X	X	ALL SWITCHES OFF, STANBY STATE						

Note 1: The 32 switches operate independently (when MODE = H).

2: Serial data is clocked in on the L to H transition of the CLK (when MODE = H).

3: All 32 switches go to a state retaining their latched condition a the rising edge of $\overline{\text{LE}}$/EN. When $\overline{\text{LE}}$/EN is low, the shift registers data flow through the latch (when MODE = H).

4: DOUT is high when data in register 31 is high (when MODE = H).

5: Shift register clocking has no effect on the switch states if $\overline{\text{LE}}$/EN is high (when MODE = H).

6: The CLR clear input overrides all the inputs (when MODE = H).

Legend: H = High, L = Low, X = Irrelevant

1.1 Typical Timing Diagram

Figure 1-1 shows timing of AC characteristic parameters graphically.

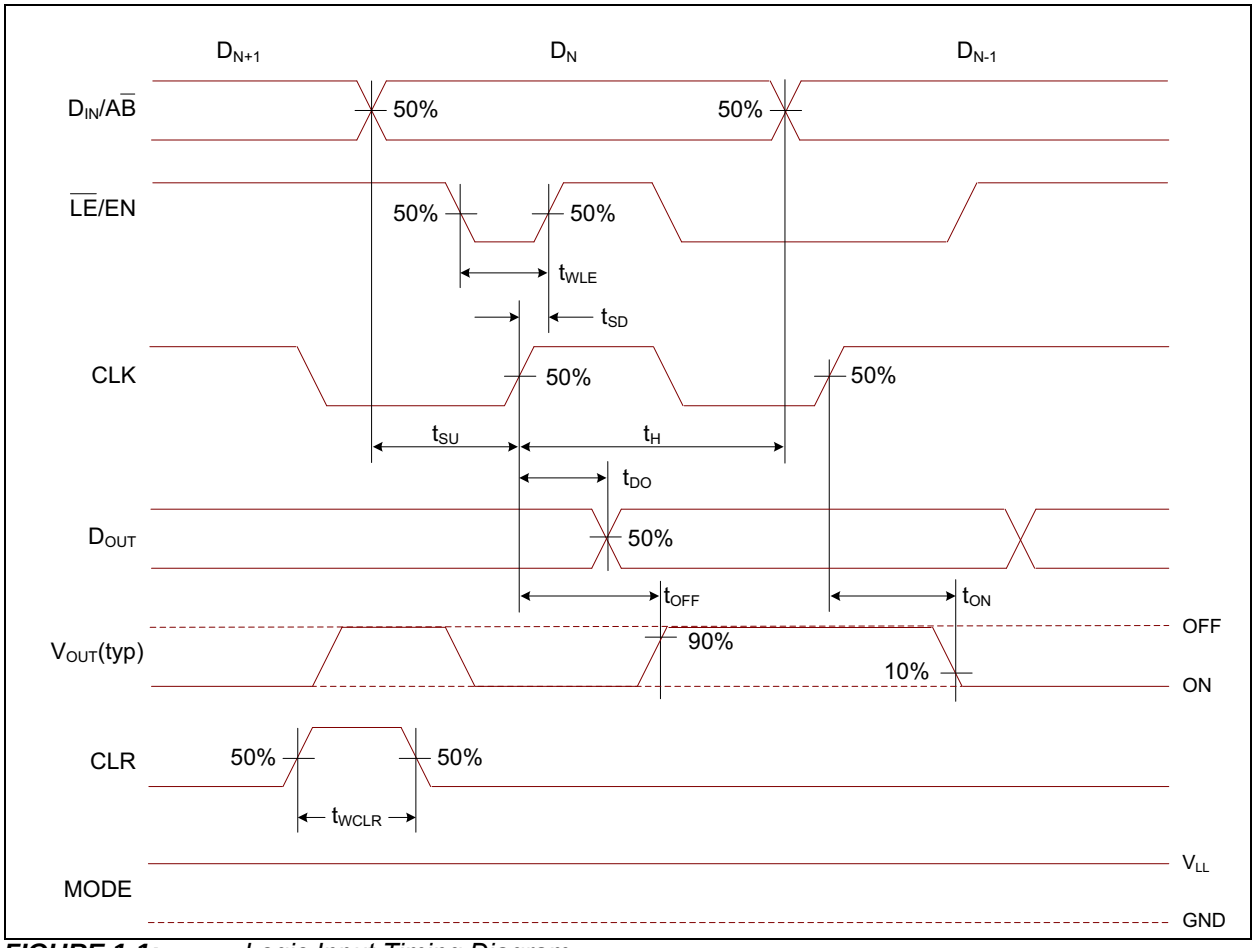


FIGURE 1-1: *Logic Input Timing Diagram.*

NOTES:

2.0 PIN DESCRIPTION

This section details the pin designation for the 121-Ball TFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

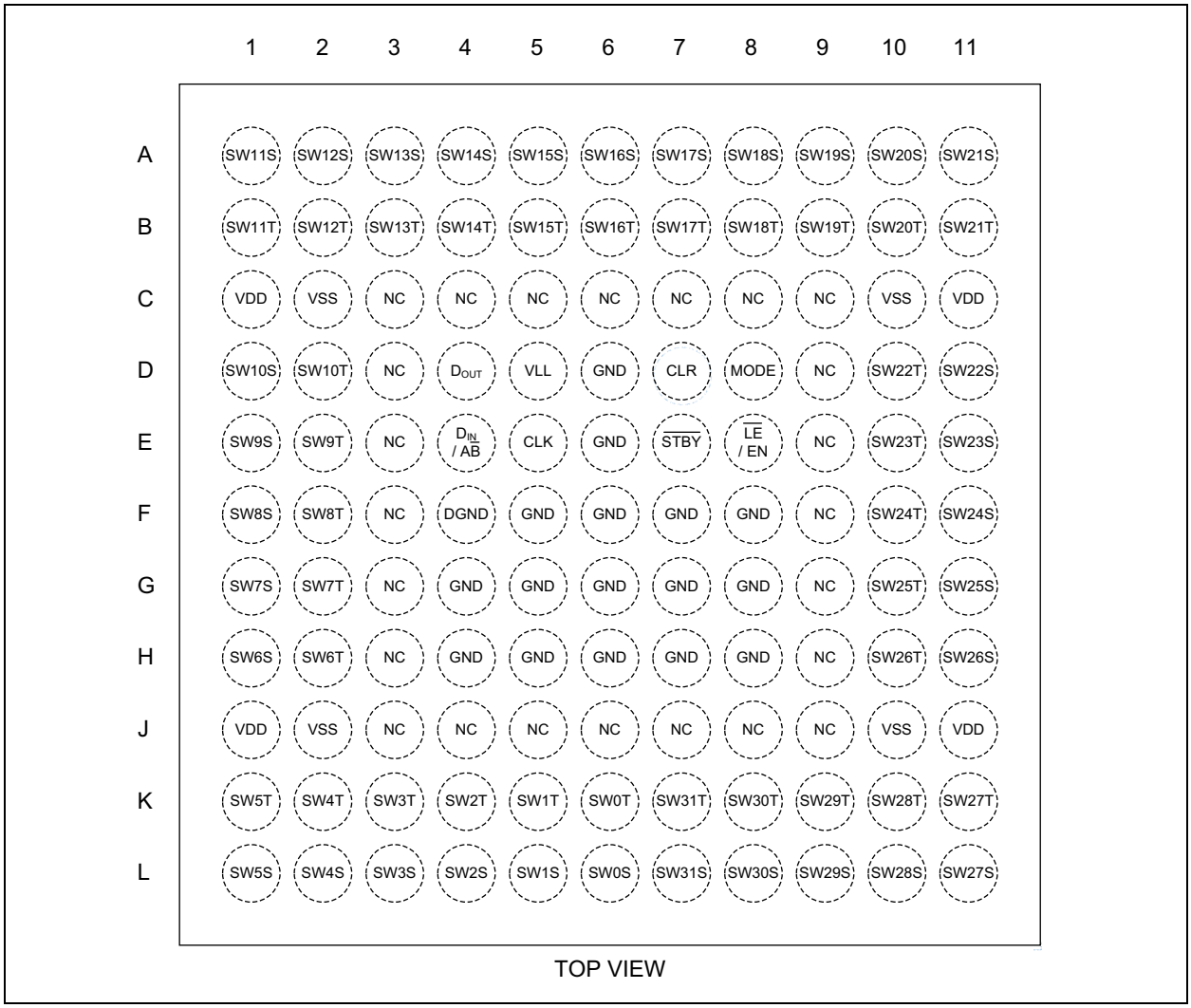


FIGURE 2-1: *121-Ball TFBGA Package - Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
A1	SW11S	Analog switch 11 terminal S
A2	SW12S	Analog switch 12 terminal S
A3	SW13S	Analog switch 13 terminal S
A4	SW14S	Analog switch 14 terminal S
A5	SW15S	Analog switch 15 terminal S
A6	SW16S	Analog switch 16 terminal S
A7	SW17S	Analog switch 17 terminal S
A8	SW18S	Analog switch 18 terminal S
A9	SW19S	Analog switch 19 terminal S
A10	SW20S	Analog switch 20 terminal S
A11	SW21S	Analog switch 21 terminal S

TABLE 2-1: (CONTINUED)PIN FUNCTION TABLE

Pin Number	Symbol	Description
B1	SW11T	Analog switch 11 terminal T
B2	SW12T	Analog switch 12 terminal T
B3	SW13T	Analog switch 13 terminal T
B4	SW14T	Analog switch 14 terminal T
B5	SW15T	Analog switch 15 terminal T
B6	SW16T	Analog switch 16 terminal T
B7	SW17T	Analog switch 17 terminal T
B8	SW18T	Analog switch 18 terminal T
B9	SW19T	Analog switch 19 terminal T
B10	SW20T	Analog switch 20 terminal T
B11	SW21T	Analog switch 21 terminal T
C1	V_{DD}	Positive supply voltage
C2	V_{SS}	Negative supply voltage
C3~C9	NC	No connection
C10	V_{SS}	Negative supply voltage
C11	V_{DD}	Positive supply voltage
D1	SW10S	Analog switch 10 terminal S
D2	SW10T	Analog switch 10 terminal T
D3	NC	No connection
D4	D_{OUT}	Data out logic output
D5	V_{LL}	Logic supply voltage
D6	GND	Ground
D7	CLR	Latch clear logic input
D8	MODE	Logic input to decide the switching mode. L = bank switching, H = Individual switching.
D9	NC	No connection
D10	SW22T	Analog switch 22 terminal T
D11	SW22S	Analog switch 22 terminal S
E1	SW9S	Analog switch 9 terminal S
E2	SW9T	Analog switch 9 terminal T
E3	NC	No connection
E4	$D_{IN}/\overline{AB}$	Data in logic input when individual switching mode, logic input to select EVEN SWs bank or ODD SWs bank when bank switching mode.
E5	CLK	Clock logic input for shift register.
E6	GND	Ground
E7	$\overline{STBY}$	Logic input for standby state, L = Standby mode (default), H = Normal operation.
E8	$\overline{LE}$/EN	Latch enable logic input, low active when individual switching mode. Enable logic input when bank switching mode.
E9	NC	No connection
E10	SW23T	Analog switch 23 terminal T
E11	SW23S	Analog switch 23 terminal S
F1	SW8S	Analog switch 8 terminal S
F2	SW8T	Analog switch 8 terminal T
F3	NC	No connection

TABLE 2-1: (CONTINUED)PIN FUNCTION TABLE

Pin Number	Symbol	Description
F4	DGND	Digital Ground
F5~F8	GND	Ground
F9	NC	No connection
F10	SW24T	Analog switch 24 terminal T
F11	SW24S	Analog switch 24 terminal S
G1	SW7S	Analog switch 7 terminal S
G2	SW7T	Analog switch 7 terminal T
G3	NC	No connection
G4~G8	GND	Ground
G9	NC	No connection
G10	SW25T	Analog switch 25 terminal T
G11	SW25S	Analog switch 25 terminal S
H1	SW6S	Analog switch 6 terminal S
H2	SW6T	Analog switch 6 terminal T
H3	NC	No connection
H4~H8	GND	Ground
H9	NC	No connection
H10	SW26T	Analog switch 26 terminal T
H11	SW26S	Analog switch 26 terminal S
J1	V_{DD}	Positive supply voltage
J2	V_{SS}	Negative supply voltage
J3~9	NC	No connection
J10	V_{SS}	Negative supply voltage
J11	V_{DD}	Positive supply voltage
K1	SW5T	Analog switch 5 terminal T
K2	SW4T	Analog switch 4 terminal T
K3	SW3T	Analog switch 3 terminal T
K4	SW2T	Analog switch 2 terminal T
K5	SW1T	Analog switch 1 terminal T
K6	SW0T	Analog switch 0 terminal T
K7	SW31T	Analog switch 31 terminal T
K8	SW30T	Analog switch 30 terminal T
K9	SW29T	Analog switch 29 terminal T
K10	SW28T	Analog switch 28 terminal T
K11	SW27T	Analog switch 27 terminal T
L1	SW5S	Analog switch 5 terminal S
L2	SW4S	Analog switch 4 terminal S
L3	SW3S	Analog switch 3 terminal S
L4	SW2S	Analog switch 2 terminal S
L5	SW1S	Analog switch 1 terminal S
L6	SW0S	Analog switch 0 terminal S
L7	SW31S	Analog switch 31 terminal S
L8	SW30S	Analog switch 30 terminal S
L9	SW29S	Analog switch 29 terminal S

TABLE 2-1: (CONTINUED)PIN FUNCTION TABLE

Pin Number	Symbol	Description
L10	SW28S	Analog switch 28 terminal S
L11	SW27S	Analog switch 27 terminal S

3.0 TEST CIRCUIT EXAMPLES

This section details a few example of test circuits.

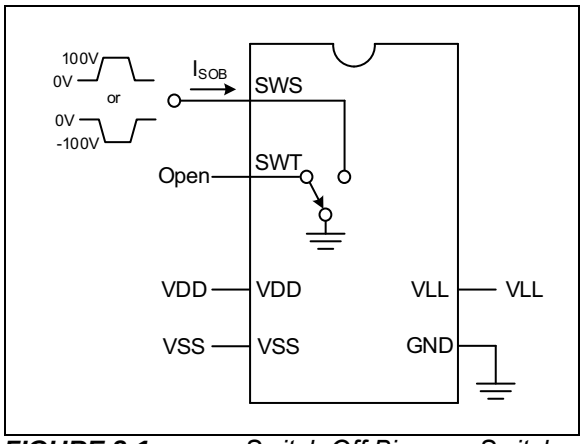


FIGURE 3-1: *Switch Off Bias per Switch.*

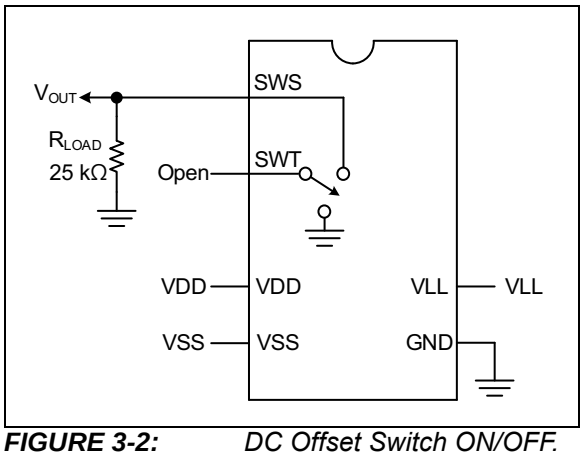


FIGURE 3-2: *DC Offset Switch ON/OFF.*

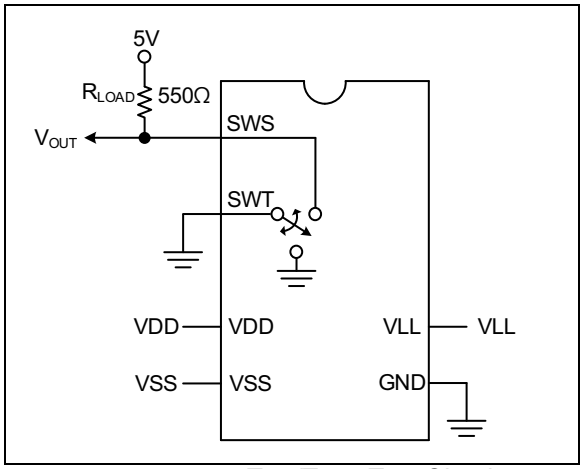


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

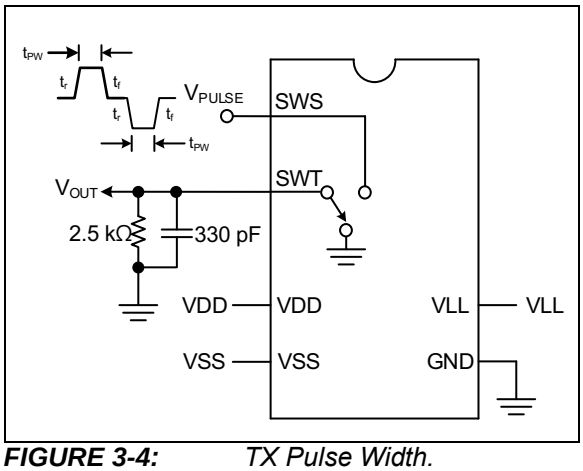


FIGURE 3-4: *TX Pulse Width.*

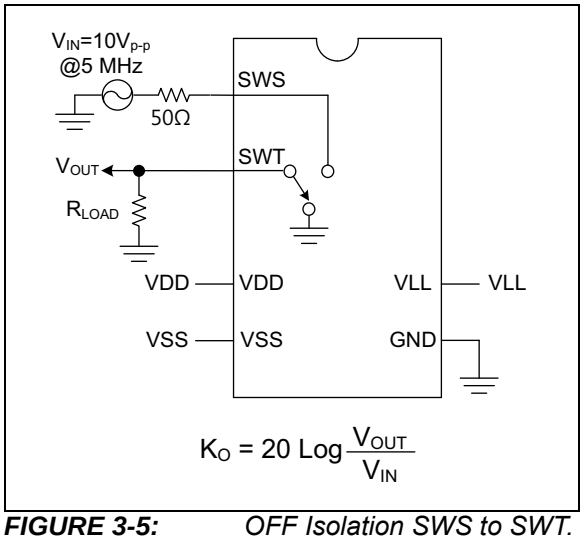


FIGURE 3-5: *OFF Isolation SWS to SWT.*

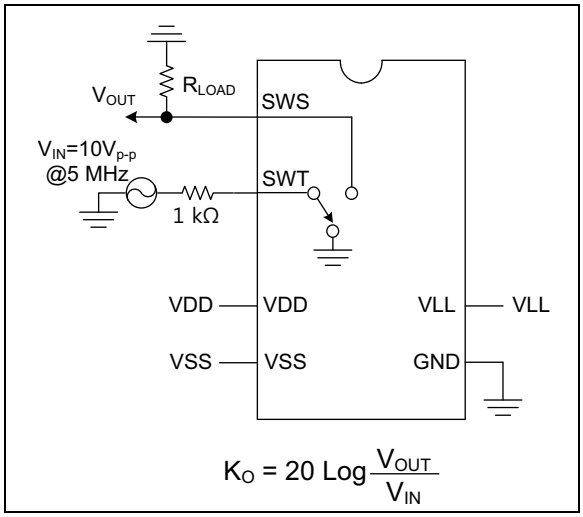


FIGURE 3-6: *Off Isolation SWT to SWS.*

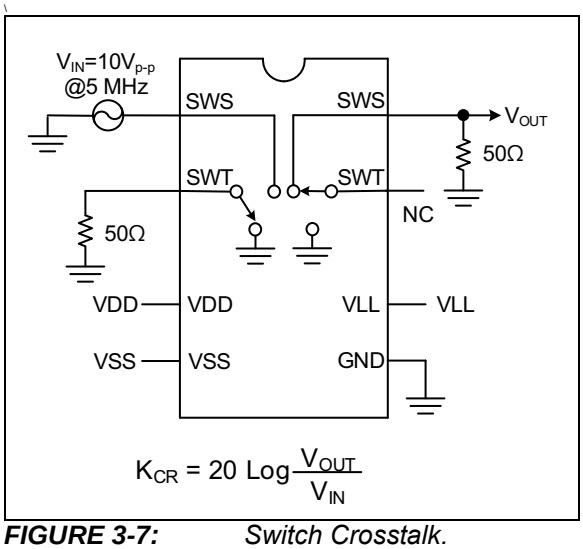


FIGURE 3-7: *Switch Crosstalk.*

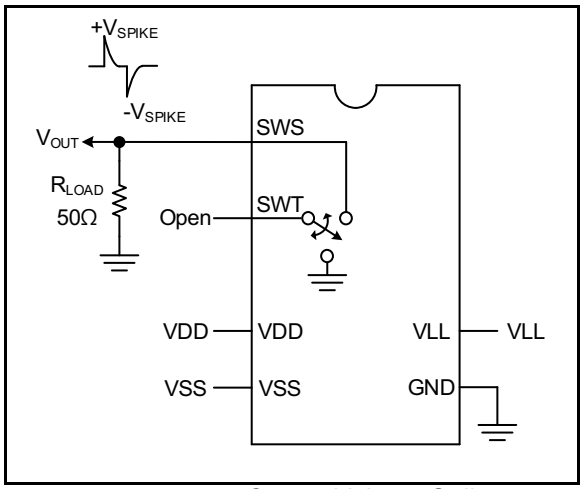


FIGURE 3-8: *Output Voltage Spike.*

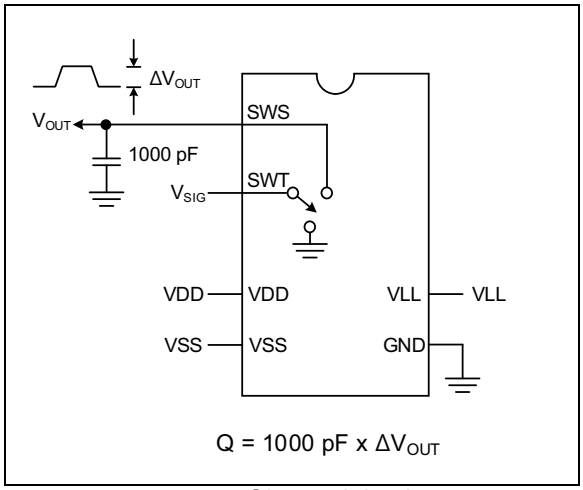


FIGURE 3-9: *Charge Injection.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

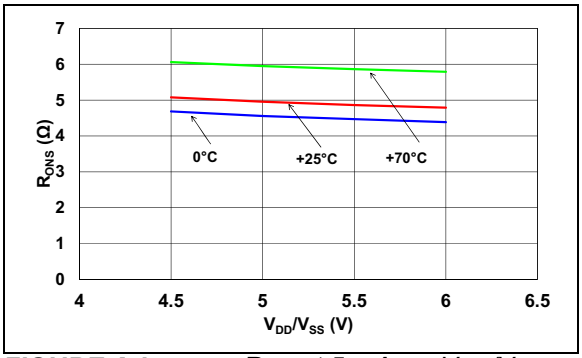


FIGURE 4-1: *Ron at 5 mA vs. V_{DD}/V_{SS}.*

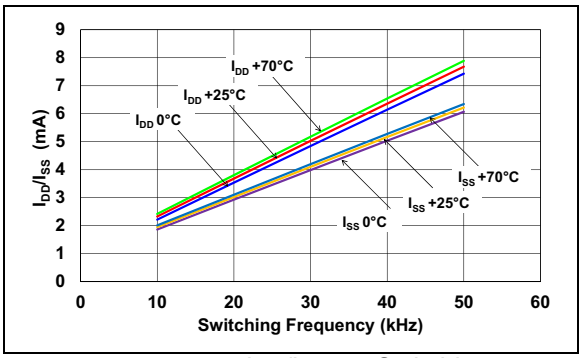


FIGURE 4-2: *I_{DD}/I_{SS} vs. Switching Frequency.*

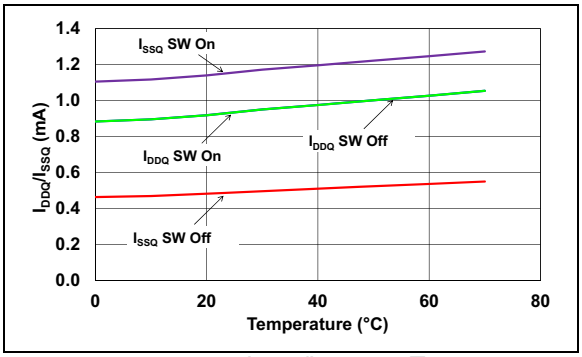


FIGURE 4-3: *I_{DDQ}/I_{SSQ} vs. Temperature.*

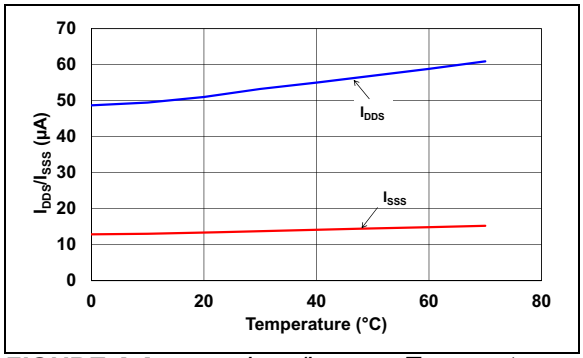


FIGURE 4-4: *I_{DDS}/I_{SSS} vs. Temperature.*

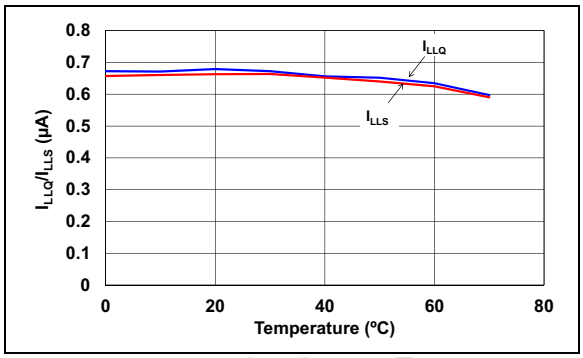


FIGURE 4-5: *I_{LLQ}/I_{LLS} vs. Temperature.*

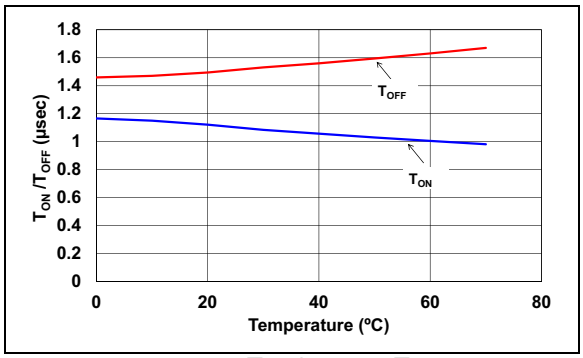


FIGURE 4-6: *$T_{ON/OFF}$ vs. Temperature.*

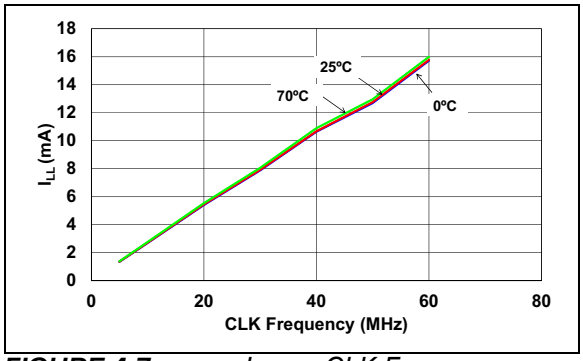


FIGURE 4-7: *I_{LL} vs. CLK Frequency.*

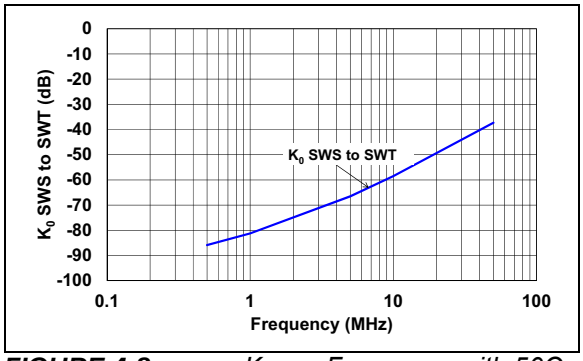


FIGURE 4-8: *Ko vs. Frequency with 50Ω Load.*

5.0 DEVICE DESCRIPTION

5.1 Overview

The HV2070 is an L-Switch™ architecture, low harmonic distortion, low charge injection, 32-channel, high-voltage analog switch that does not require high-voltage supplies.

The device requires only ±6V or ±5V low-voltage supplies and no high-voltage supplies. However, all of the analog switches can transmit ±100V high-voltage pulses with typical 4.5Ω on-resistance and 100 MHz bandwidth for small signals. The low on-resistance makes HV2070 ideal for applications such as shear wave elastography and HIFU that require high power dissipation.

The device has two digital logics and controls for two switch control modes which are individual switching mode and bank switching mode.

Figure 5-1 shows a typical medical ultrasound image system consisting of 64 channels of transmit pulsers, 64 channels of receivers (LNA and ADC), and 64 channels of T/R switches connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

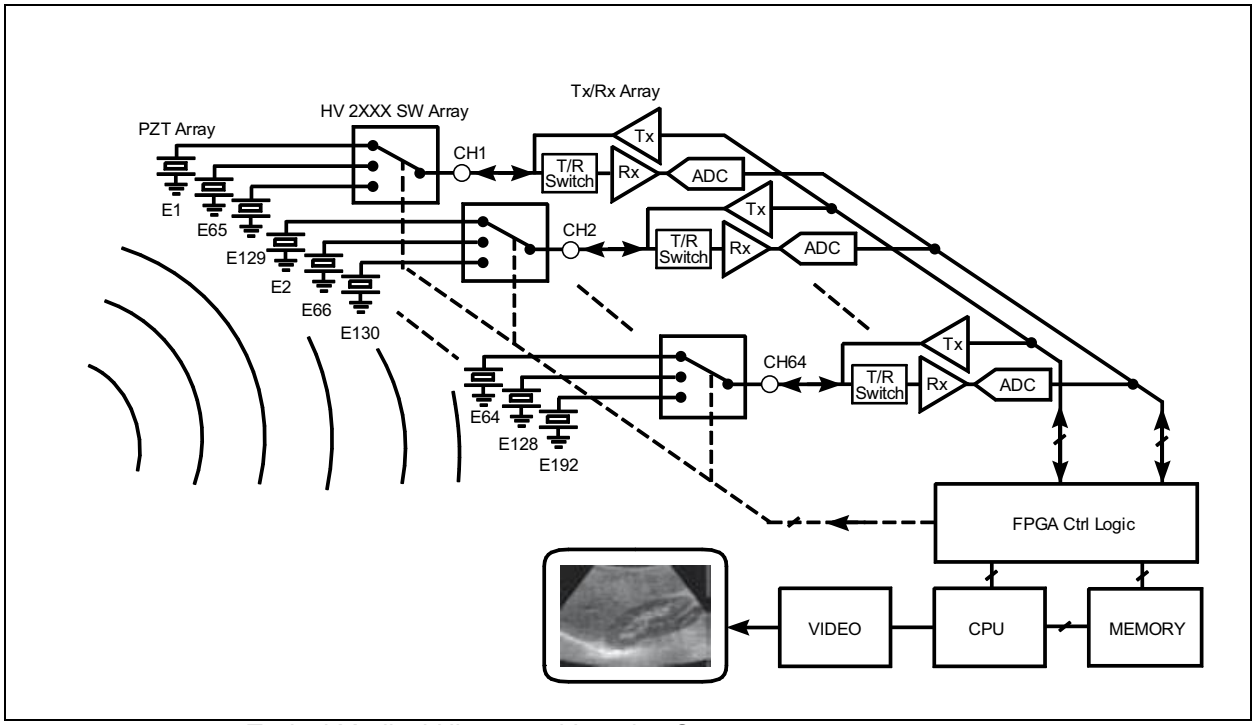


FIGURE 5-1: *Typical Medical Ultrasound Imaging System.*

5.2 Individual Switching Mode and Bank Switching Mode

The HV2070 has two logic circuitries to support two switching modes determined by MODE pin logic input. One mode is individual switching mode, and the other mode is bank switching mode. When MODE pin is High, the device operates in individual switching mode and can control 32-channel SPST switches individually through digital serial interface. When MODE pin is Low, the device operates in bank switching mode that works as a 16PDT switch for probe selection. Table 5-1 shows the functional difference of logic pins in the two modes. When MODE input is changed from Low to High, all the shift registers are reset to zero.

TABLE 5-1: LOGIC PINS AT INDIVIDUAL SWITCHING VS BANK SWITCHING

Pin Name	Individual Switching Mode		Bank Switching Mode	
	Function	Description (MODE=H)	Function	Description (MODE=L)
$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	L = Standby mode (default), H = Normal operation	$\overline{\text{STBY}}$	L = Standby mode (default), H = Normal operation

Pin Name	Individual Switching Mode		Bank Switching Mode	
	Function	Description (MODE=H)	Function	Description (MODE=L)
$D_{IN}/A\overline{B}$	D_{IN}	Data in logic input	$A/\overline{B}$	Logic input to select ON bank, H = EVEN SWs ON & ODD SWs OFF, L = EVEN SWs OFF & ODD SWs ON
$\overline{LE}$/EN	$\overline{LE}$	Latch enable logic input	EN	Logic input for enable/disable bank switching, H = Enable, L = Disable (All SWs OFF)
CLR	CLR	Latch clear logic input	GND	Should connect to GND
CLK	CLK	Clock logic input for shift register	GND	Should connect to GND
D_{OUT}	D_{OUT}	Data out logic output	Hi-Z	High impedance

5.3 Individual Switching Mode Logic Input Timing

When the MODE pin logic input is High, the HV2070 operates in the individual switching mode. The HV2070 has a digital serial interface consisting of Data In ($D_{IN}/A\overline{B}$), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$/EN) and Clear (CLR) for the individual switching mode. The digital circuits are supplied by V_{LL}. The serial clock frequency is up to 66 MHz.

The switch state configuration data is shifted into the shift registers on the rising edge (low-to-high transition) of the clock. The Switch Configuration bit of SW31 is shifted in first, and the Configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable Input ($\overline{LE}$/EN) should remain high, while the 32-bit Data In signal is shifted into the 32-bit register. After the valid 32-bit data completes shifting into the shift registers, the high-to-low transition of the $\overline{LE}$/EN signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$/EN high again, allows all the latches to keep the current state while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 32 latches to low. Consequently, all the high-voltage switches are set to an OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

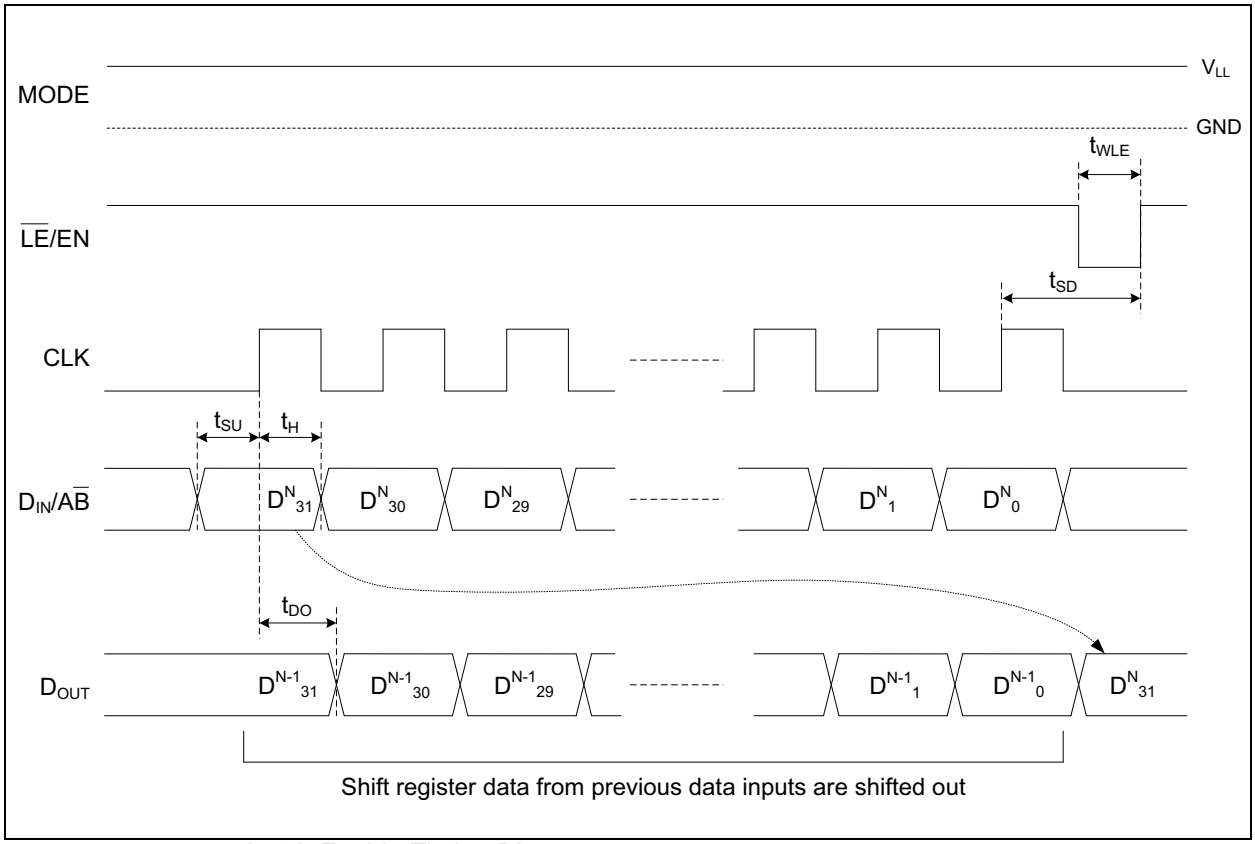


FIGURE 5-2: *Latch Enable Timing Diagram.*

5.4 Multiple Devices Connection in Individual Switching Mode

The serial input interface of the HV2070 allows multiple devices to daisy-chain together. In this configuration, DOUT of a device is connected to the D_{IN}/$\overline{AB}$ of the subsequent device, and so forth. The last DOUT of the daisy-chained HV2070 can be either floating or fed back to an FPGA to check the previously stored shift register data.

To control all the high-voltage analog switch states in daisy-chained N devices, N-times 32 clocks and N-times 32 bits of data are shifted into shift registers, while $\overline{LE}$/EN remains high and CLR remains low. After all the data finishes shifting in, one single negative pulse of $\overline{LE}$/EN transfers the data from all shift registers to all the latches simultaneously. Consequently, all N-times 32 high-voltage analog switches change states simultaneously.

5.5 Bank Switching Mode

When the mode pin logic input is Low, the HV2070 operates in the bank switching mode.

The D_{IN}/$\overline{AB}$ pin is used as A/$\overline{B}$ input and $\overline{LE}$/EN pin is used as EN input in the bank switching mode. The CLR and CLK logic inputs are not used and recommended to drive logic low. The D_{OUT} pin is in a high-impedance state. See Table 1-1 for details on bank switching mode.

The EN function allows the HV2070 to be configured as either a 2:1 or 4:1 multiplexer/demultiplexer. The HV2070 can replace the relay in the medical ultrasound system. Compared to a mechanical relay, the HV2070 is a faster switching, less power consuming and no audible noise emitting switch. Figure 5-3 shows an application example of 4 probe selection configuration using HV2070 bank switching mode. Please note that the MODE pin is connected to GND.

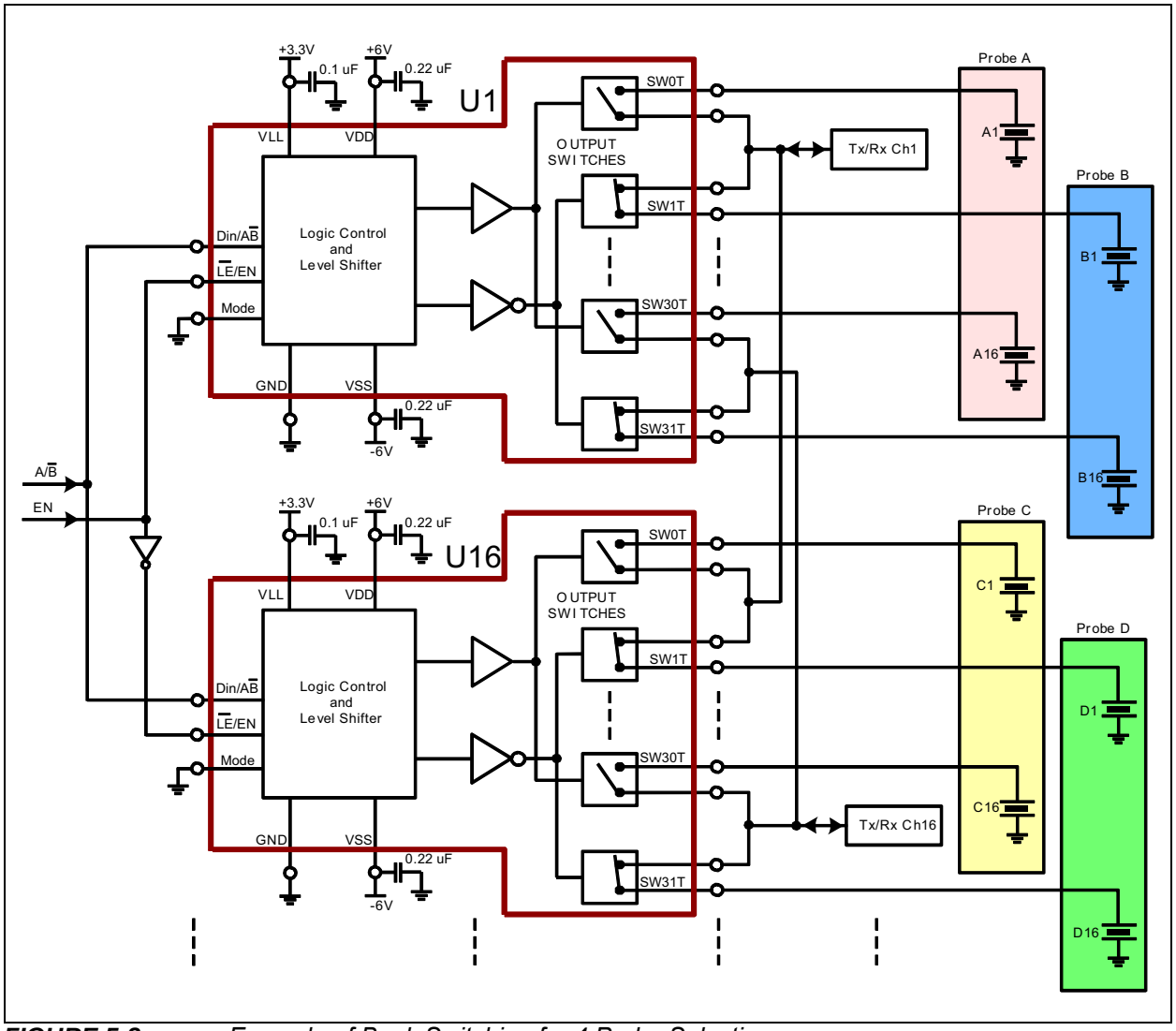


FIGURE 5-3: *Example of Bank Switching for 4 Probe Selection*

5.6 Standby Mode

To reduce the current consumption during the idle time, HV2070 includes Standby mode. If the $\overline{\text{STBY}}$ logic input is Low, the device is in Standby mode to reduce the current consumption by shutting down most of the circuity. If the $\overline{\text{STBY}}$ logic input is changed from Low to High, the devices are out of Standby mode and the digital logic circuitry starts working normally after the wake up time, t_{WU}. Figure 5-4 and Figure 5-5 show the Standby mode timing diagram at Bank Switching mode and Individual switching mode respectively. The default logic condition is standby state. The $\overline{\text{STBY}}$ logic input has the highest priority in logic control. See Table 1-1 for details.

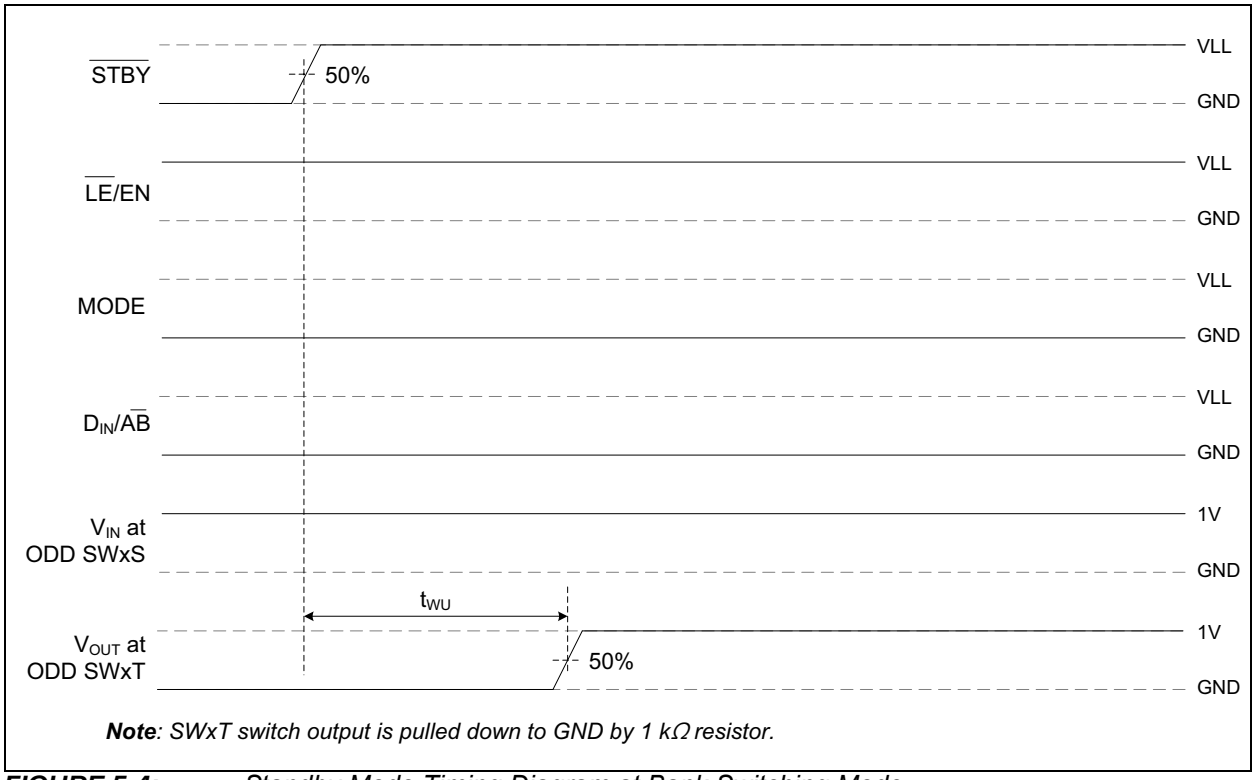
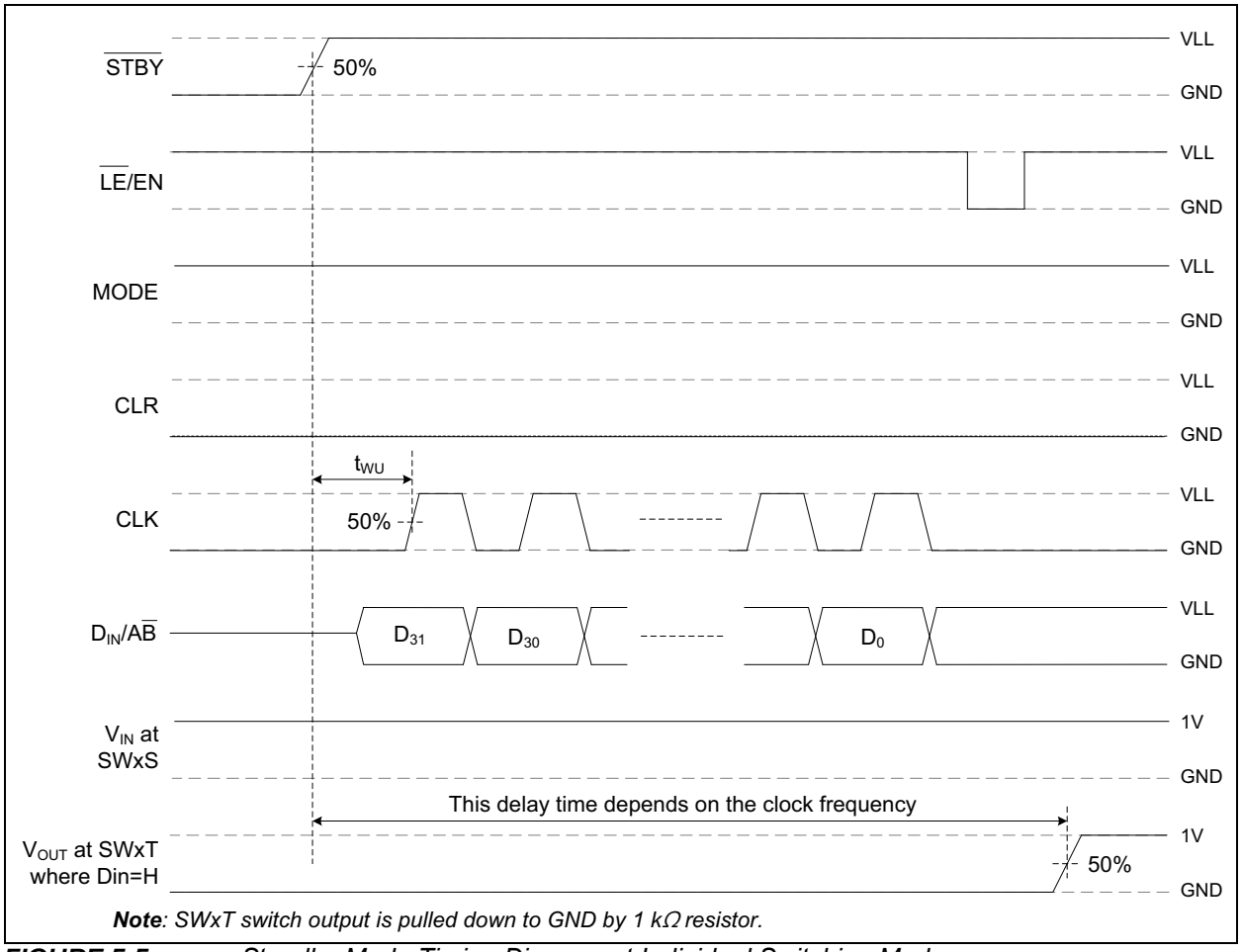


FIGURE 5-4: *Standby Mode Timing Diagram at Bank Switching Mode.*



***Note**: SWxT switch output is pulled down to GND by 1 kΩ resistor.*

FIGURE 5-5: *Standby Mode Timing Diagram at Individual Switching Mode.*

5.7 Power-Up Sequence

The HV2070 device has a recommended power-up sequence. It is recommended that V_{SS} and V_{DD} are powered up first, and the V_{LL} is powered up. The power-down sequence is in reverse order of the power-up sequence. During the power-up/down period, all the analog switch inputs should be within between V_{DD} and V_{SS} or floating.

5.8 Layout Considerations

The HV2070 device has two separate ground connections. DGND is the ground connection for digital circuitry and GND is the ground connection for analog switches and substrate. It is important to have a good PCB layout that minimizes noise and ground bounce. It is recommended to use two separate ground planes in the PCB and to connect the ground planes at the return terminal of the input power line. See Figure 5-6.

It is recommended that 0.1 µF or larger ceramic decoupling capacitors, with low ESR (Equivalent Series Resistance) and appropriate voltage ratings, be connected between ground and power supplies as shown in Figure 5-6. The decoupling capacitor of V_{LL} should be connected to DGND, and the decoupling capacitors of V_{DD} and V_{SS} should be connected to GND. These decoupling capacitors should be placed as close as possible to the device.

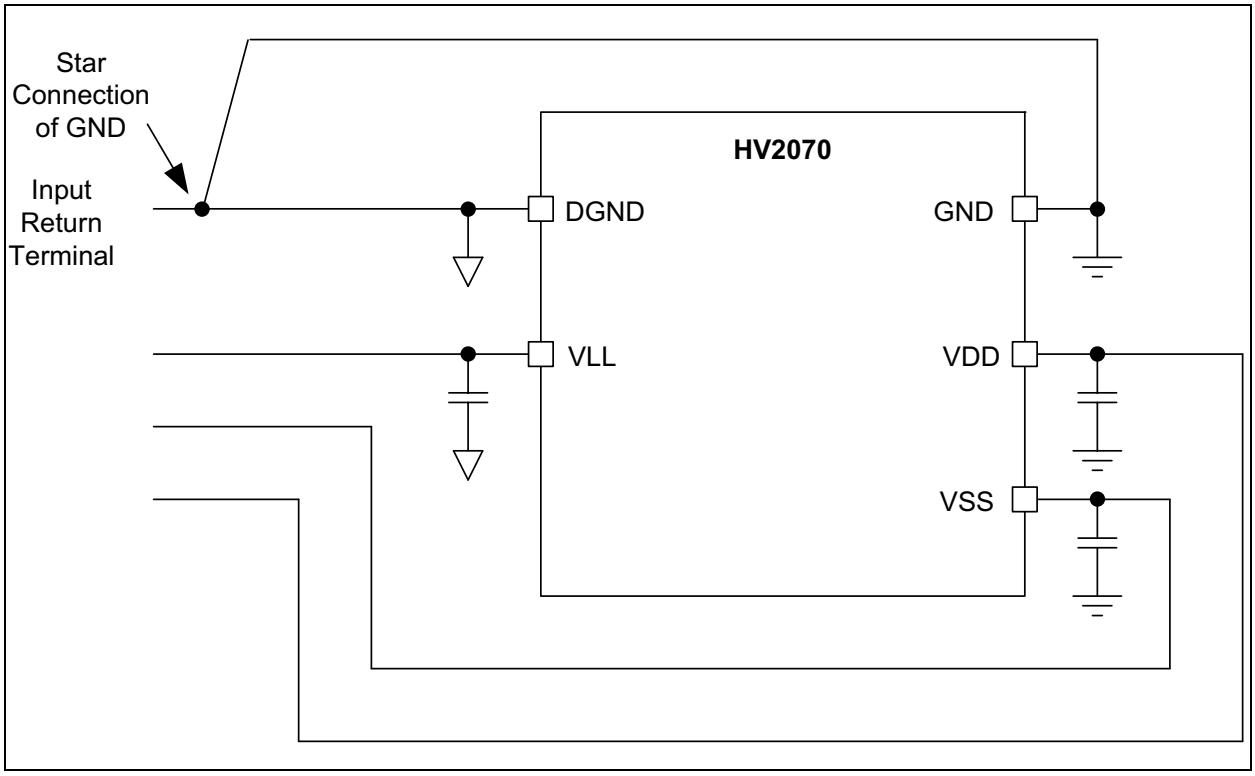


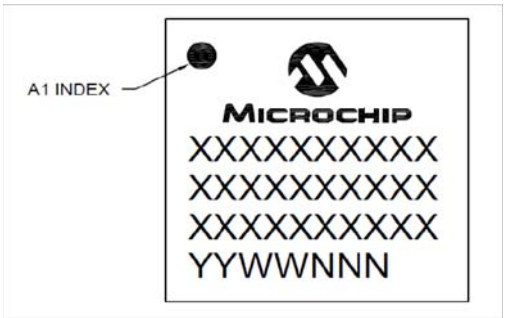
FIGURE 5-6: *Layout Guidelines.*

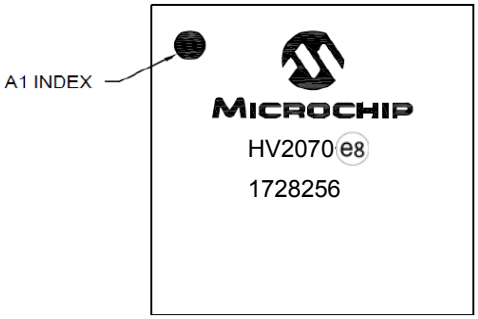
NOTES:

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

121-Ball TFBGA(10 x10 x 1.1 mm)



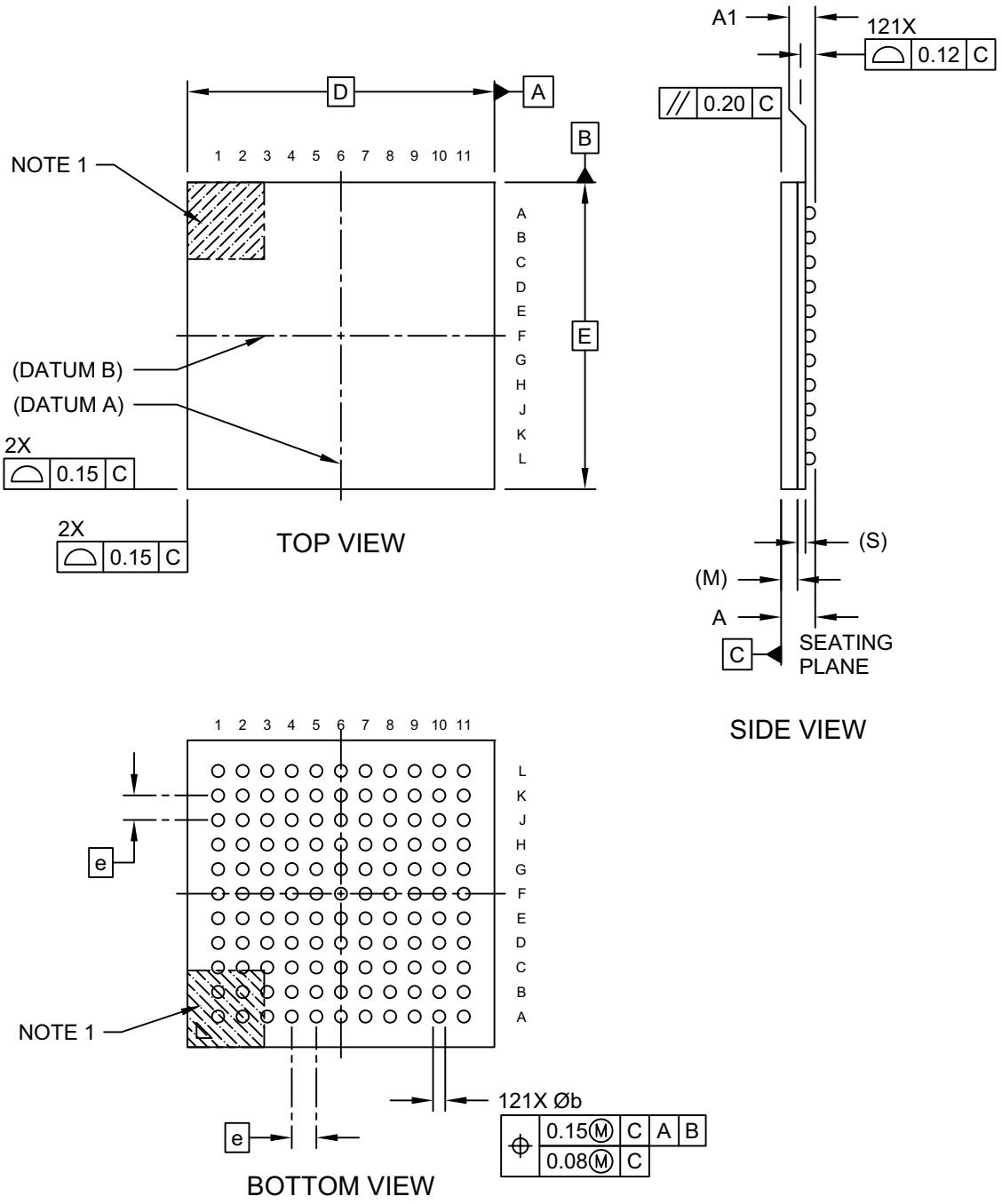


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e8	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e8) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

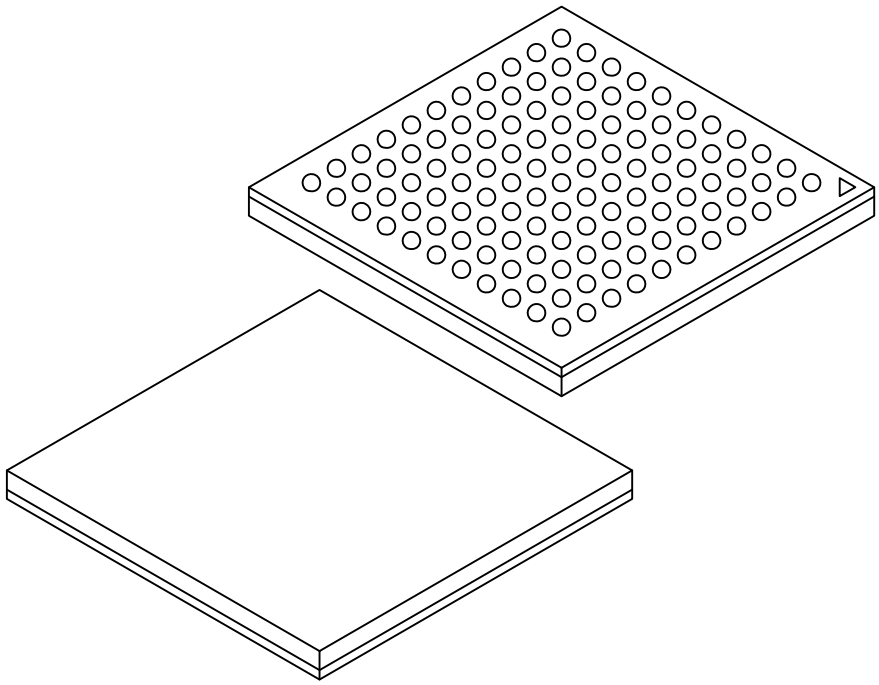
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1216A Sheet 1 of 2

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		121	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Terminal (ball) height	A1	0.270	-	0.37
Substrate Thickness	S		0.26 REF	
Mold Cap Thickness	M		0.53 REF	
Overall Length	D		10.00 BSC	
Overall Width	E		10.00 BSC	
Terminal Width	b	0.38	0.40	0.48

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

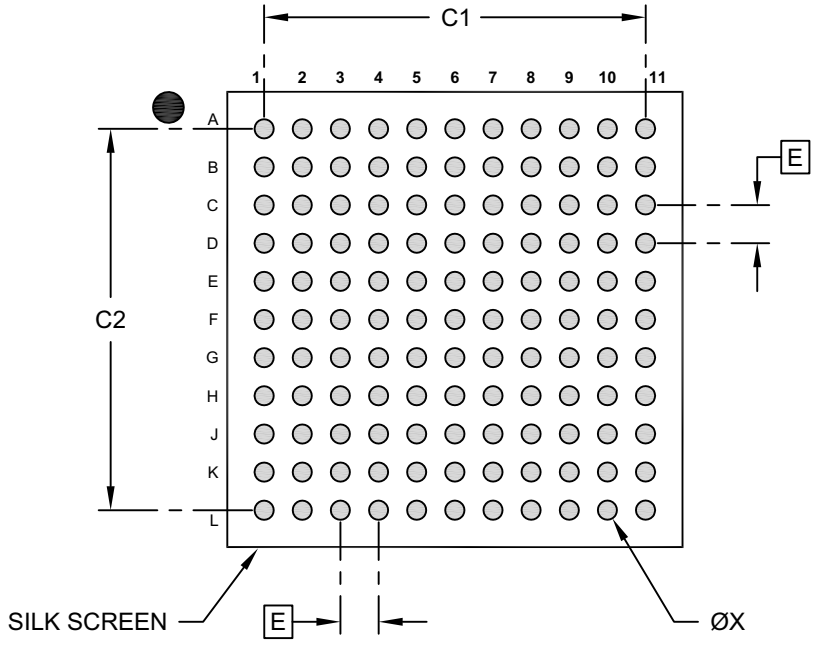
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1216A Sheet 2 of 2

121-Ball Thin, Fine Pitch Ball Grid Array (AJA) - 10x10 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.40

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3216A

APPENDIX A: REVISION HISTORY

Revision A (December 2017)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. /XX Device Package	Examples:
Device: HV2070: No High-Voltage Bias, 32-Channel, High-Voltage Analog Switch with L-Switch Architecture **Package:** AJA= Thin Fine Pitch Ball Grid Array - 10 x10 x 1.1 mm (TFBGA), 121 Ball	a) HV2070/AJA: No High-Voltage Bias, 32-Channel, High-Voltage Analog Switch with L-Switch Architecture, Thin Fine Pitch Ball Grid Array (TFBGA), 121 Ball Package

NOTES:

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