- **Members of the Texas Instruments**
  ***Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes**
  PCB Layout
- **Distributed V$_{CC}$ and GND Pin Configuration**
  Minimizes High-Speed Switching Noise
- ***EPIC*™ (Enhanced-Performance Implanted**
  CMOS) 1-μm Process
- **500-mA Typical Latch-Up Immunity at**
  125°C
- **Package Options Include Plastic 300-mil**
  Shrink Small-Outline (DL) Packages Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Packages Using 25-mil Center-to-Center
  Pin Spacings

54ACT16827 . . . WD PACKAGE
74ACT16827 . . . DL PACKAGE
(TOP VIEW)

1$\overline{OE1}$	1	56	1$\overline{OE2}$
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	A14
V$_{CC}$	7	50	V$_{CC}$
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
V$_{CC}$	22	35	V$_{CC}$
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2$\overline{OE1}$	28	29	2$\overline{OE2}$
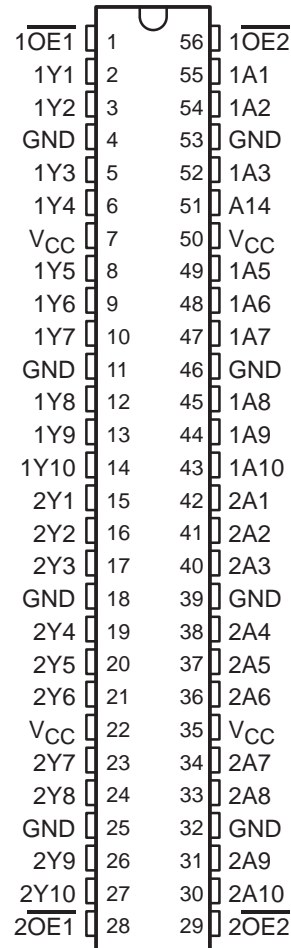
description

The 'ACT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$ or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74ACT16827 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16827 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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logic symbol†

Pin	Signal			Pin	Signal
1	1$\overline{OE1}$		& EN1		
56	1$\overline{OE2}$				
28	2$\overline{OE1}$		& EN2		
29	2$\overline{OE2}$				
55	1A1	1	1 ▽	2	1Y1
54	1A2			3	1Y2
52	1A3			5	1Y3
51	1A4			6	1Y4
49	1A5			8	1Y5
48	1A6			9	1Y6
47	1A7			10	1Y7
45	1A8			12	1Y8
44	1A9			13	1Y9
43	1A10			14	1Y10
42	2A1	1	2 ▽	15	2Y1
41	2A2			16	2Y2
40	2A3			17	2Y3
38	2A4			19	2Y4
37	2A5			20	2Y5
36	2A6			21	2Y6
34	2A7			23	2Y7
33	2A8			24	2Y8
31	2A9			26	2Y9
30	2A10			27	2Y10
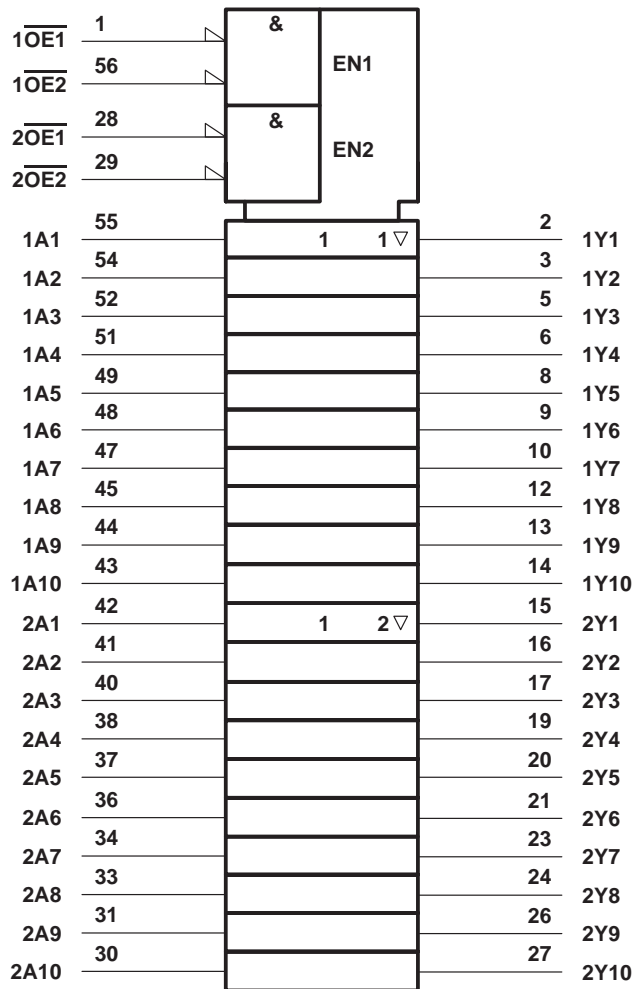
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Nine Other Channels

To Nine Other Channels
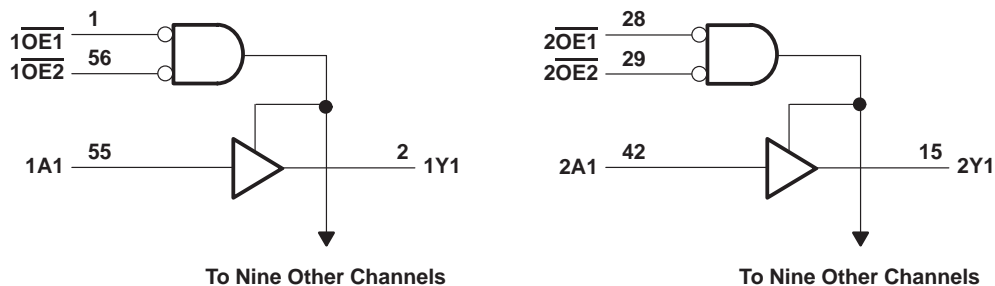
absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... 50 mA
Continuous current through V_{CC} or GND .... ±500 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DL package .... 1.4 W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16827			54ACT16827			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16827		74ACT16827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24$ mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75$ mA†	5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50$ µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75$ mA†	5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5$ V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16827		74ACT16827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.6	7.4	9.8	3.6	11	3.6	11	ns
t_{PHL}			2.8	7.4	9.8	2.8	10.8	2.8	10.8	
t_{PZH}	$\overline{OE}$	Y	3	7.9	10.4	3	11.7	3	11.7	ns
t_{PZL}			4	9.6	12.4	4	14	4	14	
t_{PHZ}	$\overline{OE}$	Y	5.8	9.1	11.3	5.8	12.4	5.8	12.4	ns
t_{PLZ}			5.3	8.5	10.5	5.3	11.5	5.3	11.5	

operating characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50$ pF, f = 1 MHz	41	pF
		Outputs disabled		10	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

From Output Under Test

500 Ω **S1**

$2 \times V_{CC}$

○ Open

○ GND

C_L = 50 pF (see Note A)

500 Ω

LOAD CIRCUIT

Input 3 V 1.5 V 1.5 V 0 V

t_{PLH} t_{PHL}

In-Phase Output V_{OH} 50% V_{CC} 50% V_{CC} V_{OL}

t_{PHL} t_{PLH}

Out-of-Phase Output V_{OH} 50% V_{CC} 50% V_{CC} V_{OL}

VOLTAGE WAVEFORMS

Output Control (low-level enabling) 3 V 1.5 V 1.5 V 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B) 50% V_{CC} ≈ V_{CC} 20% V_{CC} V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) V_{OH} 50% V_{CC} 80% V_{CC} ≈ 0 V

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
      D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ACT16827DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16827	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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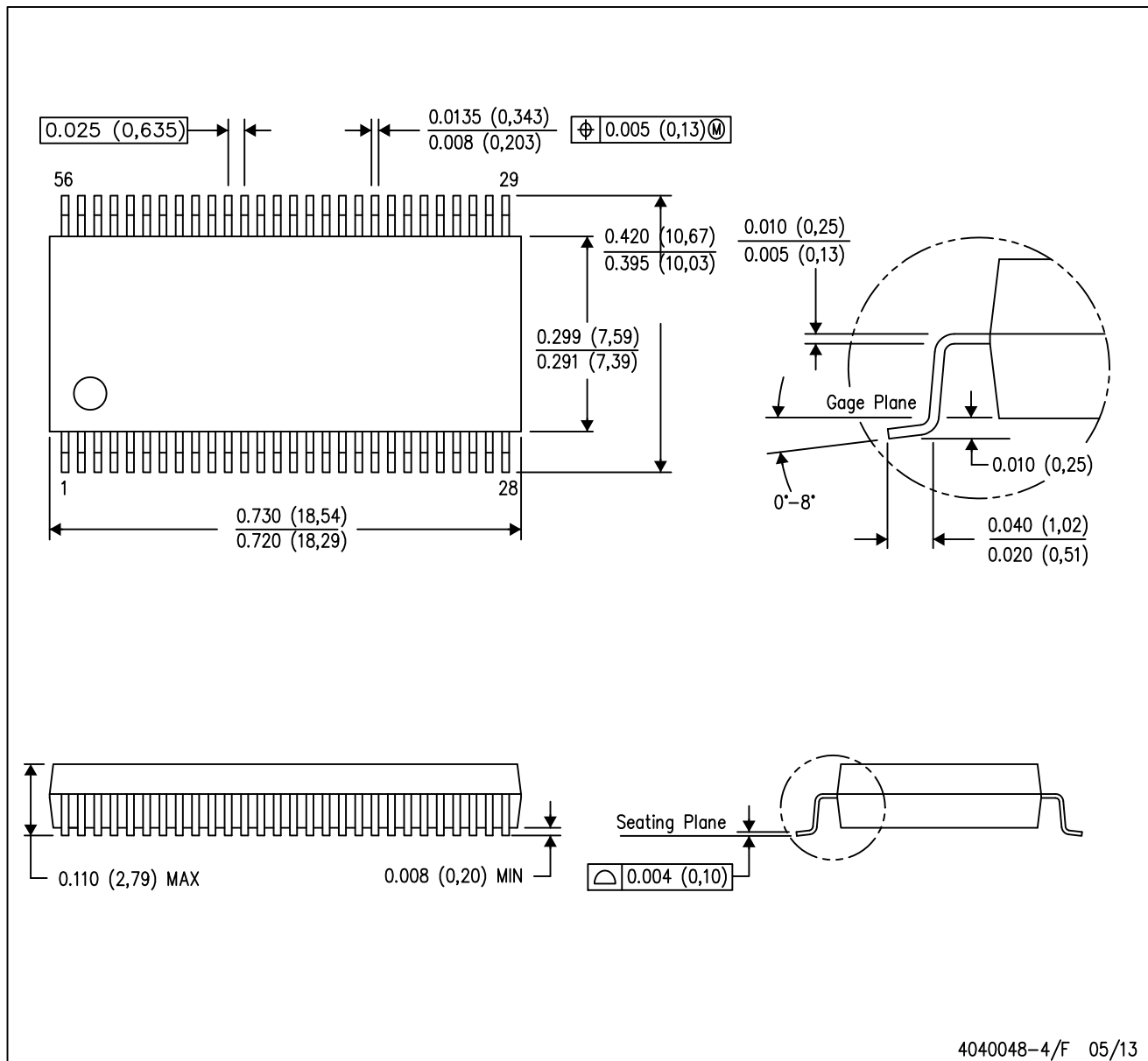# PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74ACT16827DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0°−8°

0.010 (0,25)

0.040 (1,02)
0.020 (0,51)

1   28

0.730 (18,54)
0.720 (18,29)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F 05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MO−118

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