0.4 Ω, Low Resistance and Capacitance, Dual DPDT / Quad SPDT Analog Switch

DESCRIPTION

The DG2523 and DG2524 are four-channel single-pole double-throw (SPDT) analog switches. The DG2523 has two control inputs that each controls a pair of single-pole double-throw (SPDT). It is also known as a two-channel double-pole double-throw (DPDT) configuration. The DG2524 has an $\overline{EN}$ pin to enable the device when the logic is low.

The parts are designed to operate from 1.8 V to 5.5 V single power rail. All switches conduct equally well in both directions, offering rail to rail signal witching and can be used both as multiplexers as well as de-multiplexers. The parts feature low control logic threshold. Break-before-make switching is guaranteed.

The DG2523 and DG2524 exhibit low parasitic capacitance, low leakage, and highly matched low and flat switch resistance over the full signal range characters that are important for precision analog designs.

The high bandwidth and excellent total harmonic distortion (THD) performance make them ideal for both analog and digital signal switching in space constrain applications requiring high performance and efficient use of board space.

The DG2523 and DG2524 come in Pb-free QFN-16 package of 3 mm x 3 mm.

BENEFITS

- Low and flat resistance
- Excellent total harmonic distortion
- Low parasitic capacitance
- Low voltage control interface

FEATURES

- 1.8 V to 5.5 V single supply operation
- Low resistance: 0.4 Ω / typ. at 2.7 V
- Highly flat and matched R_{on}
- Low parasitic capacitance, C_{on} = 26 pF, C_{off} = 14.5 pF
- Typical switch off leakage of 40 pA
- High bandwidth: 310 MHz
- Guaranteed logic high 1.2 V, logic low 0.3 V
- Break before make switching
- Signal swing over V+ capable
- Power down protection
- Latch up current: 300 mA (JESD78)
- ESD/HBM: > 6 kV
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

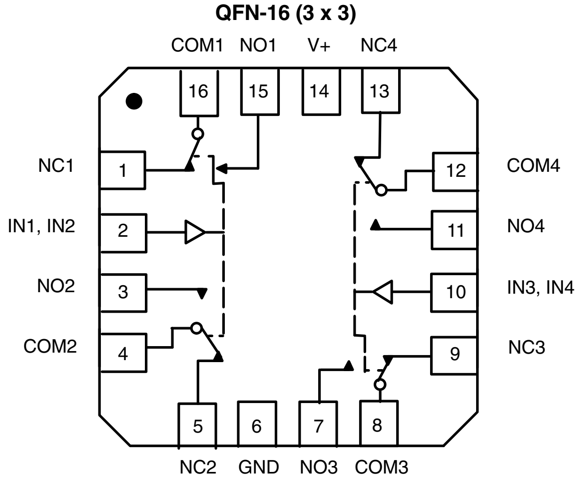
RoHS COMPLIANT

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Battery powered systems
- Computer peripherals
- Data storage
- Relay replacement

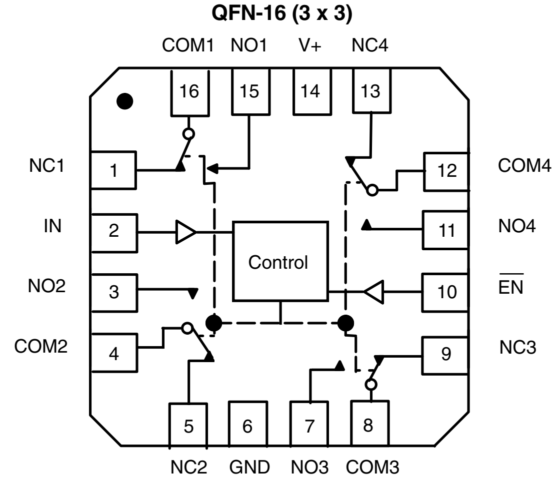
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2523DN
QFN-16 (3 x 3)



Top View

DG2524DN
QFN-16 (3 x 3)



Top View

TRUTH TABLE DG2523		
INx	NC1, 2, 3, and 4	NO1, 2, 3, and 4
0	On	Off
1	Off	On

TRUTH TABLE DG2524			
$\overline{EN}$	LOGIC IN	NC1, 2, 3, and 4	NO1, 2, 3, and 4
1	x	Off	Off
0	0	On	Off
0	1	Off	On

ORDERING INFORMATION			
TEMPERATURE RANGE	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY
-40 °C to +85 °C lead (Pb)-free	QFN-16 (3 mm x 3 mm)	DG2523DN-T1-GE4	Tape and reel, 2500 units
		DG2524DN-T1-GE4	

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Reference to GND	V+		-0.3 to +6	V
	IN, COM, NC, NO [a]		-0.3 to (V+ + 0.3)	
Current (any terminal except NO, NC, or COM)			30	mA
Continuous current (NO, NC, or COM)			± 300	
Peak current (pulsed at 1 ms, 10 % duty cycle)			± 500	
Storage temperature (D suffix)			-65 to +150	°C
Package solder reflow conditions [d]	QFN-16		250	
Power dissipation (packages) [b]	QFN-16 [c]		1385	mW

Notes

a. Signals on NC, NO, or COM, or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 17.3 mW/°C above 70 °C.

d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

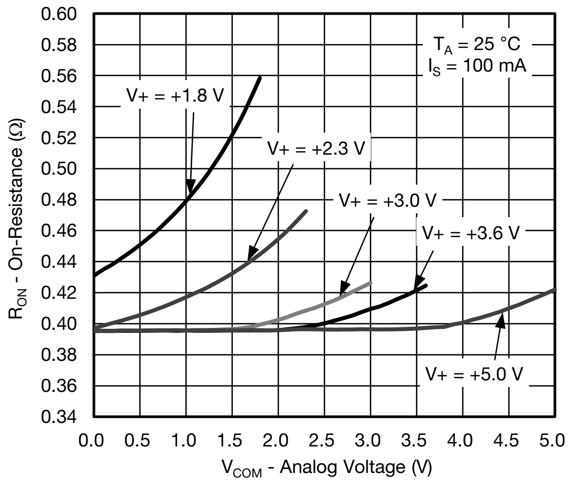
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)							
PARAMETER	SYMBOL	TEST CONDITIONS unless otherwise specified $V+ = 3$ V, ± 10 %, $V_{IN} = 0.5$ V or 1.4 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	$V+ = 2.7$ V, $V_{COM} = 0$ to 2.7 V, I_{NO}, $I_{NC} = 100$ mA	Room	-	0.40	0.55	Ω
			Full	-	-	0.65	
R_{ON} flatness [d]	R_{ON} flatness	$V+ = 2.7$ V, $V_{COM} = 0$ to V+, I_{NO}, $I_{NC} = 100$ mA	Full	-	0.03	0.08	
R_{ON} match [d]	ΔR_{ON}		Room	-	0.05	-	
Switch off leakage current	$I_{NO(off)}$, $I_{NC(off)}$	$V+ = 5.5$ V, V_{NO}, $V_{NC} = 0.5$ V / 4 V, $V_{COM} = 4$ V / 0.5 V	Room	-1	0.04	1	nA
			Full	-5	-	5	
	$I_{COM(off)}$		Room	-1	0.17	1	
			Full	-5	-	5	
Channel-on leakage current	$I_{COM(on)}$	$V+ = 5.5$ V, V_{NO}, $V_{NC} = V_{COM} = 0.5$ V / 4 V	Room	-1	0.17	1	
			Full	-5	-	5	
Digital Control							
Input high voltage	V_{INH}		Full	1.2	-	-	V
Input low voltage	V_{INL}			-	-	0.3	
Input capacitance	C_{IN}		Full	-	5	-	pF
Input current	I_{INL} or I_{INH}	$V_{IN} = 0$ or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or $V_{NC} = 1.5$ V, $R_L = 50$ Ω, $C_L = 35$ pF	Room	-	38	60	µs
			Full	-	-	70	
Turn-off time	t_{OFF}		Room	-	0.43	1	
			Full	-	-	3	
Break-before-make time	t_d		Full	1	-	-	
Charge injection [d]	Q_{INJ}	$C_L = 1$ nF, $V_{GEN} = 1.5$ V, $R_{GEN} = 0$ Ω	Room	-	-19	-	pC
-3 dB bandwidth	BW	$R_L = 50$ Ω, $C_L = 5$ pF	Room	-	310	-	MHz
Off-isolation [d]	OIRR	$R_L = 50$ Ω, $C_L = 5$ pF, f = 100 kHz	Room	-	-82	-	dB
		$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz		-	-55	-	
Crosstalk [d, f]	X_{TALK}	$R_L = 50$ Ω, $C_L = 5$ pF, f = 100 kHz		-	-89	-	
		$R_L = 50$ Ω, $C_L = 5$ pF, f = 1 MHz		-	-61	-	
Total harmonic distortion plus noise	THD + N	2.5 V, signal peak to peak voltage $R_L = 32$ Ω, f = 1 kHz		-	-100	-	
NO, NC off capacitance [d]	$C_{NO(off)}$	f = 1 MHz	Room	-	14.5	-	pF
	$C_{NC(off)}$			-	14.5	-	
Channel-on capacitance [d]	$C_{NO(on)}$			-	26	-	
	$C_{NC(on)}$			-	26	-	
Power Supply							
Power supply range	V+			1.8	-	5.5	V
Power supply current	I+	$V_{IN} = 0$ or V+	Full	-	29	60	µA

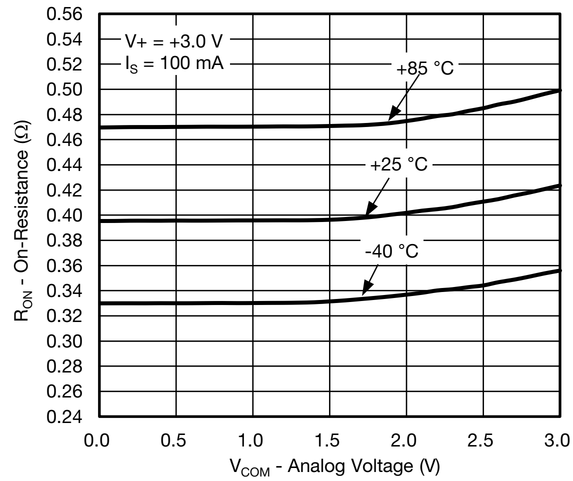
Notes

a. Room = 25 °C, full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk measured between channels.

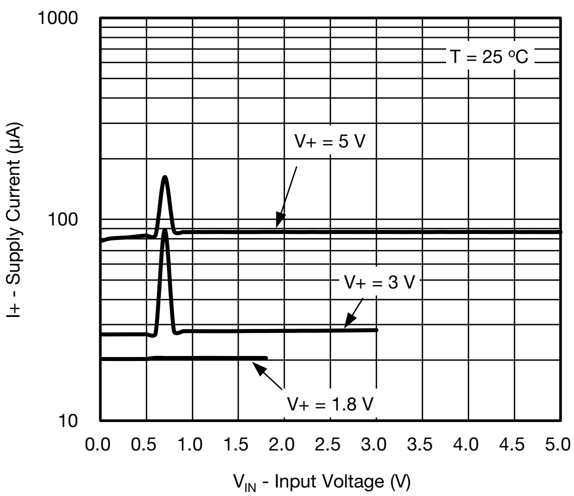
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



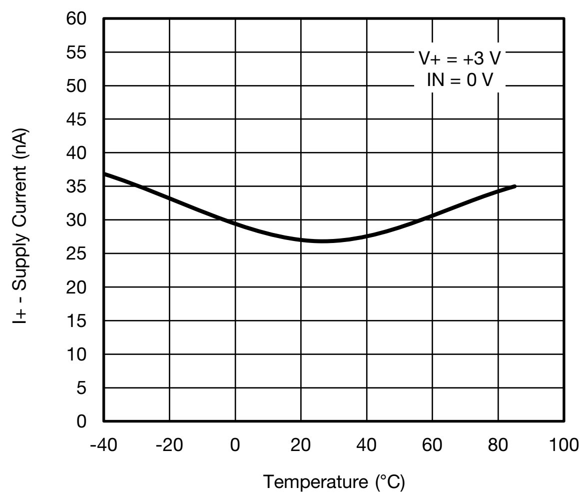
R_{ON} vs. V_{COM} and Supply Voltage



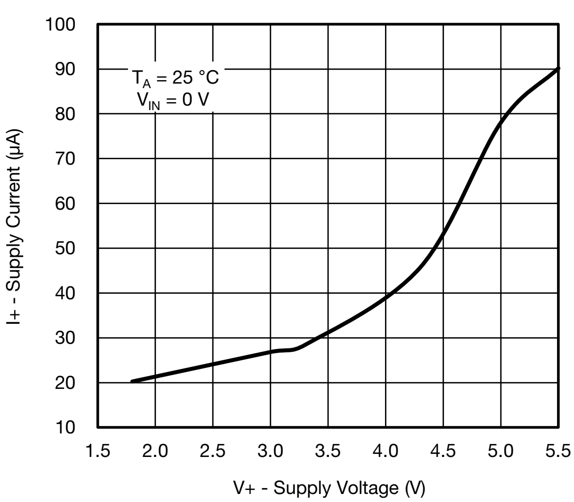
R_{ON} vs. Analog Voltage and Temperature



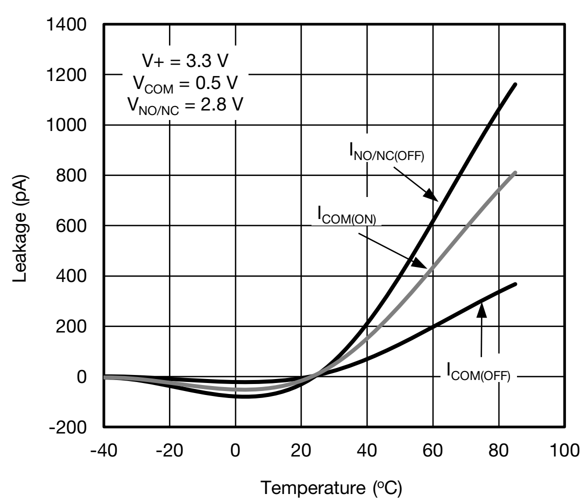
Supply Current vs. Input Voltage



Supply Current vs. Temperature

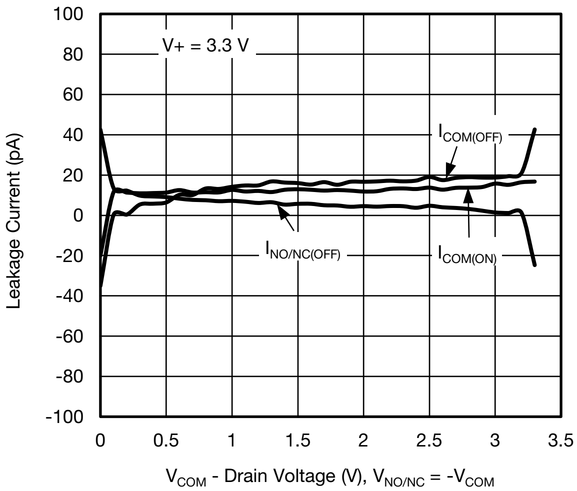


Supply Current vs. Supply Voltage

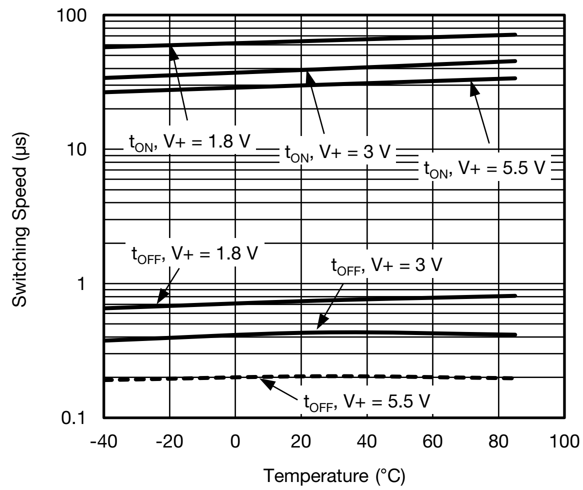


Leakage Current vs. Temperature

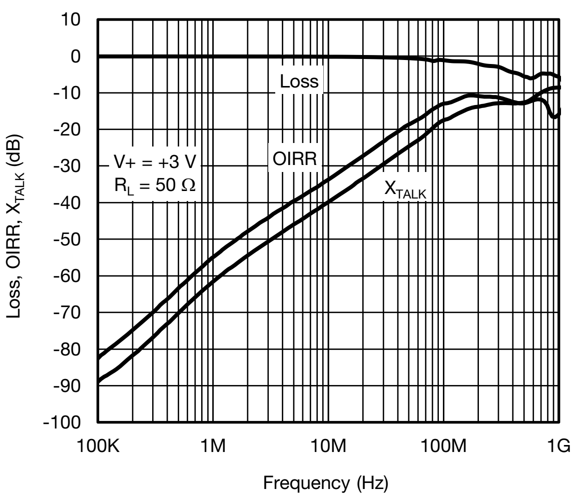
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



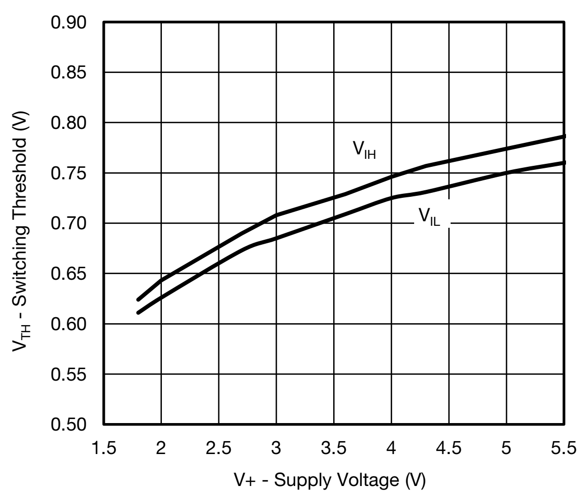
Leakage Current vs. Drain Voltage



Switching Time vs. Temperature

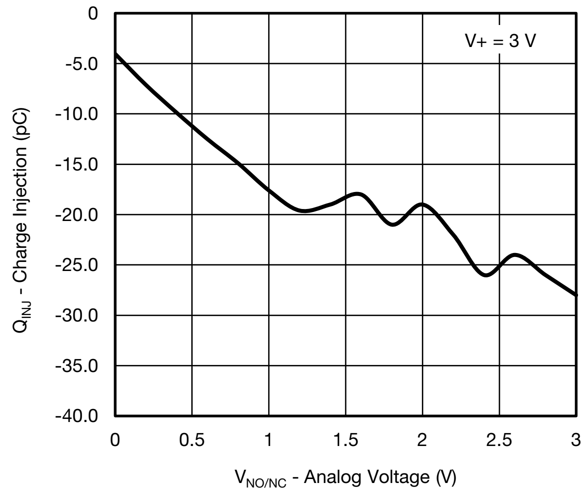


Insertion Loss, Off-Isolation Crosstalk vs. Frequency

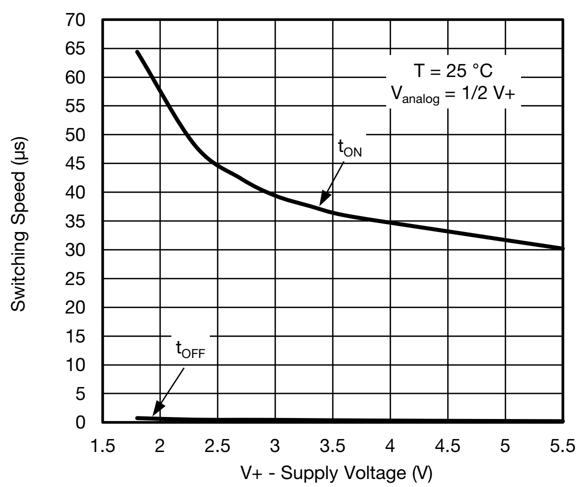


Switching Threshold vs. Supply Voltage

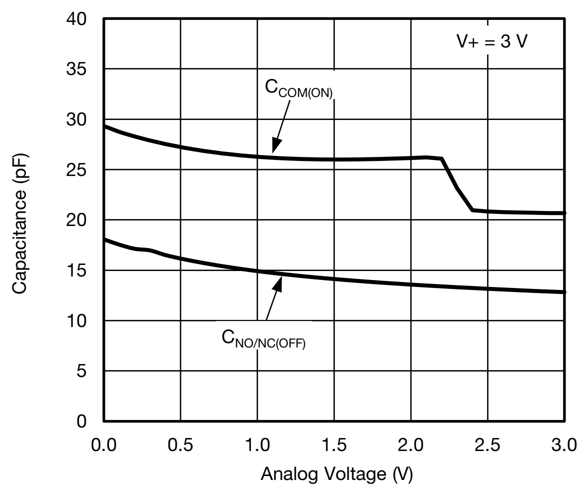
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Charge Injection vs. Analog Voltage

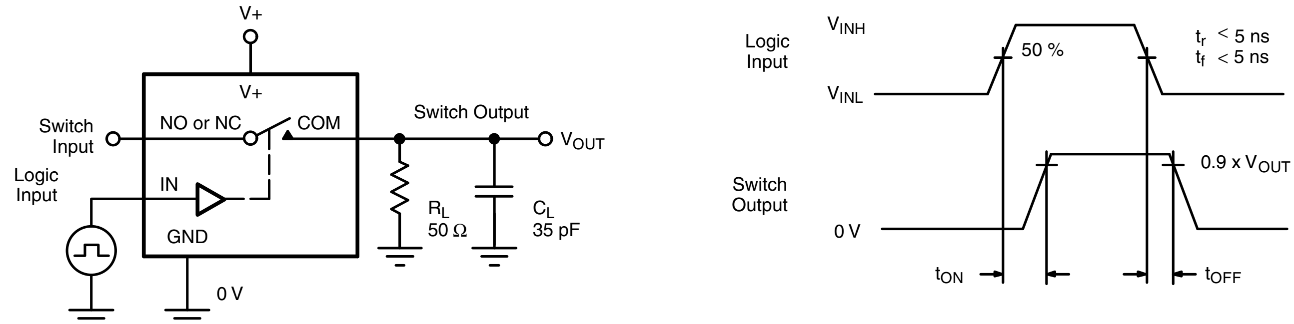


Switching Time vs. Supply Voltage



Capacitance vs. Analog Voltage

TEST CIRCUITS

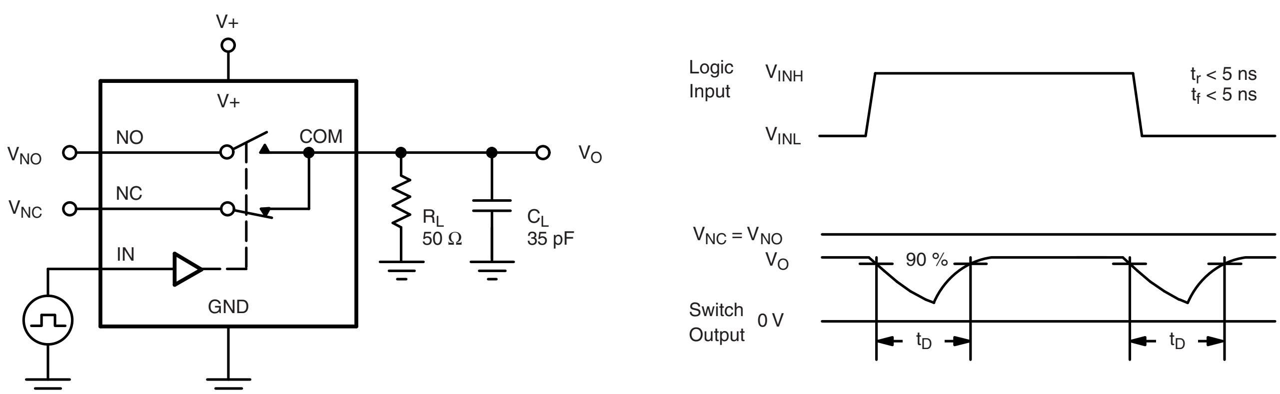


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

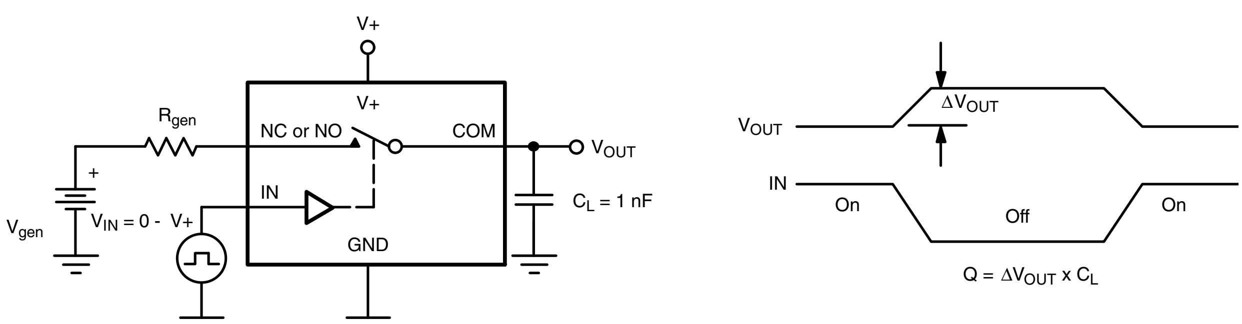
Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

Fig. 2 - Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

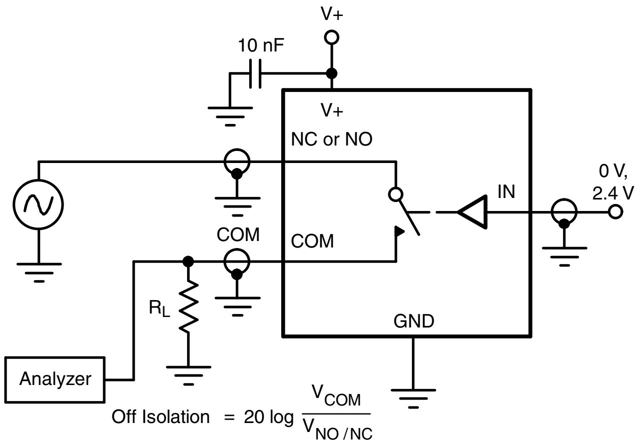


Fig. 4 - Off-Isolation

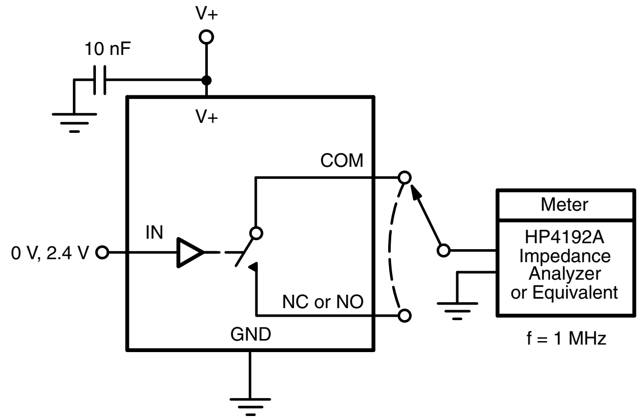


Fig. 5 - Channel Off / On Capacitance

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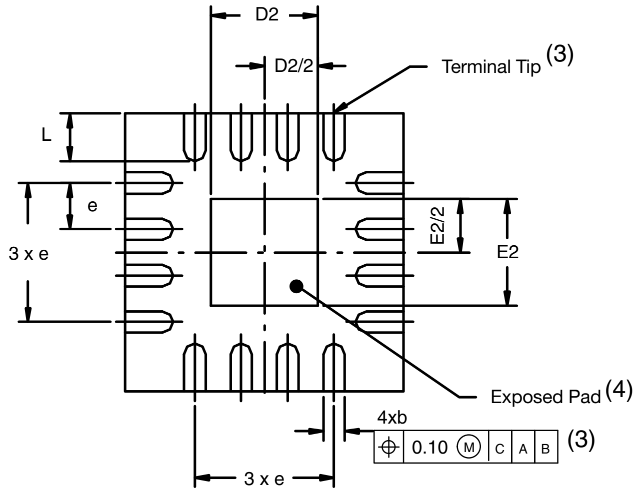
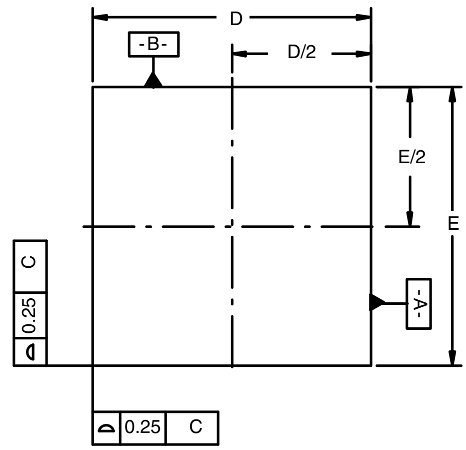
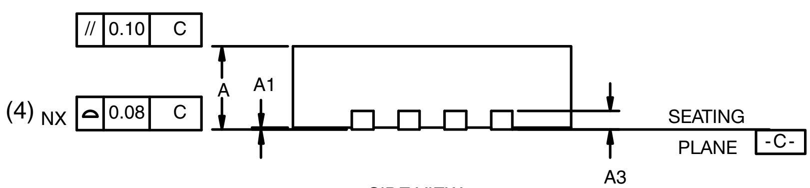
QFN-16 Lead (3 x 3)



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Notes

(1) All dimensions are in millimeters.
(2) N is the total number of terminals.
(3) Dimension b applies to metallized terminal and is measured between 0.25 and 0.30 mm from terminal tip.
(4) Coplanarity applies to the exposed heat sink slug as well as the terminal.
(5) The pin #1 identifier may be either a mold or marked feature, it must be located within the zone indicated.

DIM.	VARIATION 1						VARIATION 2					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039	0.80	0.90	1.00	0.031	0.035	0.039
b	0.18	0.23	0.30	0.007	0.009	0.012	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
E	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020	0.30	0.40	0.50	0.012	0.016	0.020
ECN: T16-0233-Rev. D, 09-May-16 DWG: 5899												

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