AK09970N

3D Magnetic Sensor with Programmable Switch

1. Genaral Description

AK09970N is a 3D magnetic sensor IC with high sensitivity and wide measurement range utilizing our latest Hall sensor technology.
Our ultra-small package of AK09970N incorporates magnetic sensors, chopper stabilized signal, amplifier chain, and all necessary interface logic for detecting weak to strong magnetic fields in the X, Y and Z planes independently. From its compact foot print, thin package, and extremely low power consumption, it is suitable for a wide range of applications such as connected home, door & window opening/close sensing, and magnetic tamper detection of IoT systems or smart meters just to name a few.

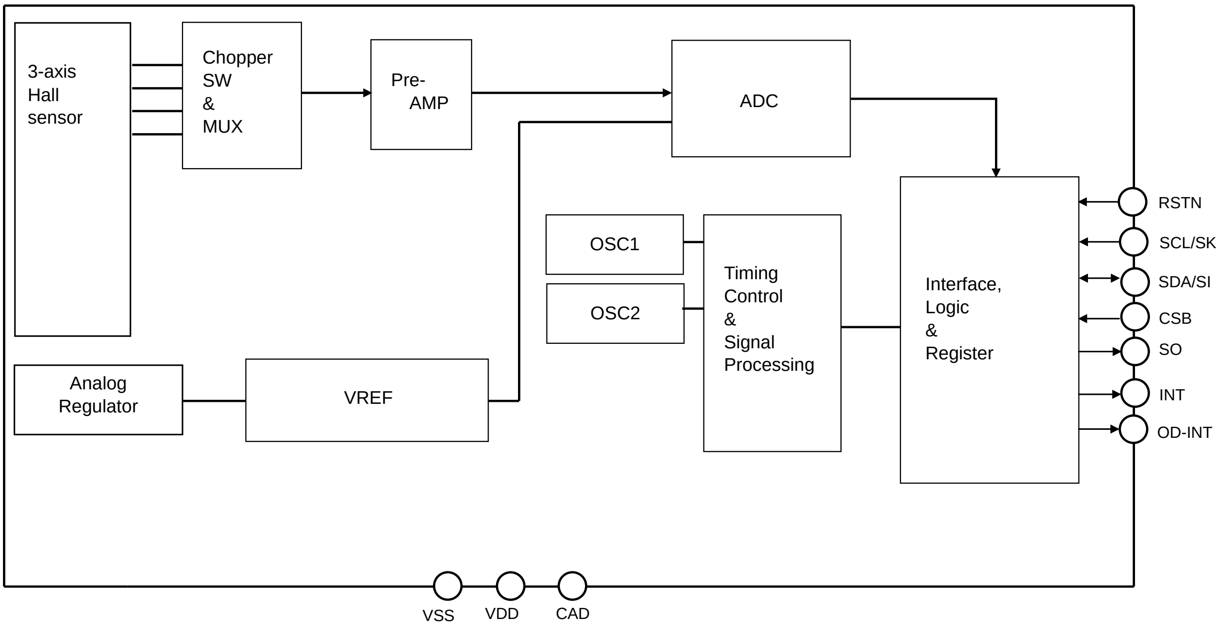
2. Features

- Functions:
  - 16 bit data out for each 3-axis magnetic component
  - Programmable threshold 3-axis magnetometer
  - Built-in A to D Converter for magnetometer data output
  - Selectable sensor measurement range and sensitivity setting
    - High sensitivity setting
      - Sensitivity: 1.1 µT/LSB (typ.)
      - Measurement range: ± 36 mT
    - Wide range setting
      - Sensitivity: 3.1 µT/LSB (typ.)
      - Measurement range: X and Y-axis → ±34.9mT, Z-axis → ±101.5mT
  - Serial interface
    - I2C bus interface
      Standard and Fast mode compliant with Philips I2C specification Ver.2.1
    - 4-wire SPI
  - Operation mode
    - Power-down, Single measurement, Continuous measurement
  - 3-axis programmable switch function
  - Output pin for event notification
    - INT pin and OD-INT pin
  - DRDY function for measurement data ready
  - Magnetic sensor overflow monitor function
  - Built-in oscillator for internal clock source
  - Selectable sensor drive
    - Low power drive / Low noise drive
- Operating temperatures:
  - -40˚C to +85˚C
- Operating supply voltage:
  - +1.7V to +3.6V
- Current consumption (VDD = +1.8V, +25˚C):
  - Power-down: 2.0 nA (typ.)
  - Measurement:
    - Average current consumption at 1 Hz/10Hz repetition rate
      - Low power drive: 1.0 µA(typ.)@1HzODR, 3.5 µA(typ.)@10HzODR
      - Low noise drive: 2.0 µA(typ.) @1HzODR, 12.0 µA(typ.)@10HzODR
- Package
  - AK09970N 16-pin QFN package: 3.0mm x 3.0mm x 0.75mm

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram



4.2. Functions

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
Chopper SW MUX	Multiplexer for selecting Hall elements.
Analog Regulator	Internal power supply.
PREAMP	Differential amplifier used to amplify the magnetic sensor signal.
ADC	Convert analog output to digital output.
OSC1	Generates an operating clock for sensor measurement.
OSC2	Generates an operating periodic clock for sequencer.
VREF	Generates temperature independent reference voltage.
Interface Logic & Register	Exchanges data with an external CPU. INT and OD-INT pin indicates State1 or/and State2 (selectable). State1: Sensor measurement has ended and data is ready to be read. State2: Measurement magnetic data exceeds setting switch threshold value. I2C bus interface using two pins (SCL and SDA). Standard and Fast modes are supported. 4-wire SPI is also supported by SK, SI, SO and CSB pins.
Timing Control & Signal Processing	Generates a timing signal required for internal operation. Magnetic sensitivity adjustment and switch calculation for switch function.

5. Pin Configurations and Functions

Pin No.	Pin name	I/O	Type	Function
1	INT	O	CMOS	Interrupt pin "H" active. Refer to section 10.6.
2	CSB	I	CMOS	Chip select pin for 4-wire SPI "L" active. Connect to VDD when selecting I2C bus interface.
3	SCL	I	CMOS	When the I2C bus interface is selected (CSB pin is connected to VDD). SCL: Control clock input pin Input: Schmitt trigger
	SK			When the 4-wire SPI is selected. SK: Serial clock input pin
4	N/C	-	-	Non-connect. Keep this pin non-connected.
5	SDA	I/O	CMOS	When the I2C bus interface is selected (CSB pin is connected to VDD). SDA: Control data input/output pin Input: Schmitt trigger, Output: Open-drain
	SI	I		When the 4-wire SPI is selected. SI: Serial data input pin
6	SO	O	CMOS	When the I2C bus interface is selected (CSB pin is connected to VDD) Hi-Z output. Keep this pin electrically non-connected.
				When the 4-wire SPI is selected. Serial data output pin
7	N/C	-	-	Non-connect. Keep this pin non-connected.
8	N/C	-	-	Non-connect. Keep this pin non-connected.
9	N/C	-	-	Non-connect. Keep this pin non-connected.
10	N/C	-	-	Non-connect. Keep this pin non-connected.
11	OD-INT	O	Open Drain	Open-drain interrupt pin "L" active. Refer to section 10.6.
12	CAD	I	CMOS	When the I2C bus interface is selected (CSB pin is connected to VDD). CAD: Slave address input pin Connect to VSS or VDD.
				When the 4-wire serial interface is selected. Connect to VSS.
13	VSS	-	Power	Ground pin
14	N/C	-	-	Non-connect. Keep this pin non-connected.
15	VDD	-	Power	Positive power supply pin
16	RSTN	I	CMOS	Reset pin Resets registers by setting to "L".

6. **Absolute Maximum Ratings**

VSS=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-10	+10	mA
Storage temperature	Tstg	-40	+125	˚C

Note:
If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

7. **Recommended Operating Conditions**

VSS=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	-	Ta	-40	-	+85	˚C
Power supply voltage	VDD pin voltage	Vdd	1.7	1.8	3.6	V

8. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd = 1.7V to 3.6V, Temperature range = -40 ˚C to 85 ˚C
Typical condition: Vdd = 1.8 V, Temperature = 25 ˚C

8.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	CSB RSTN SCL/SK SDA/SI CAD	-	70%Vdd	-	-	V
Low level input voltage	VIL		-	-	-	30%Vdd	V
Input current	IIN		VIN = Vss or Vdd	-10		+10	µA
Hysteresis input voltage *1	VHS	CSB RSTN SCL/SK SDA/SI	Vdd≥2V	5%Vdd	-	-	V
			Vdd<2V	10%Vdd			
High level output voltage *2	VOH	SO INT	IOH≥-100µA	80%Vdd	-	-	V
Low level output voltage 1 *2	VOL1	SO INT	IOL≤+100µA	-	-	20%Vdd	V
Low level output voltage 2 *3	VOL2	SDA/SI OD-INT	IOL2≤+3mA Vdd≥2V	-	-	0.4	V
			IOL2≤+3mA Vdd<2V	-	-	20%Vdd	V
Current consumption *4	IDD1	VDD	Power-down mode	-	2.0	2000	nA
	IDD2		When magnetic sensor is driven	-	1.5	2.2	mA
	IDD3		All Power-down (RSTN pin = L)	-	2.0	2000	nA

Notes:
* 1. Schmitt trigger input (reference value for design).
* 2. IOH: High level output current. IOL: Low level output current.
* 3. Output is open-drain. Connect to a pull-up resistor externally.
* 4. Without any resistance load.

8.2. AC Characteristics of RSTN

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Wait time for reset	twRST	RSTN	Vdd > 80%Vdd	5	-	-	µs
Reset input effective pulse width	tRSTL	RSTN	Vdd > 80%Vdd	5	-	-	µs
Reset input ineffective pulse width	tSPRST	RSTN	-	-	-	1	µs

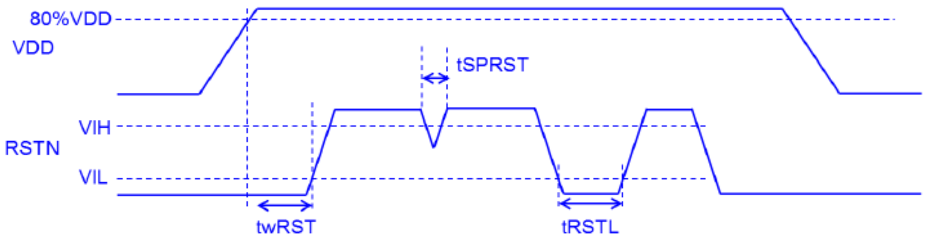


Figure 8.1 Reset condition

8.3. **AC Characteristics of INT and OD-INT**

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Fall time of OD-INT	TfOD	OD-INT	CL = 50 pF RL = 20 kΩ(typ.)	-	-	250	ns
Fall time of INT	TfINT	INT	CL = 50 pF	-	-	250	ns
Rise time of INT	TrINT	INT	CL = 50 pF	-	-	250	ns

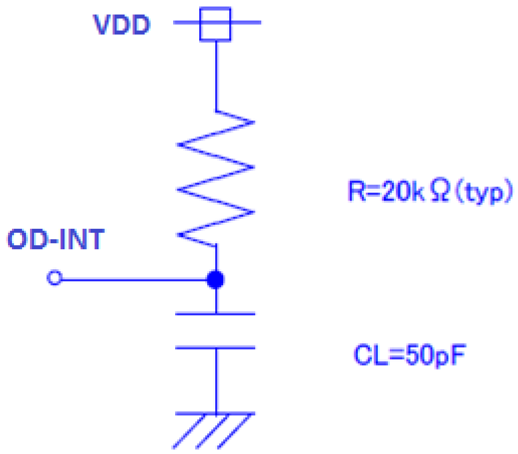
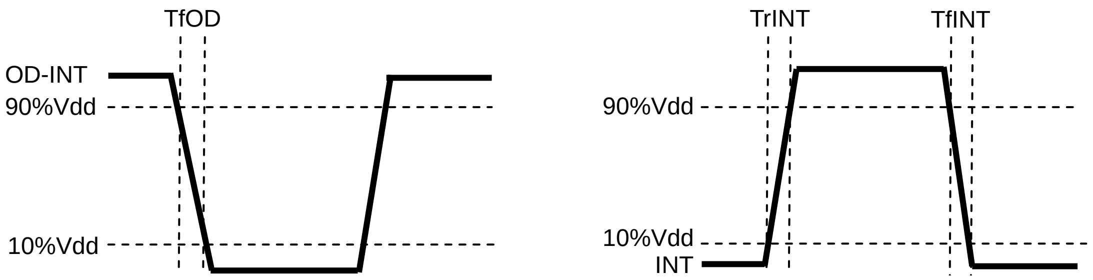


Figure 8.2 Output load circuit of OD-INT (recommended circuit)

[Rise time and fall time]



8.4. **Overall Characteristics**

Table 8.1 High sensitivity setting

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	-	-	16	-	Bit
Time for measurement	TSM	SDR bit = “0” (Low noise drive)	-	0.792	0.872	ms
		SDR bit = “1” (Low power drive)	-	0.23	0.253	
Magnetic sensor sensitivity	BSE	Ta = 25 ˚C, SMR bit = “0”	0.99	1.1	1.21	µT/LSB
Magnetic sensor measurement range	BRG	Ta = 25 ˚C, SMR bit = “0”	±32.44	±36.04	±39.64	mT
Magnetic sensor initial offset[* 5]	BOF	Ta = 25 ˚C, X and Y-axis	-614	-	+614	LSB
		Ta = 25 ˚C, Z-axis	-868	-	+868	
Noise[* 6]	NIS	SDR bit = “0” (Low noise drive)	-	5.0	-	µTrms
		SDR bit = ”1” (Low power drive)	-	15.0	-	

Table 8.2 Wide range setting

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	-	-	16	-	Bit
Time for measurement	TSM	SDR bit = “0” (Low noise drive)	-	0.792	0.872	ms
		SDR bit = “1” (Low power drive)	-	0.23	0.253	
Magnetic sensor sensitivity	BSE	Ta = 25 ˚C, SMR bit = “1”	2.79	3.1	3.41	µT/LSB
Magnetic sensor measurement range	BRG	Ta = 25 ˚C, X and Y-axis, SMR bit = “1”	±31.42	±34.91	±38.4	mT
		Ta = 25 ˚C, Z-axis, SMR bit = “1”	±91.42	±101.57	±111.73	
Magnetic sensor initial offset[* 5]	BOF	Ta = 25 ˚C, X and Y-axis	-218	-	+218	LSB
		Ta = 25 ˚C, Z-axis	-308	-	+308	
Noise[* 6]	NIS	SDR bit = “0” (Low noise drive)	-	6.0	-	µTrms
		SDR bit = “1” (Low power drive)		18.0		

Note:
* 5. Value of measurement data register on shipment test without applying magnetic field on purpose.
* 6. Reference value for design. Under steady magnetic field.

8.5. **4-wire SPI**

4-wire SPI is compliant with mode 3 (SPI-mode3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SK clock frequency	Fspi	-	-	-	4.0	MHz
CSB setup time	Tcs	-	50	-	-	ns
Data setup time	Ts	-	50	-	-	ns
Data hold time	Th	-	50	-	-	ns
SK high time	Twh	Vdd≥2.5V	100	-	-	ns
		2.5V>Vdd≥1.7V	150	-	-	ns
SK low time	Twl	Vdd≥2.5V	100	-	-	ns
		2.5V>Vdd≥1.7V	150	-	-	ns
SK setup time	Tsd	-	50	-	-	ns
SK to SO delay time* 7	Tdd	-	-	-	50	ns
CSB to SO delay time* 7	Tcd	-	-	-	50	ns
SK rise time* 8	Tr	-	-	-	100	ns
SK fall time* 8	Tf	-	-	-	100	ns
CSB high time	Tch	-	450	-		ns

Notes:
* 7.SO load capacitance: 20pF
* 8.Reference value for design

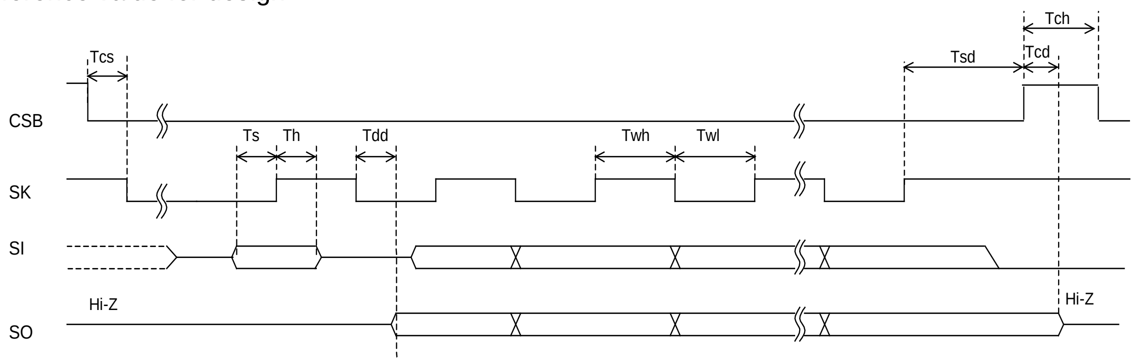


Figure 8.3 4-wire SPI

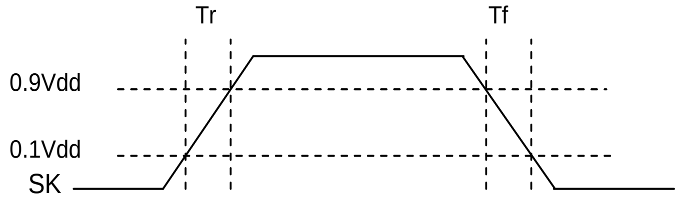


Figure 8.4 Rise time and fall time

8.6. I²C Bus Interface

CSB pin = "H"

I²C bus interface is compliant with Standard mode and Fast mode. Standard/Fast is selected automatically by fSCL.

- Standard mode
  fSCL≤100kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency	-	-	100	kHz
tHIGH	SCL clock "High" time	4.0	-	-	µs
tLOW	SCL clock "Low" time	4.7	-	-	µs
tR	SDA and SCL rise time	-	-	1.0	µs
tF	SDA and SCL fall time	-	-	0.3	µs
tHD:STA	Start Condition hold time	4.0	-	-	µs
tSU:STA	Start Condition setup time	4.7	-	-	µs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0	-	-	µs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250	-	-	ns
tSU:STO	Stop Condition setup time	4.0	-	-	µs
tBUF	Bus free time	4.7	-	-	µs

- Fast mode
  100kHz<fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency	-	-	400	kHz
tHIGH	SCL clock "High" time	0.6	-	-	µs
tLOW	SCL clock "Low" time	1.3	-	-	µs
tR	SDA and SCL rise time	-	-	0.3	µs
tF	SDA and SCL fall time	-	-	0.3	µs
tHD:STA	Start Condition hold time	0.6	-	-	µs
tSU:STA	Start Condition setup time	0.6	-	-	µs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0	-	-	µs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100	-	-	ns
tSU:STO	Stop Condition setup time	0.6	-	-	µs
tBUF	Bus free time	1.3	-	-	µs
tSP	Noise suppression pulse width	-	-	50	ns

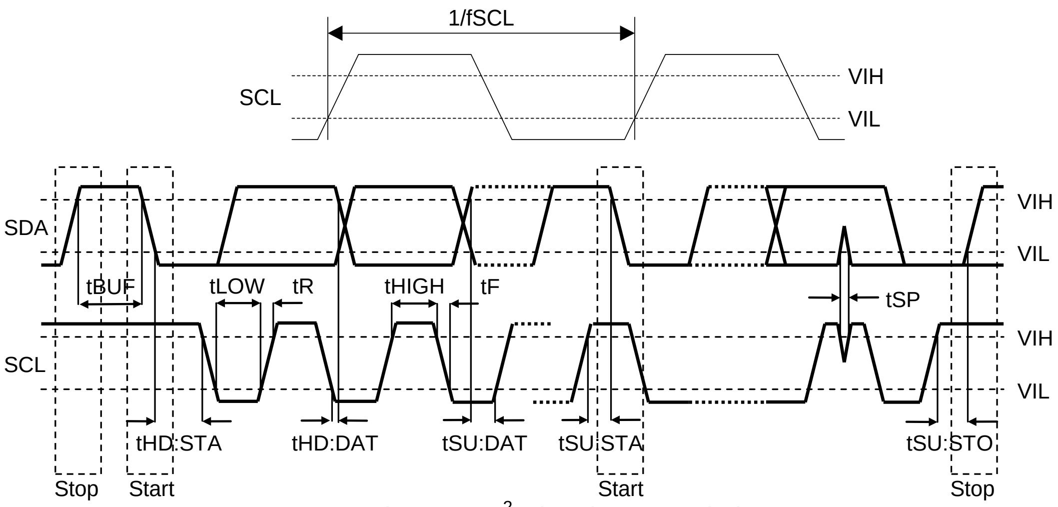


Figure 8.5 I²C bus interface timing

9. Status Description

9.1. State Transition Diagram

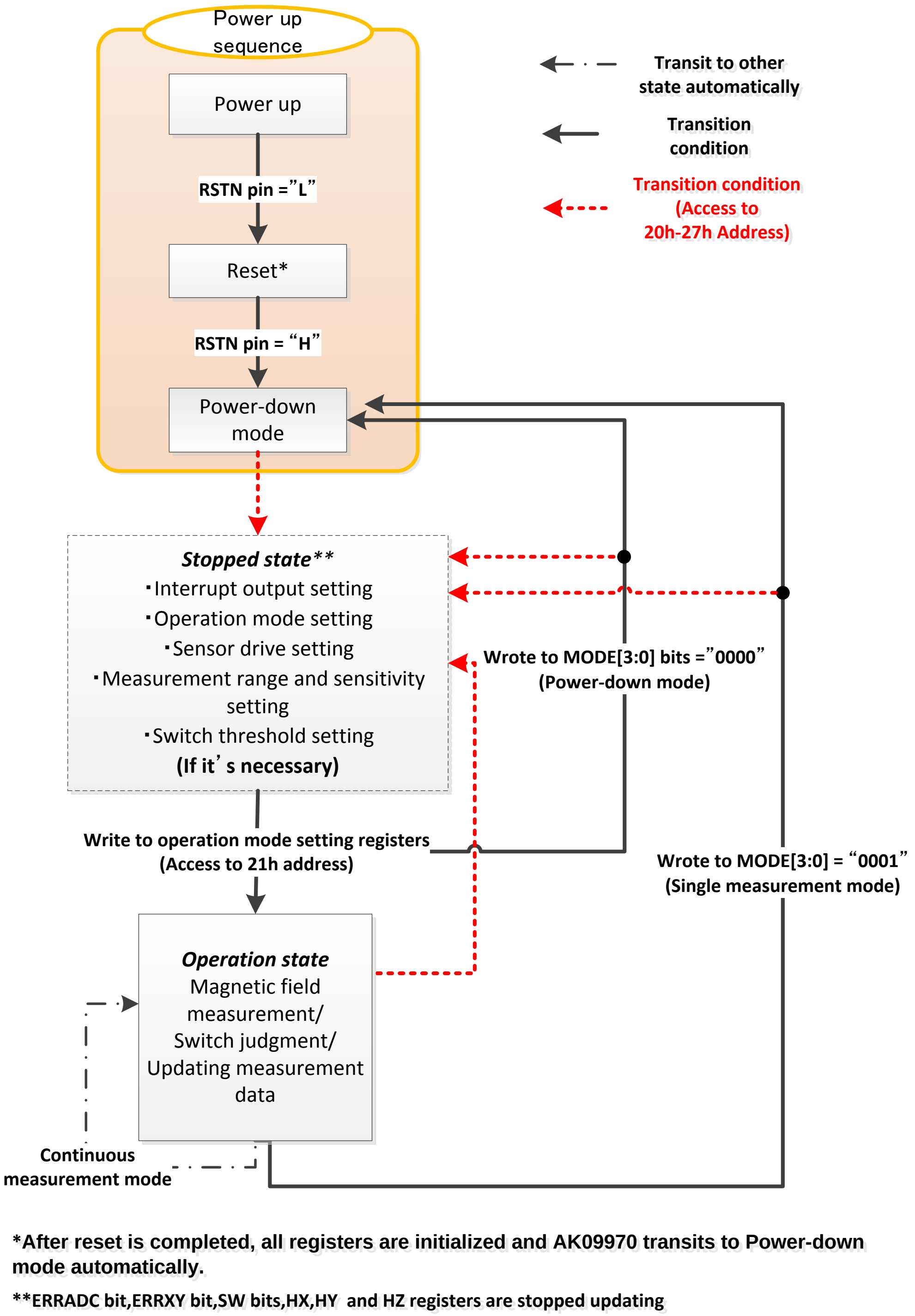


Figure 9.1 State transition diagram

9.2. **Power States**

AK09970N does not have built in power on reset circuit. Reset has to be done manually by user. When RSTN pin is applied a specified voltage (VIL), all registers in AK09970N are initialized.

Table 9.1 Power States

State	VDD	Power state
1	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL, SDA and OD-INT pin should be fixed to "L" (0V).
2	1.7V to 3.6V	ON After reset (RSTN pin = "L"), AK09970N can measure magnetic field. Refer to 8.2.

9.3. **Register States**

Refer to Figure 9.1.

State	**DRDYbit /DOR bit**	**Switch register*9**	**Measurement data register*10**	**Other register**
Reset	0	Default value	Default value	Default value
Power-down mode	Refer to 10.3	Default value or previous result	Default value or previous measurement value	Setting value
Stopped state	DRDY: 0 DOR: previous measurement value	Default value or previous result	Default value or previous measurement value	Setting value
Operation state: (Magnetic field measurement)	Refer to 10.3	Default value or previous result	Default value or previous measurement value	Setting value
Operation state: (Switch judgment and updating measurement data)	Refer to 10.3	Default value or previous result	Previous measurement value	Setting value

Note:
* 9.SW bits (SWX1 bit,SWX2 bit,SWY1 bit,SWY2 bit,SWZ1 bit,SWZ2 bit) , ERRDAC bit and ERRXY bit
* 10.HX, HY and HZ registers

9.4. **Pin States**

Refer to Figure 9.1

State	**INT pin**	**SDA/SI pin**	**SO pin**	**OD-INT pin**	**RSTN pin**	**Other pins**
Reset	L	Hi-Z	Hi-Z	Hi-Z	L	Don't care
Power-down mode	Previous result	Serial interface	Serial interface	Previous result	H	Don't care
Stopped state	L	Serial interface	Serial interface	Hi-Z	H	Don't care
Operation state: (Magnetic field measurement)	Previous result	Serial interface	Serial interface	Previous result	H	Don't care
Operation state: (Switch judgment and updating measurement data)	Previous result	Serial interface	Serial interface	Previous result	H	Don't care

10. Functional Descriptions

10.1. Reset Functions

When AK09970N changes to reset status, it consumes the current of reset state (IDD3).

AK09970N has two types of reset;

I. Reset pin (RSTN)
   AK09970N is reset by Reset pin.
II. Soft reset
   AK09970N is reset by setting SRST bit.

After reset is completed, all registers are initialized and AK0970 transits to Power-down mode automatically.

10.2. Operation modes

AK09970N has following nine operation modes:

(1) Power-down mode (MODE[3:0] bits = ”0000”)
(2) Single measurement mode (MODE[3:0] bits = ”0001”)
   - Sensor is measured for one time and data is output. Transits to Power-down mode automatically after measurement ended.
(3) Continuous measurement mode 1 (MODE[3:0] bits = ”0010”)
   - Sensor is measured periodically in 0.25 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(4) Continuous measurement mode 2 (MODE[3:0] bits = ”0100”)
   - Sensor is measured periodically in 0.5 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(5) Continuous measurement mode 3 (MODE[3:0] bits = ”0110”)
   - Sensor is measured periodically in 1 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(6) Continuous measurement mode 4 (MODE[3:0] bits = ”1000”)
   - Sensor is measured periodically in 10 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(7) Continuous measurement mode 5 (MODE[3:0] bits = ”1010”)
   - Sensor is measured periodically in 20 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(8) Continuous measurement mode 6 (MODE[3:0] bits = ”1100”)
   - Sensor is measured periodically in 50 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.
(9) Continuous measurement mode 7 (MODE[3:0] bits = ”1110”)
   - Sensor is measured periodically in 100 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

By setting CNTL2 registers MODE[3:0] bits, the operation set for each mode is started.
When power is turned ON and reset action, AK09970N is in Power-down mode. When a specified value is set to MODE[3:0] bits, AK09970N transits to the specified mode and starts operation. Refer to Figure 9.1.

10.2.1. Description of Each Operation Mode

10.2.1.1. Power-down Mode

Power to almost all internal circuits is turned off, all registers are accessible in Power-down mode and data stored in read/write registers still remains. They can be reset by soft reset function.

10.2.1.2. **Single Measurement Mode**

When Single measurement mode (MODE[3:0] bits = “0001”) is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers (HX, HY and HZ registers), then AK09970N transits to Power-down mode automatically. On transition to Power-down mode, MODE[3:0] bits turns to “0000”. At the same time, DRDY bit in ST register turns to “1” and SW bits in ST register turns to another state when measurement magnetic data exceed a setup threshold value. Refer to 9.1, 9.3 and 9.4.

10.2.1.3. **Continuous Measurement Mode 1,2,3,4,5,6 and 7**

When Continuous measurement modes (1 to 7) are set, magnetic sensor measurement is started periodically at 0.25 Hz, 0.5 Hz, 1 Hz, 10 Hz, 20 Hz, 50 Hz and 100Hz respectively. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers and all circuits except for the minimum circuit required for counting cycle length are turned off (Power Save: PS). When the next measurement timing comes, AK09970N wakes up automatically from PS and starts measurement again.

Continuous measurement mode ends when a different operation mode is set or threshold value is reset. It repeats measurement until other operation mode is set or threshold value is reset. When user access to Setting Registers (address 20h to 27h), AK09970N stops updating switch states and measurement data registers. After CNTL2 register (address 21h) is set again, a new measurement starts. ST register (without DRDY bit and DOR bit) and measurement data registers will not be initialized by this. Refer to 9.1, 9.3 and 9.4.

Table 10.1 Continuous measurement modes

Operation mode	Register setting (MODE[3:0] bits)	Measurement frequency [Hz]
Continuous measurement mode 1	0010	0.25
Continuous measurement mode 2	0100	0.5
Continuous measurement mode 3	0110	1
Continuous measurement mode 4	1000	10
Continuous measurement mode 5	1010	20
Continuous measurement mode 6	1100	50
Continuous measurement mode 7	1110	100

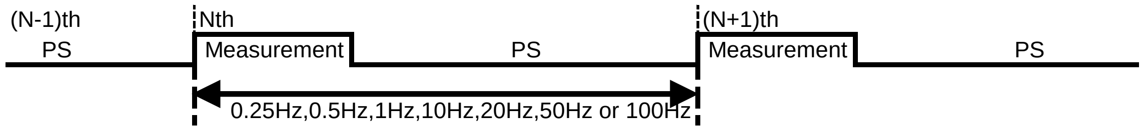


Figure 10.1 Continuous measurement modes

10.3. **Data Ready**

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When DRDYEN bit in CNTL1 register is ”1”, INT pin and OD-INT pin notify user of the Data Ready state. When any of measurement data register (HX,HY or/and HZ register) is read all the way through or access to Setting Registers (address 20h to 27h), DRDY bit turns to “0”. Refer to 9.1, 9.3 and 9.4. When measurement is performed correctly, AK09970N becomes Data Ready on transition to PS after measurement.

10.3.1. Normal Measurement Data Read Sequence

(1) Check Data Ready or not by any of the following method.
Monitor INT or OD-INT pin
Polling DRDY bit of ST register
When Data Ready, proceed to the next step.

(2) Read ST and measurement data
When ST register and any of measurement data register (HX,HY or/and HZ) is read all the way through, or access to Setting Registers (address 20h to 27h), AK09970N judges that data reading is finished. When data reading is finished, DRDY bit and DOR bit turns to “0”.

When measurement data register is accessed, AK09970N judges that data reading is started. Stored measurement data is protected during data reading and data is not updated. By reading measurement data register is finished, this protection is released.

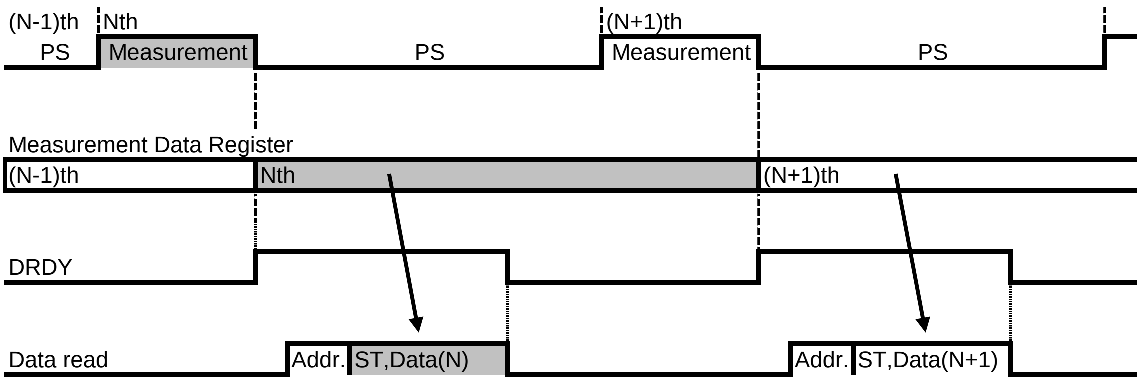


Figure 10.2 Timing chart of Measurement data read

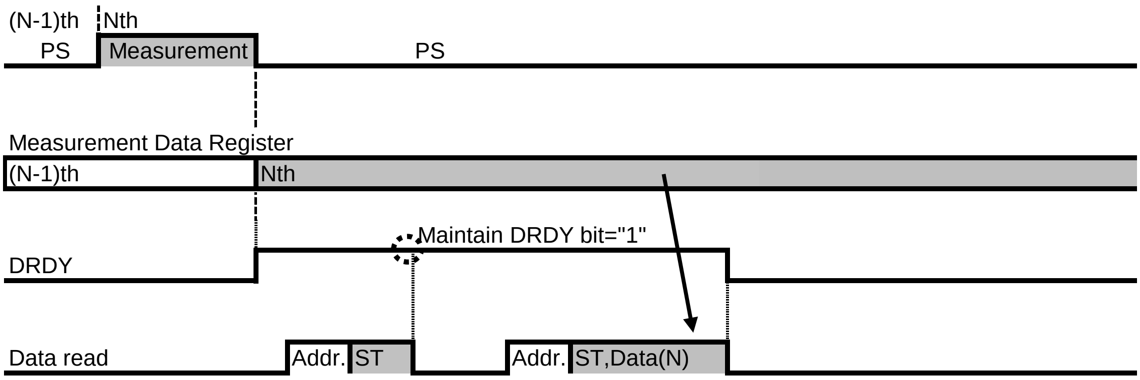


Figure 10.3 Timing chart of ST data read

10.3.2. Data Read Start during Measurement

When the sensor is measuring (Measurement period), measurement data registers (HX, HY and HZ) keep the previous data. Therefore, it is possible to read out data even during the in measurement period. If data is started to be read during measurement period, previous data is read.

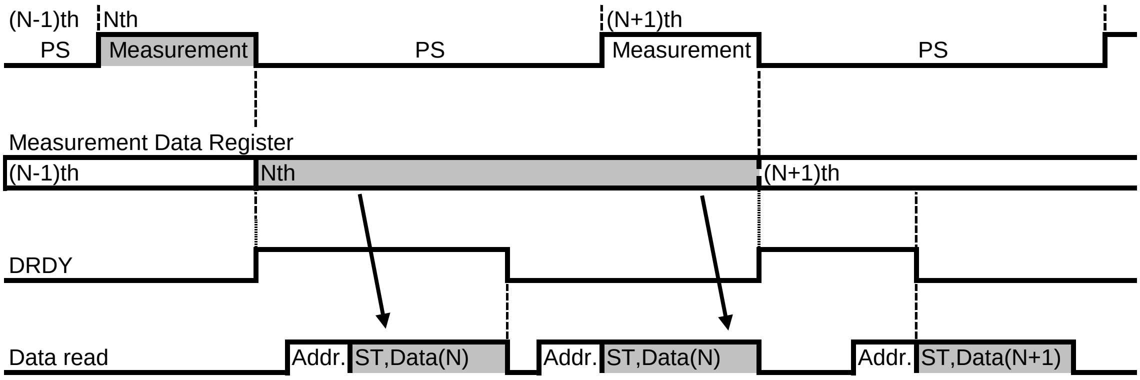


Figure 10.4 Data read start during measuring

10.3.3. Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turns to “1”. DOR bit turns to “0” at the (N+2)th measurement ended.

When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is not skipped and stored after finish reading Nth measurement data so that DOR bit = “0”.

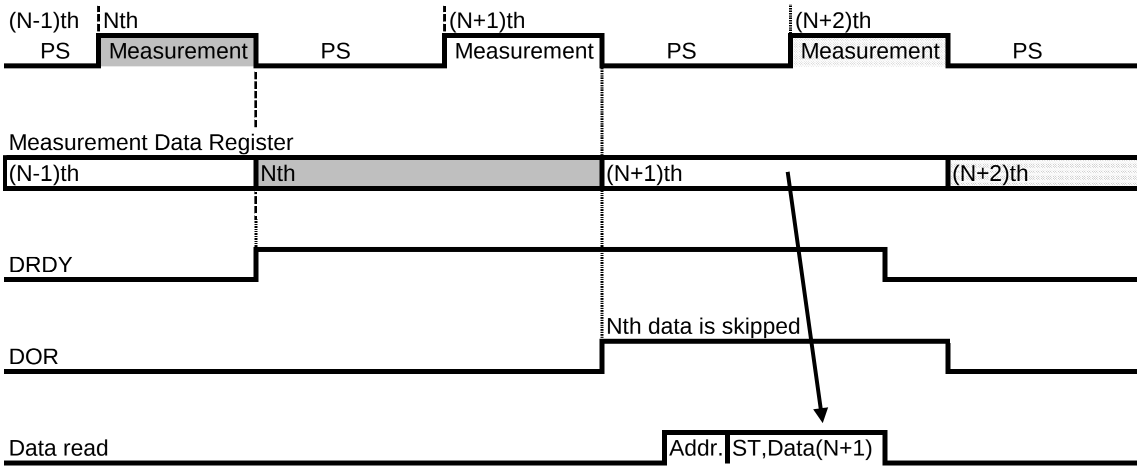


Figure 10.5 Data Skip: When data is not read

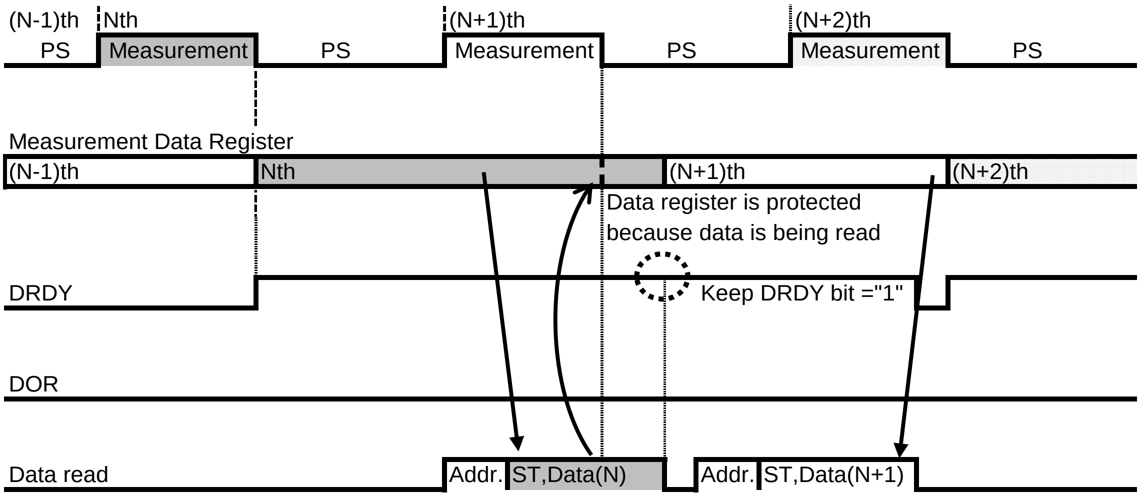


Figure 10.6 Data Not Skip: When data read has not been finished before the next measurement end

10.3.4. End Operation
Set Power-down mode (MODE[3:0] bits = “0000”) to end Continuous measurement mode.

10.4. **Programmable Switch Function**

AK09970N has a programmable switch function created by setting switch threshold values (operating threshold[* 11] and returning threshold[* 12]), switch function enable. When measurement magnetic data exceed the operating threshold value, switch event bit (SW bits[* 13]) turns to “1”. When measurement magnetic data is lower than the returning threshold, SW bits turns to “0”. The switch function is used to check the magnitude relation between the measurement data and the switch threshold values. After the magnetic sensor measurement and signal processing has finished, measurement data is stored to the measurement data register. Then the AK09970N compares the measurement data with the defined switch threshold values and outputs the comparison result at the SW bits in ST register. Switch thresholds can be free to set (Settable range: same as measurement range. Settable sensitivity: same as measurement sensitivity). Refer to Table 10.2 and Figure 10.7.

Note:
* 11. BOPX1[15:0], BOPX2[15:0], BOPY1[15:0], BOPY2[15:0], BOPZ1[15:0] and BOPZ2[15:0]
* 12. BRPX1[15:0], BRPX2[15:0], BRPY1[15:0], BRPY2[15:0], BRPZ1[15:0] and BRPZ2[15:0]
* 13. SWX1 bit, SWX2 bit, SWY1 bit, SWY2 bit, SWZ1 bit and SWZ2 bit

Table 10.2 Relation between threshold values and SWX1 bit[* 14]

Relation between BOPX1 and BRPX1	Magnitude relation between measurement data and threshold values	SWX1 bit result
BOPX1 ≤ BRPX1 (Switch function disable)	Don't care	Don't care
BOPX1 > BRPX1 (Switch function enable)	BOPX1 < HX	1
	BRPX1 > HX	0
	Other relations	Previous result

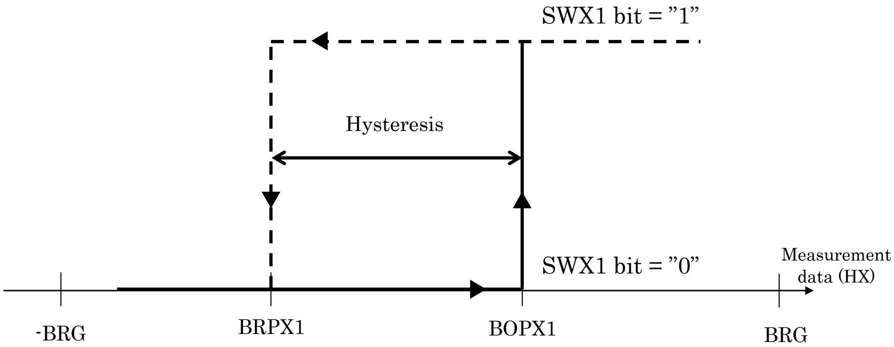


Figure 10.7 Relation between threshold values and SWX1 bit[* 14]

Note:
* 14. SWX1 bit, SWY1 bit, SWZ1 bit, SWX2 bit, SWY2 bit and SWZ2 bit exhibits the same relationship

10.5. **Error Notification Function**

10.5.1. Magnetic Sensor Overflow

AK09970N has a limitation for measurement range, where the absolute value of X-axis and Y-axis should be smaller than 36.04 mT (High sensitivity mode) or 34.91 mT (Wide range mode). When the magnetic field exceeds this limitation, AK09970N outputs limitation value at the X-axis or/and Y-axis (fixed value: 36.04 mT or 34.91 mT). This is called magnetic sensor overflow. When magnetic sensor overflow occurs, ERRXY bit turns to "1". When the magnetic field less than limitation value, measurement data register (HX and HY) and ERRXY bit are updated.

10.5.2. ADC Overflow

AK09970N has a limitation for ADC range, when the magnetic field exceeded this limitation, data stored at measurement data registers (HX, HY and HZ) are not correct. This is called ADC overflow. When ADC overflow occurs, ERRADC bit turns to "1".When measurement data registers are updated, ERRADC bit is updated.

10.6. **Interrupt Function**

AK09970N has two interrupt pins, INT pin (CMOS) and OD-INT pin (Open-drain). When CNTL1 register is set and interrupt event (magnetic event) occurred, AK09970N outputs selected interrupt event at the INT pin or/and OD-INT pin. AK09970N can output four type of interrupt event (Data ready, Magnetic sensor overflow, ADC overflow and Switch event) to pins. INTEN bit and ODINTEN bit can select interrupt function be enabled or disabled. When set INTEN bit/ODINTEN bit ="1" and magnetic event occurs, INT pin turn to "H" and OD-INT pin turn to "L".

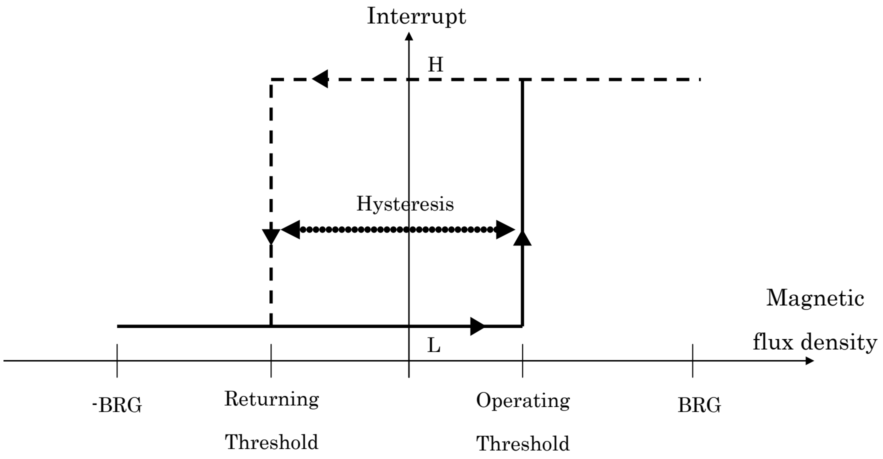


Figure 10.8 Interrupt pin

Table 10.3 Interrupt event and interrupt function

Content of interrupt event	**Conditions of event**	**INTEN bit**	**ODINTEN bit**	**INT pin output**	**OD-INT pin output**
Data ready (Refer to 10.3)	DRDYEN bit = "1", DRDY bit = "1"	0	0	L	H
			1	L	L
		1	0	H	H
			1	H	L
Magnetic sensor Overflow (Refer to 10.5.1)	ERRXYEN bit ="1", ERRXY bit = "1"	0	0	L	H
			1	L	L
		1	0	H	H
			1	H	L
ADC overflow (Refer to 10.5.2)	ERRADCEN bit ="1", ERRADC bit = "1"	0	0	L	H
			1	L	L
		1	0	H	H
			1	H	L
Switch event (Refer to 10.4)	SWEN bit[* 15] ="1", SW bit[* 16] : "0"→"1" or "1"→"0"	0	0	L	H
			1	L	L
		1	0	H	H
			1	H	L
-	Other than those above condition	Don't care	Don't care	L	H

Note:
* 15. SWX1EN bit, SWY1EN bit, SWZ1EN bit, SWX2EN bit, SWY2EN bit and/or SWZ2EN bit
* 16. SWX1 bit, SWX2 bit, SWY1 bit, SWY2 bit, SWZ1 bit and/or SWZ2 bit

10.6.1. Timing of Interrupt Function Operation

Timing of interrupt function operation is given below. Refer to Table 10.4, Figure 10.9 and Figure 10.10.

Table 10.4 Timing of interrupt function operation

Pin name	Output transition	Timing of transition	Remarks
INT pin	L → H	End of measurement	-
	H → L	Read address 10h -1Fh or Write address 20h - 27h	During access to address, INT pin is always “L” state.
OD-INT pin	H → L	End of measurement	-
	L → H	Read address 10h - 1Fh or Write address 20h - 27h	During access to address, OD-INT pin is always “H” state.

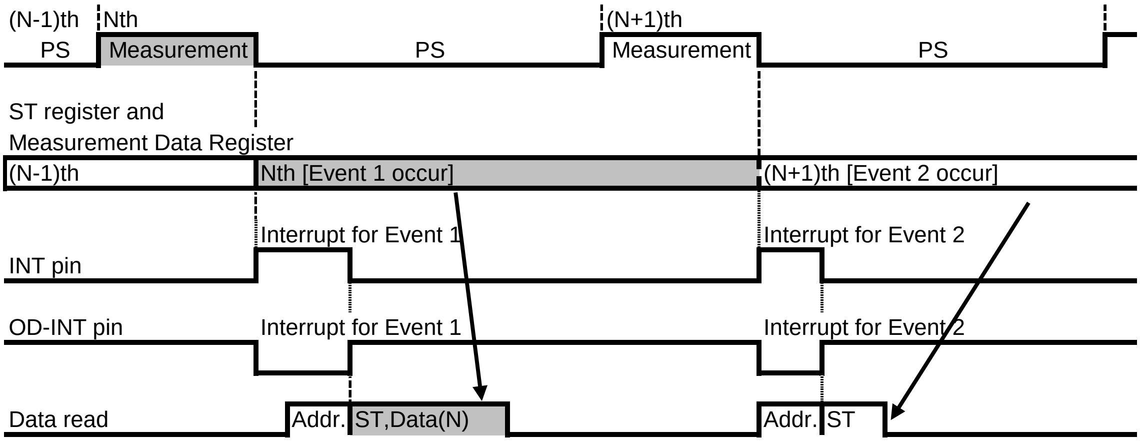


Figure 10.9 Timing chart of interrupt function (Normal read sequence)

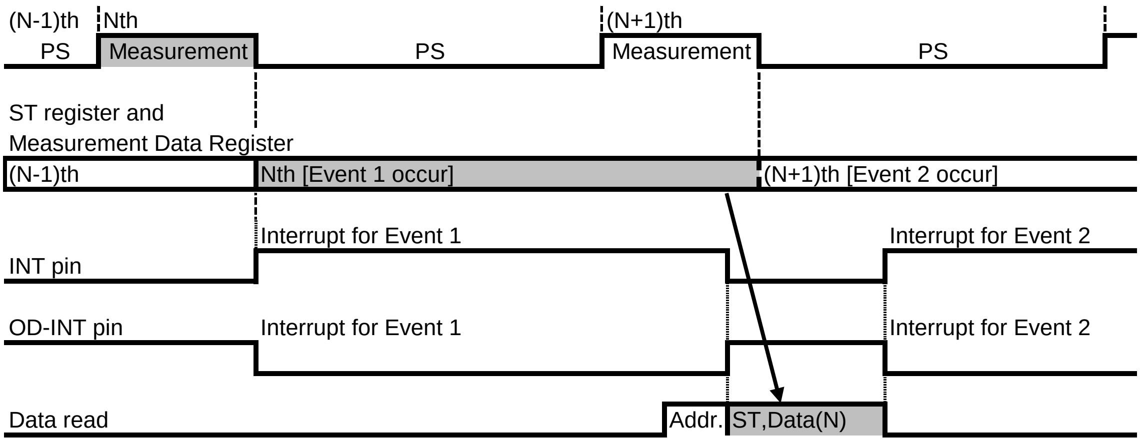


Figure 10.10 Timing chart of interrupt function
(When Nth data is read start immediately before (N+1)th measurement end)

10.7. **Sensor Drive Select**

Users can choose “Low power” or “Low noise” drive by the SDR bit.
“Low power” is used to save the current consumption and “Low noise” is used to reduce the noise of the AK09970N. When Low noise (SDR bit = “0”) is set, output magnetic data noise is more reduced than Low power (about 70% of Low power). When Low power (SDR bit = “1”) is set, average current consumption at 10 Hz repetition rate is saved from 12.0 µA to 3.2 µA (VDD=1.8V, +25˚C). Default SDR bit is Low noise enable (SDR bit = “0”).

10.8. **Sensor Measurement Range and Sensitivity Select**

Users can choose “High sensitivity (Normal measurement range and high sensitivity)” or “Wide range (Wide measurement range and normal sensitivity)” setting.
“High sensitivity” is used to measure with high magnetic sensitivity and “Wide range” is used to measure strong magnetic field (apply only to Z-axis). When High sensitivity (SMR bit = “0”) is set, magnetic sensor sensitivity is about three times higher than Wide range (3.1 µT/LSB → 1.1µT/LSB). When Wide range (SMR bit = “1”) is set, Z-axis measurement range is about three times wider than High sensitivity (Z-axis measurement range:±36.04 mT → ±101.57 mT). Default SMR bit is High sensitivity enable (SMR bit = “0”).

11. Serial Interface

AK09970N supports I2C bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.

CSB pin = “L”: 4-wire SPI
CSB pin = “H”: I2C bus interface

11.1. 4-wire SPI

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB, and is provided in 16bit protocol. Data consists of Read/Write control bit (R/W), register address (7-bit) and control data (8-bit). To read out all axes measurement data (X, Y, Z), an option to read out more than one byte data using automatic increment command is available. (Sequential read operation)

CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI-mode3)
Communication starts when CSB pin transits to “L” and stops when CSB pin transits to “H”. SK pin must be “H” during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is “H” and SK pin is “H”.

11.1.1. Writing Data

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8-bit specify the R/W control bit (R/W = “0” when writing) and register address (7-bit), and the latter 8-bit are control data (8-bit). When any of addresses listed on Table 12.2 is input, AK09970N recognizes that it is selected and takes in latter 8-bit as setting data.
If the number of clock pulses is less than 16, no data is written. It is compliant with serial write operation for multiple addresses. AK09970N has one increment line; 20h to 27h. AK09970N increments as follows: 20h → 21h → 22h → 23h ... → 27h → 20h → 21h … .

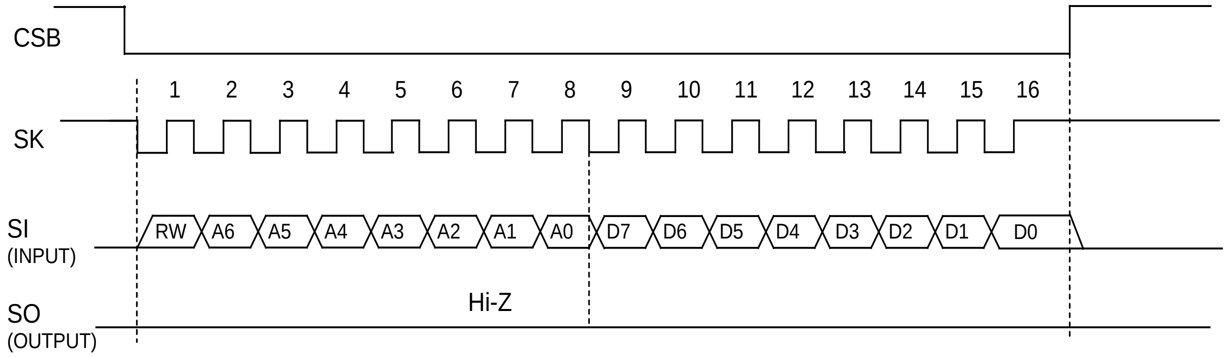


Figure 11.1 4-wire SPI writing data

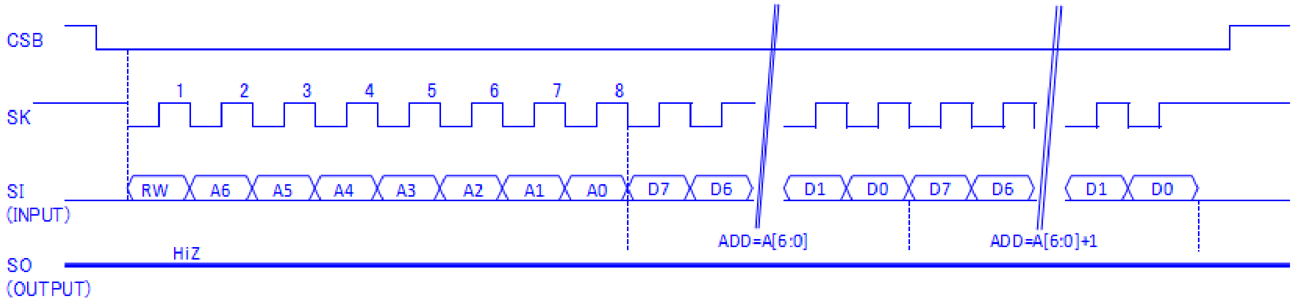


Figure 11.2 4-wire SPI serial writing data

11.1.2. Reading Data

Input the R/W control bit (R/W = “1”) and 7-bit register address on SI pin in synchronous with the first 8-bit of the 16 bits of a serial clock input on SK pin. Then AK09970N outputs the data held in the specified register with MSB first from SO pin.
When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 15th clock and CSB pin is “L”, the data in the next address is output on SO pin. When CSB pin is driven “L” to “H”, SO pin is placed in the high-impedance state.
AK09970N has one increment line; 20h to 27h. AK09970N increments as follows: 20h → 21h → 22h → 23h ... → 27h → 20h → 21h … .

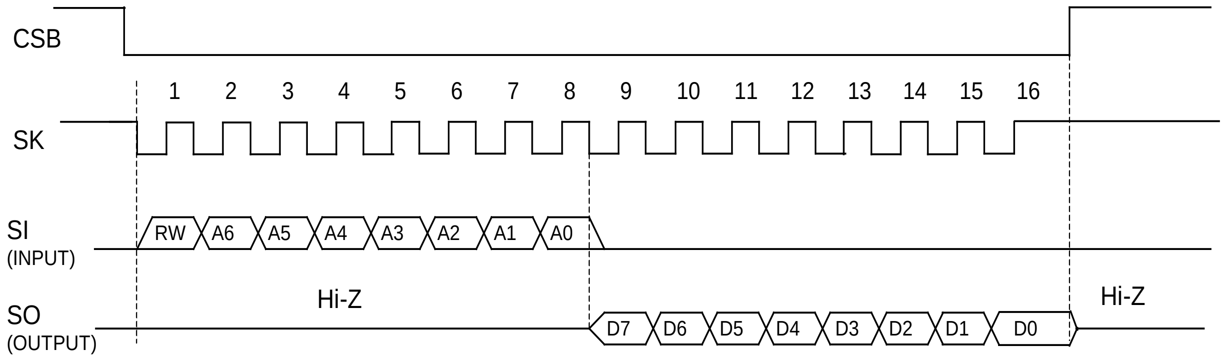


Figure 11.3 4-wire SPI reading data

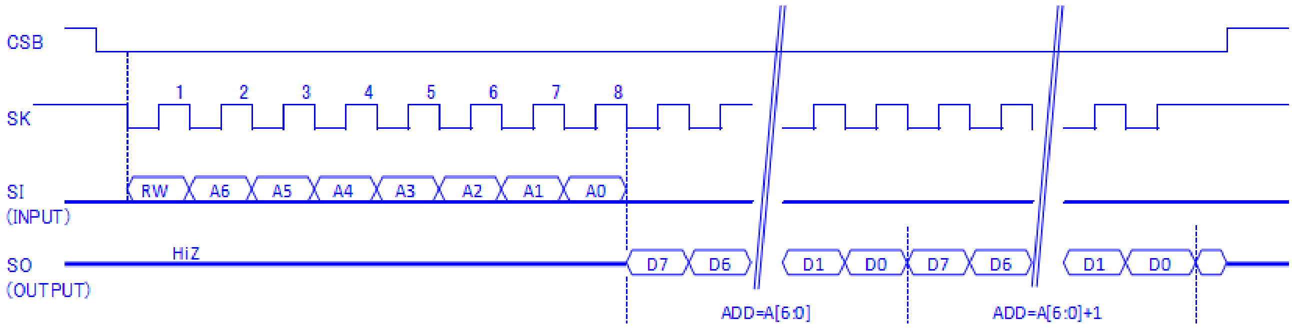


Figure 11.4 4-wire SPI serial reading data

11.2. I²C Bus Interface

The I2C bus interface of AK09970N supports the Standard mode (100 kHz max.) and the Fast mode (400 kHz max.).

11.2.1. Data Transfer

To access AK09970N on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, AK09970N compares the slave address with its own address. If these addresses match, AK09970N generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

11.2.1.1. Change of Data

A change of data on the SDA line must be made during “Low” period of the clock on the SCL line. When the clock signal on the SCL line is “High”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is “Low”.)
During the SCL line is “High”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

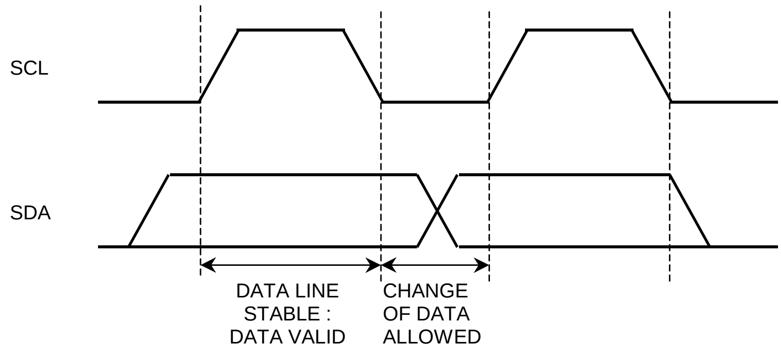


Figure 11.5 Data Change

11.2.1.2. **Start/Stop Condition**

If the SDA line is driven to "Low" from "High" when the SCL line is "High", a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to "High" from "Low" when the SCL line is "High", a stop condition is generated. Every instruction stops with a stop condition.

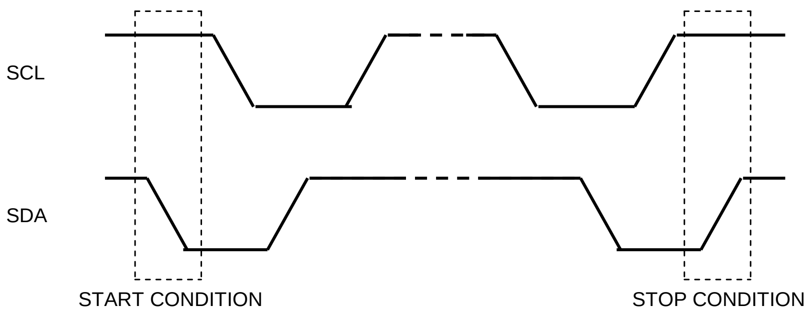


Figure 11.6 Start and stop condition

11.2.1.3. **Acknowledge**

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data. The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred as an acknowledge. With this operation, whether data has been transferred successfully can be checked. AK09970N generates an acknowledge after receipt of the start condition and slave address.
When a WRITE instruction is executed, AK09970N generates an acknowledge after every byte that is received.
When a READ instruction is executed, AK09970N generates an acknowledge then transfers the data stored at the specified address. Next, AK09970N releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK09970N transmits the 8-bit data stored at the next address. If no acknowledge is generated, AK09970N stops data transmission.

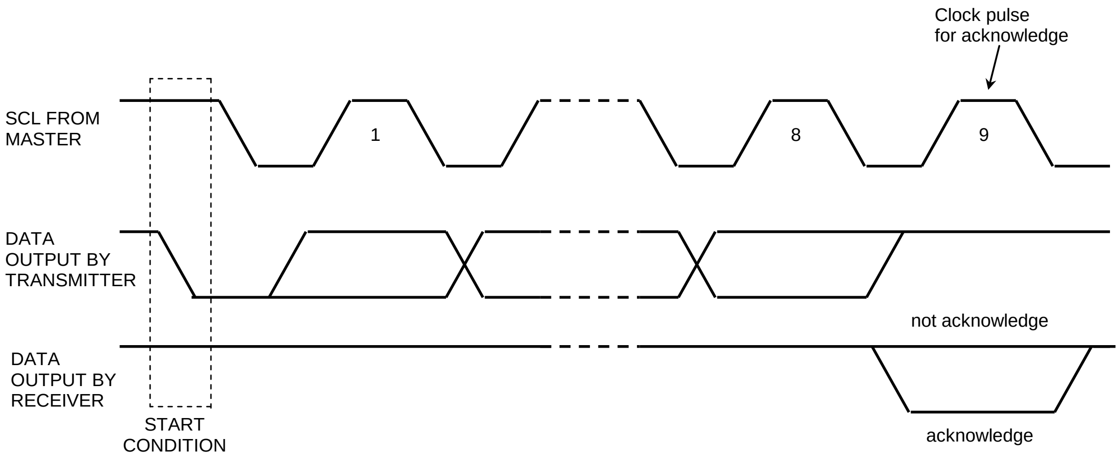


Figure 11.7 Generation of acknowledge

11.2.1.4. **Slave Address**

The slave address of AK09970N can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0“. When CAD pin is fixed to VDD, the corresponding slave address bit is “1”.

Table 11.1 Slave address and CAD pin

CAD	Slave Address
0	0Ch
1	0Dh

MSB							LSB
0	0	0	1	1	0	CAD	R/W

Figure 11.8 Slave address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to “1“, READ instruction is executed. When the R/W bit is set to “0“, WRITE instruction is executed.

11.2.2. WRITE Instruction

When the R/W bit is set to “0”, AK09970N performs write operation.
In write operation, AK09970N generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

Figure 11.9 Register address

After receiving the second byte (register address), AK09970N generates an acknowledge then receives the third byte.

The third and the following bytes represent control data. Control data consists of 8-bit and is based on the MSB-first configuration. AK09970N generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Figure 11.10 Control data

AK09970N can write multiple bytes of data at a time.
After reception of the third byte (control data), AK09970N generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.
The address is incremented from 20h to 27h. When the address is between 20h and 27h, the address is incremented 20h → 21h → 22h → 23h ... → 27h, and the address goes back to 20h after 27h.
Actual data is written only to Read/Write registers (Table 12.2)

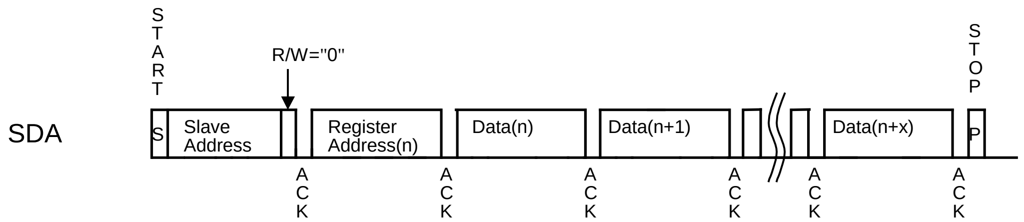


Figure 11.11 WRITE Instruction

11.2.3. READ Instruction

When the R/W bit is set to “1”, AK09970N performs read operation.
If a master IC generates an acknowledge instead of a stop condition after AK09970N transfers the data at a specified address, the data at the next address can be read.
Address can be 20h to 27h. When the address is between 20h and 27h, the address is incremented 20h → 21h → 22h → 23h ... → 27h, and the address goes back to 20h after 27h.
AK09970N supports one byte read and multiple byte read.

11.2.3.1. **Current Address Read**

AK09970N has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read.
In current address read operation, AK09970N generates an acknowledge after receiving a slave address for the READ instruction (R/W bit = “1”). Next, AK09970N transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK09970N transmits one byte of data, the read operation stops.

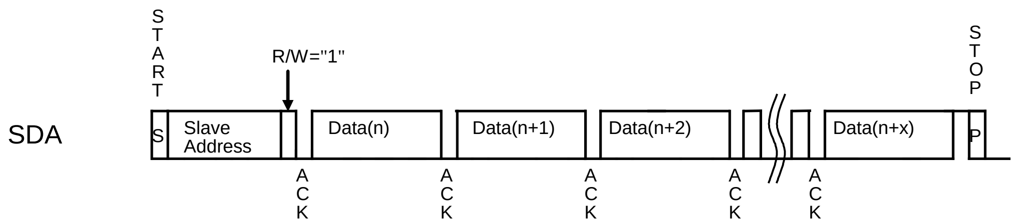


Figure 11.12 Current address read

11.2.3.2. **Random Address Read**

By random address read operation, data at an arbitrary address can be read.

The random address read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit = "1") is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit = "0") and a read address are transmitted sequentially.

After AK09970N generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit = "1") are generated again. AK09970N generates an acknowledge in response to this slave address transmission. Next, AK09970N transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

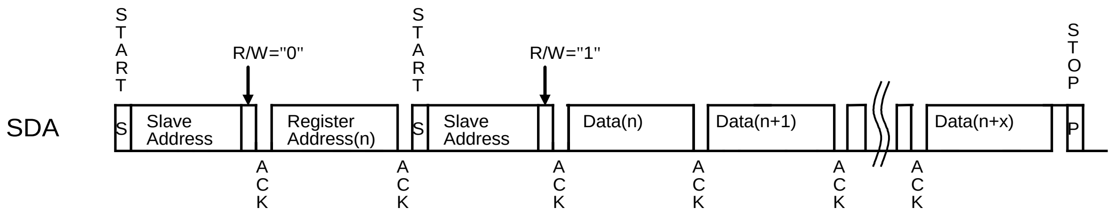


Figure 11.13 Random address read

12. Registers

12.1. Description of Registers

AK09970N has registers of 29 addresses as indicated in Table 12.1. Every address consists of 1-byte to 8-byte data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 12.1 Register Table

Address	READ/ WRITE	Description	Byte width	Remarks
00H	READ	Company ID, Device ID	4	Device Information
10H		Status	2	ST data
11H		Status and Measurement Magnetic Data	4	ST + X-axis data
12H			4	ST + Y-axis data
13H			6	ST + X and Y-axis data
14H			4	ST + Z-axis data
15H			6	ST + X and Z-axis data
16H			6	ST + Y and Z-axis data
17H			8	ST + X,Y and Z-axis data
18H		Status and Measurement Magnetic Data (upper 8 bits of measurement data register)	2	ST data
19H			3	ST + X-axis data
1AH			3	ST + Y-axis data
1BH			4	ST + X and Y-axis data
1CH			3	ST + Z-axis data
1DH			4	ST + X and Z-axis data
1EH			4	ST + Y and Z-axis data
1FH			5	ST + X,Y and Z-axis data
20H	READ/ WRITE	Control 1	2	Interrupt function settings
21H		Control 2	1	Operation Mode, Sensor Drive, Measurement Range and Sensitivity
22H		Control 3 (Switch threshold value)	4	X-axis threshold 1 settings
23H			4	X-axis threshold 2 settings
24H			4	Y-axis threshold 1 settings
25H			4	Y-axis threshold 2 settings
26H			4	Z-axis threshold 1 settings
27H			4	Z-axis threshold 2 settings
30H		Reset	1	Soft reset
31H		I2C disable	1	
40H		Test	2	DO NOT ACCESS
41H			1	DO NTO ACCESS

Addresses 20h to 27h are compliant with automatic increment function of serial interface respectively. When the address is in 20h to 27h, the address is incremented 20h → 21h → 22h → 23h ... → 27h, and the address goes back to 20h after 27h.

12.2. **Register Map**

Table 12.2 Register Map

Addr.	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
Read only register								
00H	WIA[15:8]	WIA[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
10H	ST[15:8]	ST[7:0]	-	-	-	-	-	-
11H	ST[15:8]	ST[7:0]	HX[15:8]	HX[7:0]	-	-	-	-
12H	ST[15:8]	ST[7:0]	HY[15:8]	HY[7:0]	-	-	-	-
13H	ST[15:8]	ST[7:0]	HY[15:8]	HY[7:0]	HX[15:8]	HX[7:0]	-	-
14H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	-	-	-	-
15H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HX[15:8]	HX[7:0]	-	-
16H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HY[15:8]	HY[7:0]	-	-
17H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HY[15:8]	HY[7:0]	HX[15:8]	HX[7:0]
18H	ST[15:8]	ST[7:0]	-	-	-	-	-	-
19H	ST[15:8]	ST[7:0]	HX[15:8]	-	-	-	-	-
1AH	ST[15:8]	ST[7:0]	HY[15:8]	-	-	-	-	-
1BH	ST[15:8]	ST[7:0]	HY[15:8]	HX[15:8]	-	-	-	-
1CH	ST[15:8]	ST[7:0]	HZ[15:8]	-	-	-	-	-
1DH	ST[15:8]	ST[7:0]	HZ[15:8]	HX[15:8]	-	-	-	-
1EH	ST[15:8]	ST[7:0]	HZ[15:8]	HY[15:8]	-	-	-	-
1FH	ST[15:8]	ST[7:0]	HZ[15:8]	HY[15:8]	HX[15:8]	-	-	--
Read/Write register								
20H	CNTL1[15:8]	CNTL1[7:8]	-	-	-	-	-	-
21H	CNTL2[7:0]	-	-	-	-	-	-	-
22H	BOP1X[15:8]	BOP1X[7:0]	BRP1X[15:8]	BRP1X[7:0]	-	-	-	-
23H	BOP2X[15:8]	BOP2X[7:0]	BRP2X[15:8]	BRP2X[7:0]	-	-	-	-
24H	BOP1Y[15:8]	BOP1Y[7:0]	BRP1Y[15:8]	BRP1Y[7:0]	-	-	-	-
25H	BOP2Y[15:8]	BOP2Y[7:0]	BRP2Y[15:8]	BRP2Y[7:0]	-	-	-	-
26H	BOP1Z[15:8]	BOP1Z[7:0]	BRP1Z[15:8]	BRP1Z[7:0]	-	-	-	-
27H	BOP2Z[15:8]	BOP2Z[7:0]	BRP2Z[15:8]	BRP2Z[7:0]	-	-	-	-
30H	SRST[7:0]	-	-	-	-	-	-	-
31H	I2CDIS[7:0]	-	-	-	-	-	-	-
40H	-	-	-	-	-	-	-	-
41H	-	-	-	-	-	-	-	-

Table 12.3 Further details about Register Map (D[7:0])

Register name	Bit number (D[7:0])							
	7	6	5	4	3	2	1	0
WIA[7:0]	1	1	0	0	0	0	0	0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
ST[7:0]	ERRXY	SWZ2	SWZ1	SWY2	SWY1	SWX2	SWX1	DRDY
HX[7:0]	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
HY[7:0]	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
HZ[7:0]	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
CNTL1[7:0]	ERRXYEN	SWZ2EN	SWZ1EN	SWY2EN	SWY1EN	SWX2EN	SWX1EN	DRDYEN
CNTL2[7:0]	0	0	SMR	SDR	MODE3	MODE2	MODE1	MODE0
BOP1X[7:0]	BOP1X7	BOP1X6	BOP1X5	BOP1X4	BOP1X3	BOP1X2	BOP1X1	BOP1X0
BRP1X[7:0]	BRP1X7	BRP1X6	BRP1X5	BRP1X4	BRP1X3	BRP1X2	BRP1X1	BRP1X0
BOP2X[7:0]	BOP2X7	BOP2X6	BOP2X5	BOP2X4	BOP2X3	BOP2X2	BOP2X1	BOP2X0
BRP2X[7:0]	BRP2X7	BRP2X6	BRP2X5	BRP2X4	BRP2X3	BRP2X2	BRP2X1	BRP2X0
BOP1Y[7:0]	BOP1Y7	BOP1Y6	BOP1Y5	BOP1Y4	BOP1Y3	BOP1Y2	BOP1Y1	BOP1Y0
BRP1Y[7:0]	BRP1Y7	BRP1Y6	BRP1Y5	BRP1Y4	BRP1Y3	BRP1Y2	BRP1Y1	BRP1Y0
BOP2Y[7:0]	BOP2Y7	BOP2Y6	BOP2Y5	BOP2Y4	BOP2Y3	BOP2Y2	BOP2Y1	BOP2Y0
BRP2Y[7:0]	BRP2Y7	BRP2Y6	BRP2Y5	BRP2Y4	BRP2Y3	BRP2Y2	BRP2Y1	BRP2Y0
BOP1Z[7:0]	BOP1Z7	BOP1Z6	BOP1Z5	BOP1Z4	BOP1Z3	BOP1Z2	BOP1Z1	BOP1Z0
BRP1Z[7:0]	BRP1Z7	BRP1Z6	BRP1Z5	BRP1Z4	BRP1Z3	BRP1Z2	BRP1Z1	BRP1Z0
BOP2Z[7:0]	BOP2Z7	BOP2Z6	BOP2Z5	BOP2Z4	BOP2Z3	BOP2Z2	BOP2Z1	BOP2Z0
BRP2Z[7:0]	BRP2Z7	BRP2Z6	BRP2Z5	BRP2Z4	BRP2Z3	BRP2Z2	BRP2Z1	BRP2Z0
SRST[7:0]	0	0	0	0	0	0	0	SRST
I2CDIS[7:0]	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
TEST1[7:0]	-	-	-	-	-	-	-	-
TEST2[7:0]	-	-	-	-	-	-	-	-

Table 12.4 Further details about Register Map (D[15:8])

Register name	Bit number (D[15:8])							
	15	14	13	12	11	10	9	8
WIA[15:8]	0	1	0	0	1	0	0	0
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
ST[15:8]	1	1	1	1	1	1	DOR	ERRADC
HX[15:8]	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
HY[15:8]	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
HZ[15:8]	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
CNTL1[15:8]	0	0	0	0	0	ODINTEN	INTEN	ERRADCEN
CNTL2[15:8]	-	-	-	-	-	-	-	-
BOP1X[15:8]	BOP1X15	BOP1X14	BOP1X13	BOP1X12	BOP1X11	BOP1X10	BOP1X9	BOP1X8
BRP1X[15:8]	BRP1X15	BRP1X14	BRP1X13	BRP1X12	BRP1X11	BRP1X10	BRP1X9	BRP1X8
BOP2X[15:8]	BOP2X15	BOP2X14	BOP2X13	BOP2X12	BOP2X11	BOP2X10	BOP2X9	BOP2X8
BRP2X[15:8]	BRP2X15	BRP2X14	BRP2X13	BRP2X12	BRP2X11	BRP2X10	BRP2X9	BRP2X8
BOP1Y[15:8]	BOP1Y15	BOP1Y14	BOP1Y13	BOP1Y12	BOP1Y11	BOP1Y10	BOP1Y9	BOP1Y8
BRP1Y[15:8]	BRP1Y15	BRP1Y14	BRP1Y13	BRP1Y12	BRP1Y11	BRP1Y10	BRP1Y9	BRP1Y8
BOP2Y[15:8]	BOP2Y15	BOP2Y14	BOP2Y13	BOP2Y12	BOP2Y11	BOP2Y10	BOP2Y9	BOP2Y8
BRP2Y[15:8]	BRP2Y15	BRP2Y14	BRP2Y13	BRP2Y12	BRP2Y11	BRP2Y10	BRP2Y9	BRP2Y8
BOP1Z[15:8]	BOP1Z15	BOP1Z14	BOP1Z13	BOP1Z12	BOP1Z11	BOP1Z10	BOP1Z9	BOP1Z8
BRP1Z[15:8]	BRP1Z15	BRP1Z14	BRP1Z13	BRP1Z12	BRP1Z11	BRP1Z10	BRP1Z9	BRP1Z8
BOP2Z[15:8]	BOP2Z15	BOP2Z14	BOP2Z13	BOP2Z12	BOP2Z11	BOP2Z10	BOP2Z9	BOP2Z8
BRP2Z[15:8]	BRP2Z15	BRP2Z14	BRP2Z13	BRP2Z12	BRP2Z11	BRP2Z10	BRP2Z9	BRP2Z8
SRST[15:8]	-	-	-	-	-	-	-	-
I2CDIS[15:8]	I2CDIS15	I2CDIS14	I2CDIS13	I2CDIS12	I2CDIS11	I2CDIS10	I2CDIS9	I2CDIS8
TEST1[15:8]	-	-	-	-	-	-	-	-
TEST2[15:8]	-	-	-	-	-	-	-	-

When RSTN pin is applied VDD, all registers of AK09970N are initialized.
TEST1 and TEST2 is test register for shipment test. Do not access this register.

12.3. **Detailed Description of Registers**

12.3.1. WIA[15:0]: Company ID and Device ID

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA[7:0]	1	1	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
00h	WIA[15:8]	0	1	0	0	1	0	0	0

WIA[7:0] bits: Device ID of AKM. It is described in one byte and fixed value.
C0h: fixed
WIA[15:8] bits: Company ID of AK09970N. It is described in one byte and fixed value.
48h: fixed

12.3.2. RSV[15:0]: Reserved Register

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
00h	RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8

RSV[7:0] bits/ RSV[15:8] bits: Reserved register for AKM.

12.3.3. ST[15:0]: Status

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h-1fh	ST[7:0]	ERRXY	SWZ2	SWZ1	SWY2	SWY1	SWX2	SWX1	DRDY
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
10h-1fh	ST[15:8]	1	1	1	1	1	1	DOR	ERRADC
Reset		1	1	1	1	1	1	0	0

DRDY bit: Data Ready
"0": Normal
"1": Data is ready

DRDY bit turns to "1" when data is ready in Single measurement mode and Continuous measurement mode 1, 2, 3, 4, 5, 6, and 7. It returns to "0" when any one of measurement data register (HX,HY or/and HZ register) is read all the way through or access to Setting Registers (address 20h to 27h).

DOR bit: Data Overrun
"0": Normal
"1": Data overrun

DOR bit turns to “1” when data has been skipped in Continuous measurement mode 1, 2, 3, 4, 5, 6 or 7.
DOR bit turns to “0” at the after the next measurement ended.

SWX1 bit, SWY1 bit, SWZ1 bit: Measurement data of X, Y and Z-axis exceed switch threshold 1
“0”: Measurement data of X, Y and Z-axis exceed returning threshold 1
“1”: Measurement data of X, Y and Z-axis exceed operating threshold 1

SWX2 bit, SWY2 bit, SWZ2 bit: Measurement data of X, Y and Z-axis exceed switch threshold 2
“0”: Measurement data of X, Y and Z-axis exceed returning threshold 2
“1”: Measurement data of X, Y and Z-axis exceed operating threshold 2

Refer to 10.4 for detailed information.

ERRXY bit: Magnetic sensor overflow
“0”: Normal
“1”: Magnetic sensor overflow occurred (X and/or Y-axis)

Refer to 10.5.1 for detailed information.

ERRADC bit: ADC overflow
“0”: Normal
“1”: ADC overflow occurred and measurement data is not correct

Refer to 10.5.2 for detailed information.

12.3.4. HX[15:0]/HY[15:0]/HZ[15:0]: Measurement Data

Addr.	**Register name**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Read-only register									
10h | 1fh	HX[7:0]	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
	HY[7:0]	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
	HZ[7:0]	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
10h | 1fh	HX[15:8]	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
	HY[15:8]	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
	HZ[15:8]	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
Reset		0	0	0	0	0	0	0	0

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis
HX[7:0] bits: X-axis measurement data lower 8-bit
HX[15:8] bits: X-axis measurement data higher 8-bit
HY[7:0] bits: Y-axis measurement data lower 8-bit
HY[15:8] bits: Y-axis measurement data higher 8-bit
HZ[7:0] bits: Z-axis measurement data lower 8-bit
HZ[15:8] bits: Z-axis measurement data higher 8-bit

Measurement data is stored in two’s complement. Measurement range of each axis is -32768 to 32767 in 16-bit output (High sensitivity setting). Measurement range of X and Y-axis are -11264 to 11264 in 16-bit output, Z-axis is -32768 to 32767 in 16-bit output (Wide range setting).

Table 12.5 Measurement magnetic data format (High sensitivity setting)

Measurement data (each axis) [15:0] bits			Magnetic flux density [mT]	ERRXY bit
Two's complement	Hex	Decimal		
0111 1111 1111 1111	7FFF	32767	>36.0437	1
0111 1111 1111 1111	7FFF	32767	36.0437	0
|	|	|	|	|
0000 0000 0000 0001	0001	1	0.0011	0
0000 0000 0000 0000	0000	0	0	0
1111 1111 1111 1111	FFFF	-1	-0.0011	0
|	|	|	|	|
1000 0000 0000 0000	8000	-32768	-36.0448	0
1000 0000 0000 0000	8000	-32768	<-36.0448	1

Table 12.6 Measurement magnetic data format (Wide range setting, X and Y-axis)

Measurement data (X and Y axis) [15:0] bits			Magnetic flux density [mT]	ERRXY bit
Two's complement	Hex	Decimal		
0010 1100 0000 0000	2C00	11264	>34.9184	1
0010 1100 0000 0000	2C00	11264	34.9184	0
|	|	|	|	|
0000 0000 0000 0001	0001	1	0.0031	0
0000 0000 0000 0000	0000	0	0	0
1111 1111 1111 1111	FFFF	-1	-0.0031	0
|	|	|	|	|
1101 0100 0000 0000	D400	-11264	-34.9184	0
1101 0100 0000 0000	D400	-11264	<-34.9184	1

Table 12.7 Measurement magnetic data format (Wide range setting, Z-axis)

Measurement data (Z axis) [15:0] bits			Magnetic flux density [mT]
Two's complement	Hex	Decimal	
0111 1111 1111 1111	7FFF	32767	>101.5777
0111 1111 1111 1110	7FFE	32766	101.5746
|	|	|	|
0000 0000 0000 0001	0001	1	0.0031
0000 0000 0000 0000	0000	0	0
1111 1111 1111 1111	FFFF	-1	-0.0031
|	|	|	|
1000 0000 0000 0001	8001	-32767	-101.5777
1000 0000 0000 0000	8000	-32768	<-101.5808

12.3.5. CNTL1[15:0]: Interrupt Output Setting

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
20h	CNTL1[7:0]	ERRXYEN	SWZ2EN	SWZ1EN	SWY2EN	SWY1EN	SWX2EN	SWX1EN	DRDYEN
Reset		0	0	0	0	0	0	0	1
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read/Write register									
20h	CNTL1[15:8]	0	0	0	0	0	ODINTEN	INTEN	ERRADCEN
Reset		0	0	0	0	0	1	1	0

DRDYEN bit: DRDY event output
“0”: DRDY event outputs disable
“1”: DRDY event outputs enable

Refer to 10.3 for detailed information.

SWX1EN bit to SWZ2EN bit: Switch event output
“0”: Switch event outputs disable
“1”: Switch event outputs enable

Refer to 10.4 for detailed information.

ERRXYEN bit: ERRXY event output
“0”: ERRXY event outputs disable
“1”: ERRXY event outputs enable

Refer to 10.5.1 for detailed information.

ERRADCEN bit: ERRADC event output
“0”: ERRADC event outputs disable
“1”: ERRADC event outputs enable

Refer to 10.5.2 for detailed information.

INTEN bit: Interrupt event output to INT pin
“0”: Disable (INT pin =”L”)
“1”: Enable

Refer to 10.6 for detailed information.

ODINTEN bit: Interrupt event output to OD-INT pin
“0”: Disable (OD-INT pin =”Hi-Z”)
“1”: Enable

Refer to 10.6 for detailed information.

12.3.6. CNTL2[7:0]: Operation Mode, Sensor Drive, Measurement Range and Sensitivity setting

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
21h	CNTL2[7:0]	0	0	SMR	SDR	MODE3	MODE2	MODE1	MODE0
Reset		0	0	0	0	0	0	0	0

MODE[3:0] bits: Operation mode setting
“0000”: Power-down mode
“0001”: Single measurement mode
“0010”: Continuous measurement mode 1
“0100”: Continuous measurement mode 2
“0110”: Continuous measurement mode 3
“1000”: Continuous measurement mode 4
“1010”: Continuous measurement mode 5
“1100”: Continuous measurement mode 6
“1110”: Continuous measurement mode 7

SDR bit: Sensor drive setting
“0”: Low noise drive
“1”: Low power drive

SMR bit: Measurement range and sensitivity setting
“0”: High sensitivity setting
“1”: Wide measurement range setting

12.3.7. BOP1,2 and BRP1,2 registers: Operating Threshold and Returning Threshold Setting of Programmable Switch Function

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
22h - 27h	BOP1X[7:0]	BOP1X7	BOP1X6	BOP1X5	BOP1X4	BOP1X3	BOP1X2	BOP1X1	BOP1X0
	BRP1X[7:0]	BRP1X7	BRP1X6	BRP1X5	BRP1X4	BRP1X3	BRP1X2	BRP1X1	BRP1X0
	BOP2X[7:0]	BOP2X7	BOP2X6	BOP2X5	BOP2X4	BOP2X3	BOP2X2	BOP2X1	BOP2X0
	BRP2X[7:0]	BRP2X7	BRP2X6	BRP2X5	BRP2X4	BRP2X3	BRP2X2	BRP2X1	BRP2X0
	BOP1Y[7:0]	BOP1Y7	BOP1Y6	BOP1Y5	BOP1Y4	BOP1Y3	BOP1Y2	BOP1Y1	BOP1Y0
	BRP1Y[7:0]	BRP1Y7	BRP1Y6	BRP1Y5	BRP1Y4	BRP1Y3	BRP1Y2	BRP1Y1	BRP1Y0
	BOP2Y[7:0]	BOP2Y7	BOP2Y6	BOP2Y5	BOP2Y4	BOP2Y3	BOP2Y2	BOP2Y1	BOP2Y0
	BRP2Y[7:0]	BRP2Y7	BRP2Y6	BRP2Y5	BRP2Y4	BRP2Y3	BRP2Y2	BRP2Y1	BRP2Y0
	BOP1Z[7:0]	BOP1Z7	BOP1Z6	BOP1Z5	BOP1Z4	BOP1Z3	BOP1Z2	BOP1Z1	BOP1Z0
	BRP1Z[7:0]	BRP1Z7	BRP1Z6	BRP1Z5	BRP1Z4	BRP1Z3	BRP1Z2	BRP1Z1	BRP1Z0
	BOP2Z[7:0]	BOP2Z7	BOP2Z6	BOP2Z5	BOP2Z4	BOP2Z3	BOP2Z2	BOP2Z1	BOP2Z0
	BRP2Z[7:0]	BRP2Z7	BRP2Z6	BRP2Z5	BRP2Z4	BRP2Z3	BRP2Z2	BRP2Z1	BRP2Z0
Reset		1	1	1	1	1	1	1	1
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read/Write register									
22h - 27h	BOP1X[15:8]	BOP1X15	BOP1X14	BOP1X13	BOP1X12	BOP1X11	BOP1X10	BOP1X9	BOP1X8
	BRP1X[15:8]	BRP1X15	BRP1X14	BRP1X13	BRP1X12	BRP1X11	BRP1X10	BRP1X9	BRP1X8
	BOP2X[15:8]	BOP2X15	BOP2X14	BOP2X13	BOP2X12	BOP2X11	BOP2X10	BOP2X9	BOP2X8
	BRP2X[15:8]	BRP2X15	BRP2X14	BRP2X13	BRP2X12	BRP2X11	BRP2X10	BRP2X9	BRP2X8
	BOP1Y[15:8]	BOP1Y15	BOP1Y14	BOP1Y13	BOP1Y12	BOP1Y11	BOP1Y10	BOP1Y9	BOP1Y8
	BRP1Y[15:8]	BRP1Y15	BRP1Y14	BRP1Y13	BRP1Y12	BRP1Y11	BRP1Y10	BRP1Y9	BRP1Y8
	BOP2Y[15:8]	BOP2Y15	BOP2Y14	BOP2Y13	BOP2Y12	BOP2Y11	BOP2Y10	BOP2Y9	BOP2Y8
	BRP2Y[15:8]	BRP2Y15	BRP2Y14	BRP2Y13	BRP2Y12	BRP2Y11	BRP2Y10	BRP2Y9	BRP2Y8
	BOP1Z[15:8]	BOP1Z15	BOP1Z14	BOP1Z13	BOP1Z12	BOP1Z11	BOP1Z10	BOP1Z9	BOP1Z8
	BRP1Z[15:8]	BRP1Z15	BRP1Z14	BRP1Z13	BRP1Z12	BRP1Z11	BRP1Z10	BRP1Z9	BRP1Z8
	BOP2Z[15:8]	BOP2Z15	BOP2Z14	BOP2Z13	BOP2Z12	BOP2Z11	BOP2Z10	BOP2Z9	BOP2Z8
	BRP2Z[15:8]	BRP2Z15	BRP2Z14	BRP2Z13	BRP2Z12	BRP2Z11	BRP2Z10	BRP2Z9	BRP2Z8
Reset		0	1	1	1	1	1	1	1

Operating threshold data of magnetic sensor X-axis/Y-axis/Z-axis
BOPX1[7:0] bits: X-axis operating threshold 1 data lower 8-bit
BOPX1[15:8] bits: X-axis operating threshold 1 data higher 8-bit
BOPY1[7:0] bits: Y-axis operating threshold 1 data lower 8-bit
BOPY1[15:8] bits: Y-axis operating threshold 1 data higher 8-bit
BOPZ1[7:0] bits: Z-axis operating threshold 1 data lower 8-bit
BOPZ1[15:8] bits: Z-axis operating threshold 1 data higher 8-bit
BOPX2[7:0] bits: X-axis operating threshold 2 data lower 8-bit
BOPX2[15:8] bits: X-axis operating threshold 2 data higher 8-bit
BOPY2[7:0] bits: Y-axis operating threshold 2 data lower 8-bit
BOPY2[15:8] bits: Y-axis operating threshold 2 data higher 8-bit
BOPZ2[7:0] bits: Z-axis operating threshold 2 data lower 8-bit
BOPZ2[15:8] bits: Z-axis operating threshold 2 data higher 8-bit

Returning threshold data of magnetic sensor X-axis/Y-axis/Z-axis
BRPX1[7:0] bits: X-axis returning threshold 1 data lower 8-bit
BRPX1[15:8] bits: X-axis returning threshold 1 data higher 8-bit
BRPY1[7:0] bits: Y-axis returning threshold 1 data lower 8-bit
BRPY1[15:8] bits: Y-axis returning threshold 1 data higher 8-bit
BRPZ1[7:0] bits: Z-axis returning threshold 1 data lower 8-bit
BRPZ1[15:8] bits: Z-axis returning threshold 1 data higher 8-bit
BRPX2[7:0] bits: X-axis returning threshold 2 data lower 8-bit
BRPX2[15:8] bits: X-axis returning threshold 2 data higher 8-bit
BRPY2[7:0] bits: Y-axis returning threshold 2 data lower 8-bit
BRPY2[15:8] bits: Y-axis returning threshold 2 data higher 8-bit
BRPZ2[7:0] bits: Z-axis returning threshold 2 data lower 8-bit
BRPZ2[15:8] bits: Z-axis returning threshold 2 data higher 8-bit

AK09970N can set Operating and Returning threshold in two's complement. It follows the same format as Measurement data. Switch thresholds can be free to set (Settable range: same as measurement range. Settable sensitivity: same as measurement sensitivity). Please refer to 12.3.4.

12.3.8. SRST[7:0]: Soft Reset

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
30h	SRST[7:0]	0	0	0	0	0	0	0	SRST
Reset		0	0	0	0	0	0	0	0

SRST bit: Soft reset
"0": Normal
"1": Reset

When "1" is set, all registers are initialized. After reset, SRST bit turns to "0" automatically.

12.3.9. I2CDIS[7:0]: I^{2}C Disable

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
31h	I2CDIS[7:0]	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
Reset		0	0	0	0	0	0	0	0

This register disables I^{2}C bus interface. I^{2}C bus interface is enabled in default. To disable I^{2}C bus interface, write "00011011" to I2CDIS[7:0] bits. Then I^{2}C bus interface is disabled.
Once I^{2}C bus interface is disabled, it is impossible to write other value to I2CDIS register. To enable I^{2}C bus interface, reset AK09970N or input start condition 8 times continuously.

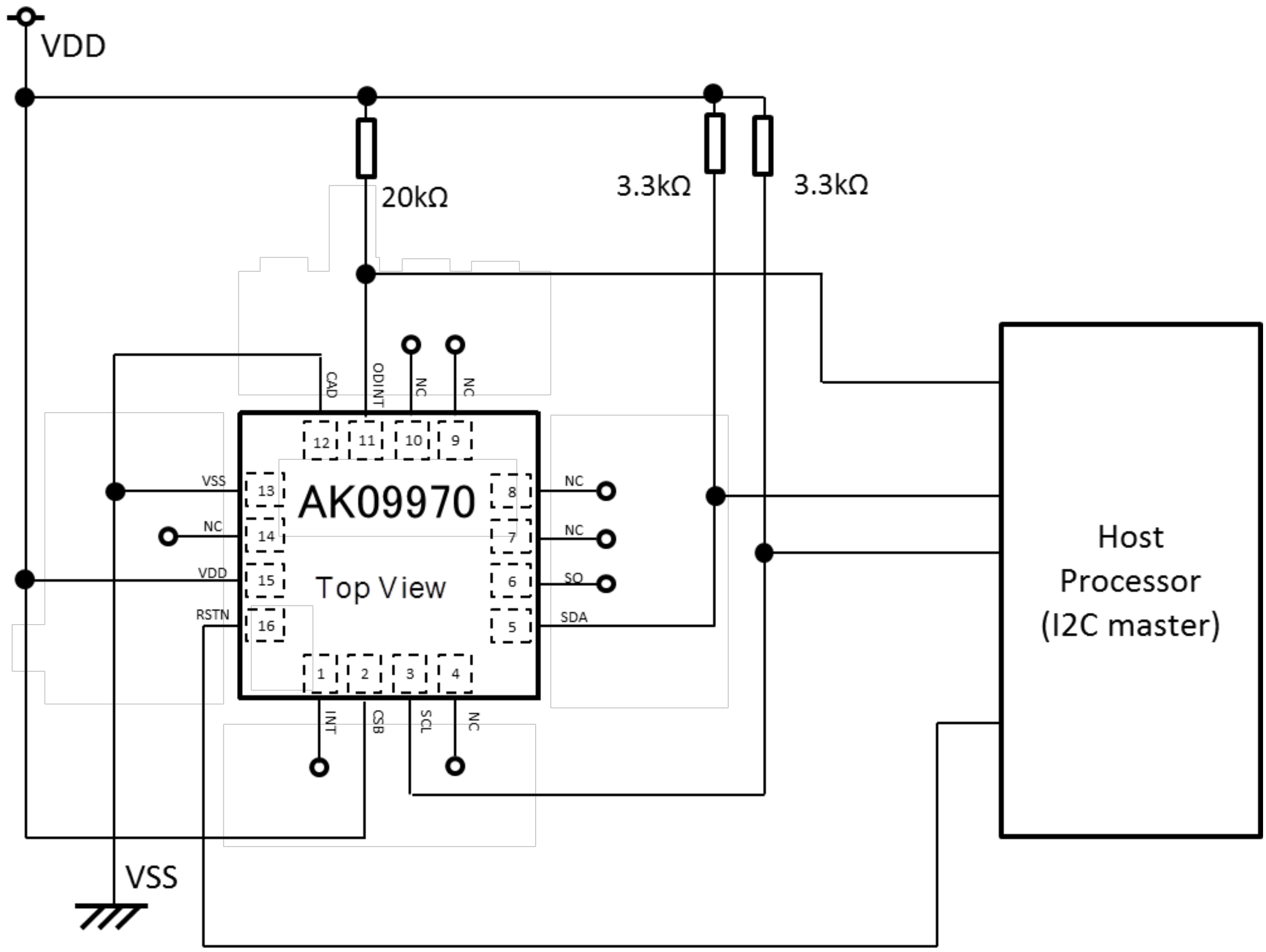
12.3.10. TST1[15:0]/TST2[7:0]: Test register

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
40h	TST1	-	-	-	-	-	-	-	-
41h	TST2	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read/Write register									
40h	TST1	-	-	-	-	-	-	-	-
41h	TST2	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

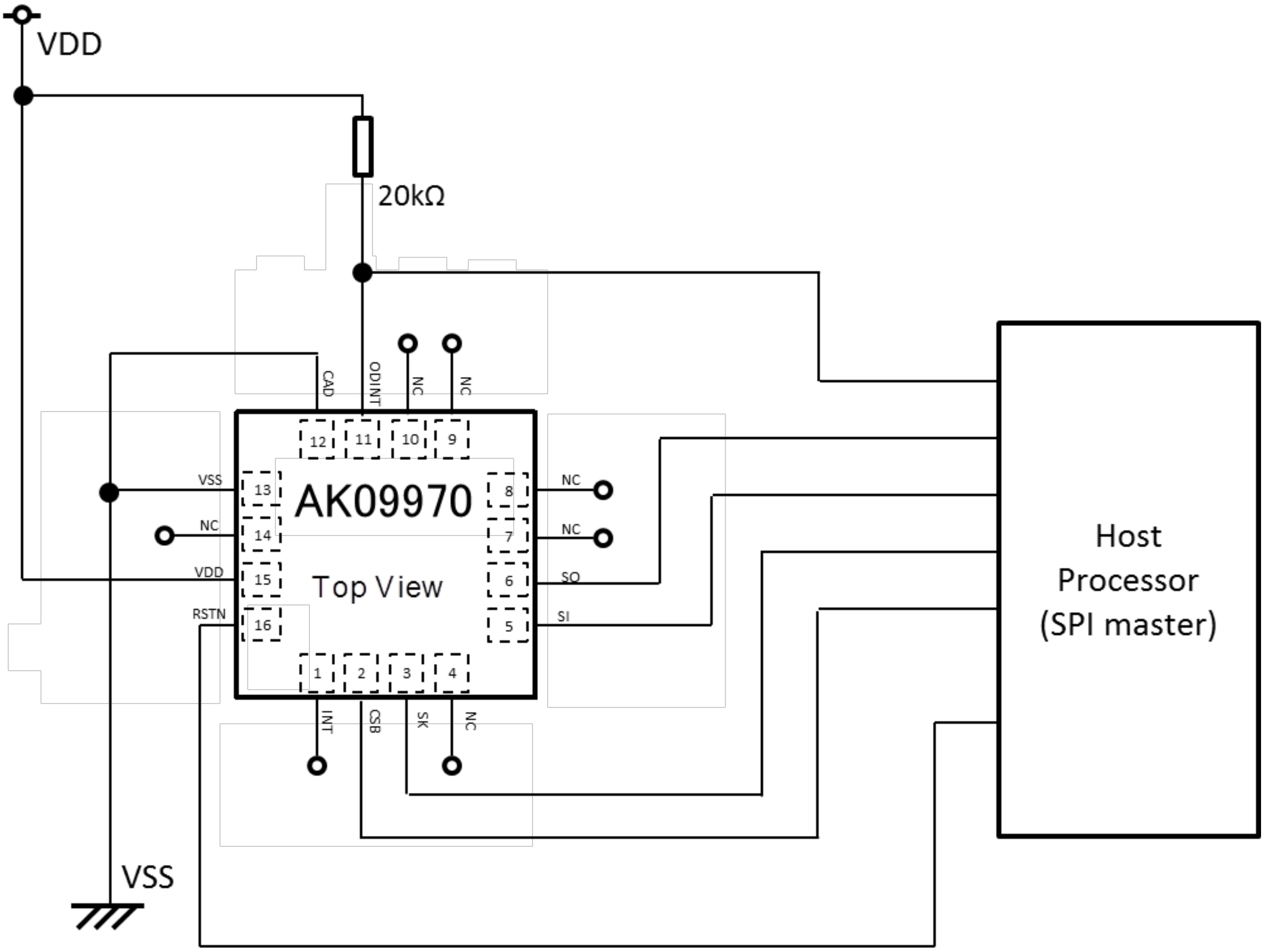
TST1 and TST2 register are test register for shipment test. Do not access this registers.

13. Recommended External Circuits

13.1. I²C Bus Interface



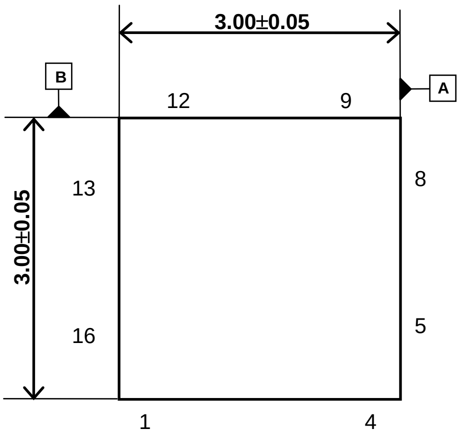
13.2. **4-wire SPI**

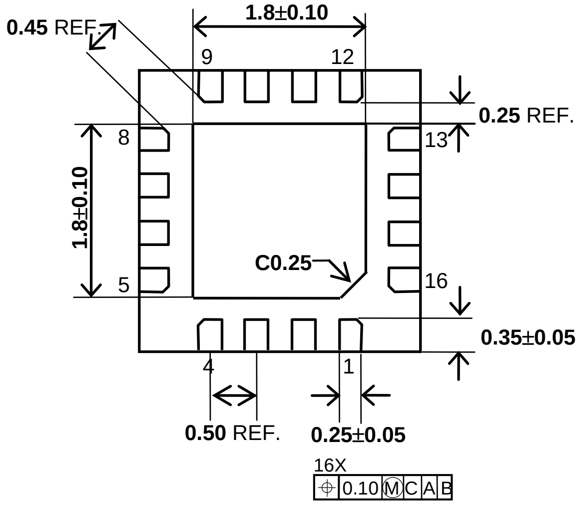


14. **Package**

14.1. **Outline Dimensions**

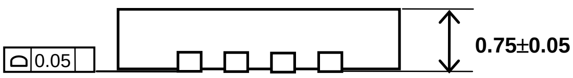
[mm]





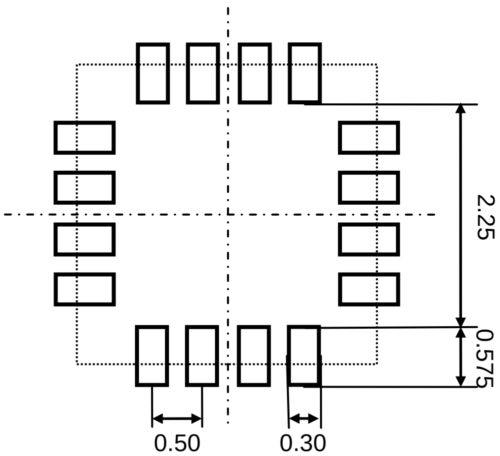
<Top view>

<Bottom view>



<Side view>

14.2. **Pad Dimensions**



14.3. **Marking**

Product name: 9970

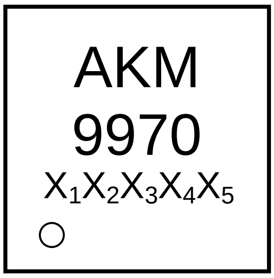
Date code: $X_1X_2X_3X_4X_5$

X1 = ID

X2 = Year code

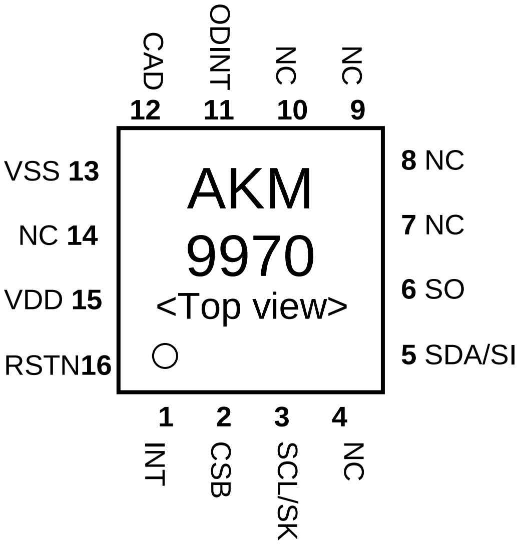
X3X4 = Week code

X5 = Lot

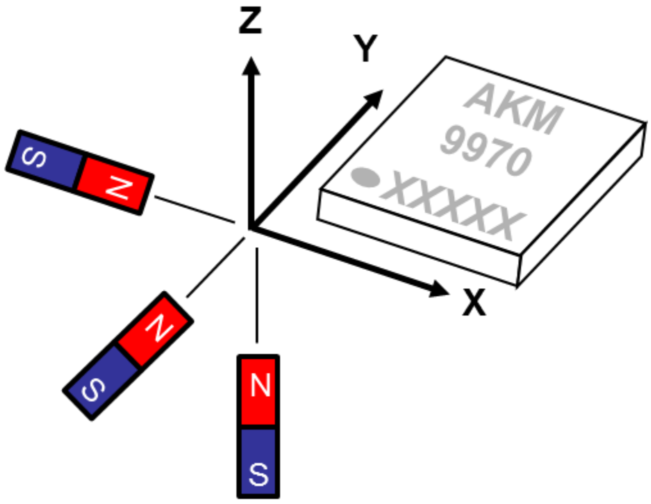


<Top view>

14.4. **Pin Assignment**



15. **Magnetic Orientation**



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