MLA-01122B

1 - 12 GHz Low-Noise MMIC Amplifier
Data Sheet

FEATURES

- **Wideband:** 1.0 to 12 GHz
- **NF (ext match):** 1.2 dB @ 2.0 GHz
  1.6 dB @ 6.0 GHz
  1.8 dB @ 12.0 GHz
- **P-1dB:** 16 dBm
- **OIP3:** 27 dBm
- **Gain:** 17 dB
- **Bias Condition:** VDD = 5 V
  IDD = 55 mA
- **50-Ohm On-chip Matching**
- **Unconditionally Stable: .5 GHz to 20 GHz**
- **Narrow-Band Optimization with External Tuning**
- **Gain Control Option Available with 2nd Gate Control Voltage**

APPLICATIONS

- **Microwave Point-to-Point Radios**
- **Satellite and Telemetry Communications**
- **Test Instrumentation**
- **EW Receiver Systems**
- **Wide-band Communication Systems**
- **Commercial Wireless Systems**

DESCRIPTION

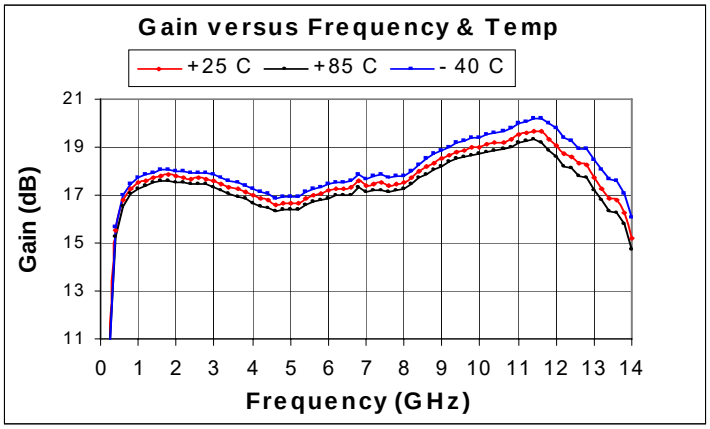
The MLA-01122B is a fully-matched broadband Low-Noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. This MMIC is suited for Satellite Communications, Microwave radios, Instrumentation, Wideband Systems and also many commercial wireless applications where low-noise figure with high-gain is desirable. It has excellent gain (17 dB) and Noise Figure (1.6 dB, mid-band) over a broad frequency range. Typical P-1dB is 16.5 dBm and OIP3 is +27dBm @ 6 GHz. It has on-chip bias circuit, choke and DC blocking to provide bias stability and ease of use. The 2nd Gate voltage input can be used for gain control if necessary. For packaged options, contact factory for further details.

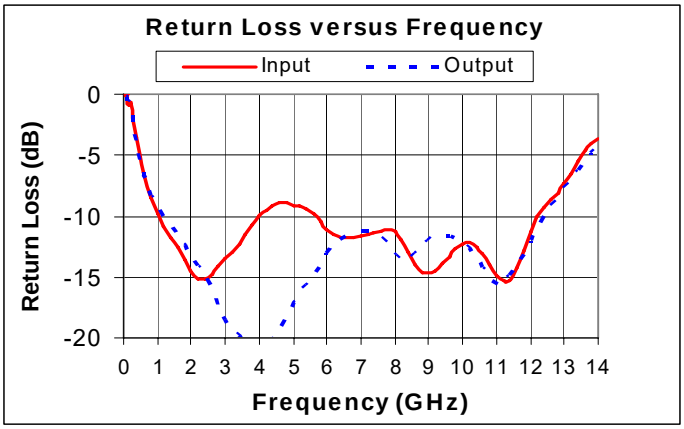
ELECTRICAL SPECIFICATIONS: *VDD=+5.0V, VG1=+0.15V, VG2=+2V, IDD=55 mA, Ta=25 C, ZO=50 ohm* (1)

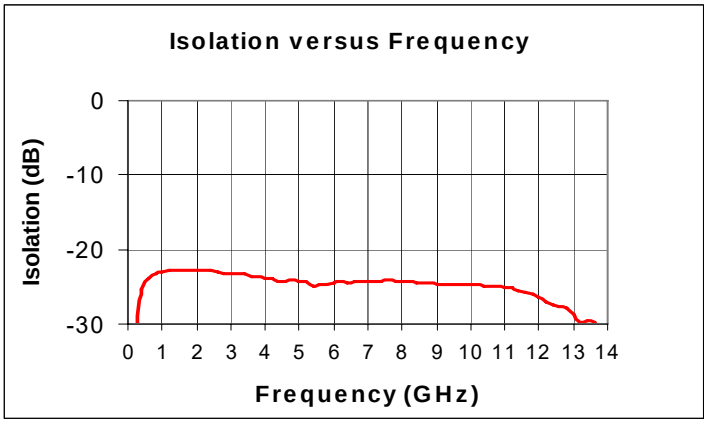
PARAMETER	TEST CONDITIONS	TYPICAL DATA	UNITS
Frequency Range		1-12	GHz
Gain	1 - 8 GHz 10 - 12 GHz	17 19	dB
Gain Flatness	1 - 8 GHz 1 - 12 GHz	0.6 1.5	+/-dB
Input Return Loss	2 GHz 5 GHz 10 GHz	15 9.5 12	dB
Output Return Loss		12	dB
Output P1dB	2 GHz 6 GHz 10 GHz 12 GHz	17 16.5 15.5 14.0	dBm
Output IP3 @ 0 dBm/tone, 1 MHz separation	2 GHz 6 GHz 12 GHz	30 27 25	dBm
Noise Figure	2 GHz 6 GHz 12 GHz	1.2 1.6 1.8	dB
Operating Bias Conditions: VDD IDD	VG1=+0.15V, VG2=+2V	+5 55	V mA
Stability Factor K	0.5 to 20 GHz	> 1	

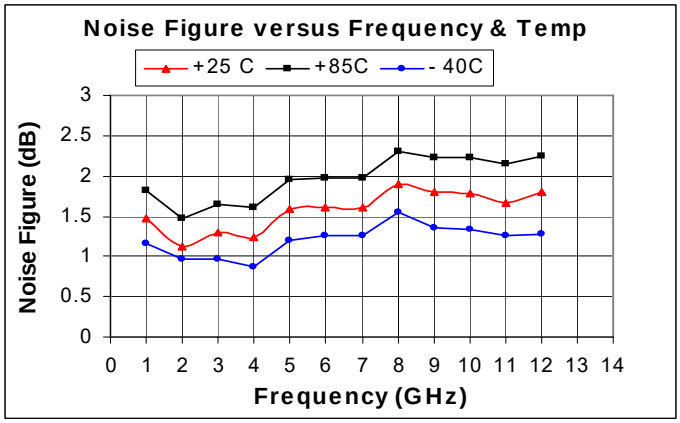
(1) All data is measured on 50 Ohm carrier with VG2 bias derived from VDD bias using resistive voltage divider and external tuning stubs shown in assembly diagram.

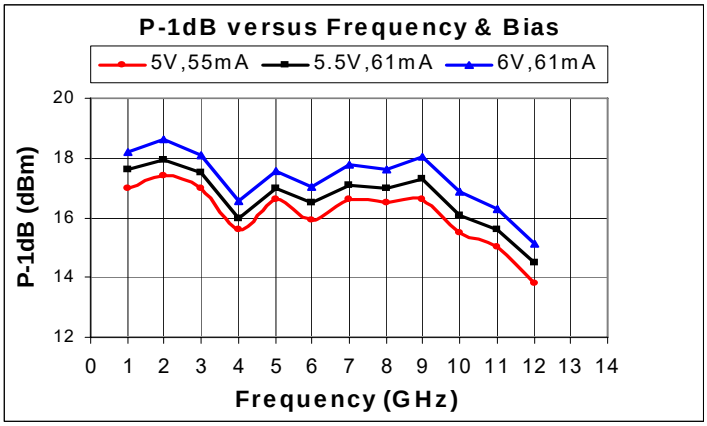
TYPICAL RF PERFORMANCE: *VDD=+5.0V, VG1=+0.15V, VG2=+2V, IDD=55 mA, Ta=25 C, ZO=50 ohm* [1]

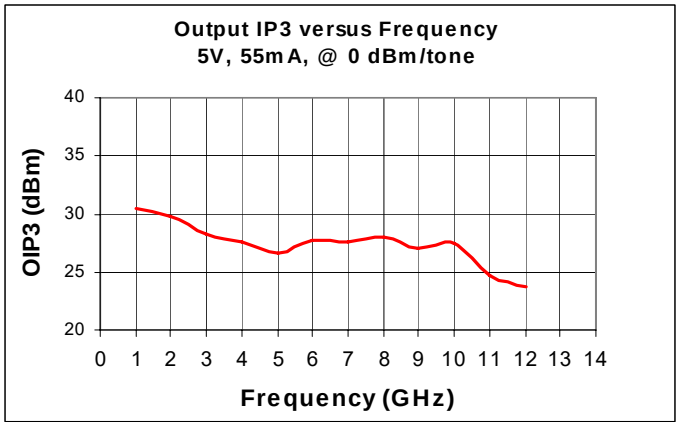




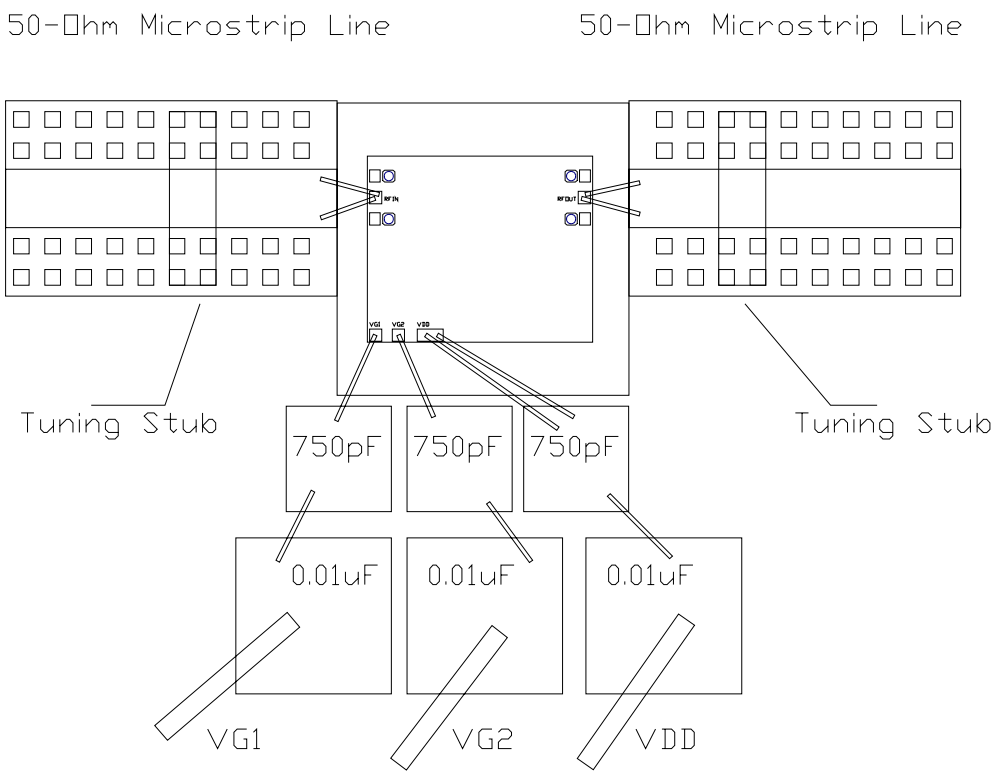








ASSEMBLY DIAGRAM: *For use with on-chip match option*



Notes:

1) 1st Close-in Bypass cap values must be at least 100pF and placed < 25mil from chip edge. The location of large bypass cap 0.01uF is not critical but recommended close to die. VG1 & VG2 large bypass cap 0.01uF may be removed to save space.
2) VG2 voltage may be derived from VDD supply using resistive voltage divider
3) RF IN/OUT Bonds must be 2 wires of length < 20 mil & 0.7 mil diameter for best RF performance.
4) Tuning stubs (10 x 40 mil) on the 50 ohm line will improve wide-band I/O return loss especially at frequencies > 8 GHz . Location may be tuned for best RF performance . All data shown includes the tuning stubs. Input Return Loss can be further optimized for narrower frequency band.

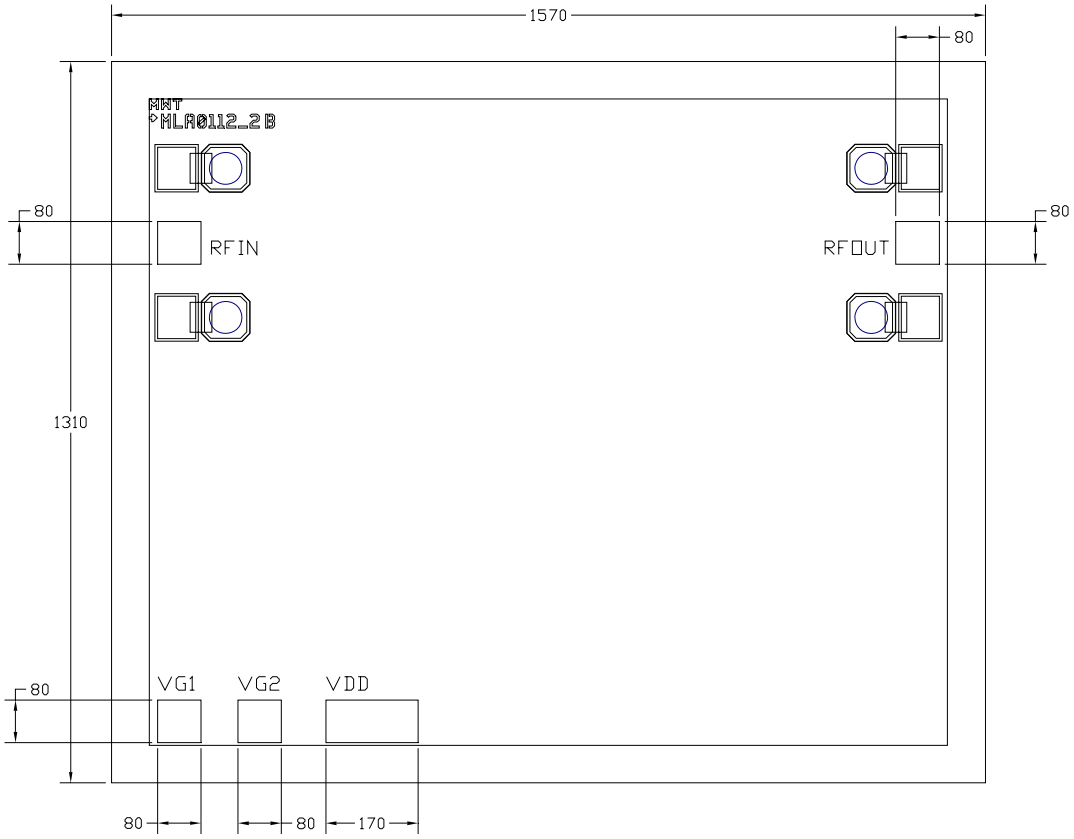
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETERS	UNITS	MAX
VDD	Drain Voltage	V	7
IDD	Drain Current	mA	75
Pdiss	DC Power Dissipation	W	0.4
Pin max	RF Input Power	dBm	13
Toper	Operating Case/Lead Temp Range	°C	-40 to +85
Tch	Channel Temperature	°C	150
Tstg	Storage Temperature	°C	-60 to 150

Exceeding any on of these limits may cause permanent damage.

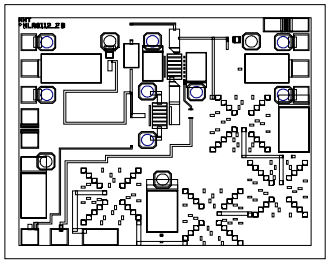
MECHANICAL INFORMATION

Outline Drawing



Notes:

1) Die Size: 1.57 x 1.31 x 0.1 mm
2) RFIN, RFOUT, VG1, VG2 Bond Pad Size is: 80 x 80 micron.
3) Backside of chip is metalized and provides DC & RF Ground.
4) Bond Pad & Backside metallization: Gold



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Functional Diagram