

# DDR5 SDRAM RDIMM Addendum

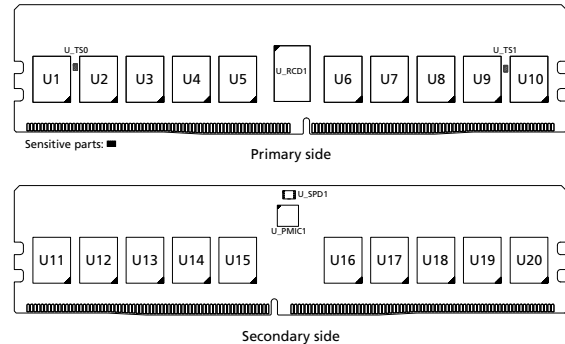
## MTC20F2085S1RC – 32GB 16Gb Die Revision A

### Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4Gig x 80)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each

**Figure 1: 288-Pin DDR5 RDIMM (R/C-E0)**



### Options

- Operating temperature
  - Commercial ( $0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$ )
- Frequency/CAS latency
  - 0.416ns @ CL = 40 (DDR5-4800)

### Marking

C  
48B

**Table 1: Addressing**

Parameter	32GB
Row address <sup>1</sup>	64K (R0-R15)
Column address <sup>1</sup>	1K (C0-C9)
Device bank group address <sup>1</sup>	8 (BG0-BG2)
Device bank address per bank group <sup>1</sup>	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

**Table 2: Part Numbers and Timing Parameters – 32GB Modules**

Base device: MT60B2G8,<sup>1</sup> 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL <sub>-n</sub> , RCD <sub>-n</sub> , RP)
MTC20F2085S1RC48BA1	32GB	4Gb x 80	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on [micron.com](http://micron.com).



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## DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3A	154	U2	0	11A	165
	1	0A	7		1	8A	18
	2	1A	9		2	9A	20
	3	2A	152		3	10A	163
	4	7A	161		4	15A	172
	5	4A	14		5	12A	25
	6	5A	16		6	13A	27
	7	6A	159		7	14A	170
U3	0	19A	176	U4	0	27A	187
	1	16A	29		1	24A	40
	2	17A	31		2	25A	42
	3	18A	174		3	26A	185
	4	23A	183		4	31A	194
	5	20A	36		5	28A	47
	6	21A	38		6	29A	49
	7	22A	181		7	30A	192
U5	0	CB3A	198	U6	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB1A	53		2	CB1B	98
	3	CB2A	196		3	CB2B	241
	4	CB7A	205		4	CB7B	236
	5	CB4A	58		5	CB4B	89
	6	CB5A	60		6	CB5B	91
	7	CB6A	203		7	CB6B	234
U7	0	3B	247	U8	0	11B	258
	1	0B	100		1	8B	111
	2	1B	102		2	9B	113
	3	2B	245		3	10B	256
	4	7B	254		4	15B	265
	5	4B	107		5	12B	118
	6	5B	109		6	13B	120
	7	6B	252		7	14B	263



**Table 3: Component-to-Module DQ Map (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U9	0	19B	269	U10	0	27B	280
	1	16B	122		1	24B	133
	2	17B	124		2	25B	135
	3	18B	267		3	26B	278
	4	23B	276		4	31B	287
	5	20B	129		5	28B	140
	6	21B	131		6	29B	142
	7	22B	274		7	30B	285
U11	0	24B	133	U12	0	16B	122
	1	27B	280		1	19B	269
	2	26B	278		2	18B	267
	3	25B	135		3	17B	124
	4	28B	140		4	20B	129
	5	31B	287		5	23B	276
	6	30B	285		6	22B	274
	7	29B	142		7	21B	131
U13	0	8B	111	U14	0	0B	100
	1	11B	258		1	3B	247
	2	10B	256		2	2B	245
	3	9B	113		3	1B	102
	4	12B	118		4	4B	107
	5	15B	265		5	7B	254
	6	14B	263		6	6B	252
	7	13B	120		7	5B	109
U15	0	CB0B	96	U16	0	CB0A	51
	1	CB3B	243		1	CB3A	198
	2	CB2B	241		2	CB2A	196
	3	CB1B	98		3	CB1A	53
	4	CB4B	89		4	CB4A	58
	5	CB7B	236		5	CB7A	205
	6	CB6B	234		6	CB6A	203
	7	CB5B	91		7	CB5A	60



**Table 3: Component-to-Module DQ Map (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U17	0	24A	40	U18	0	16A	29
	1	27A	187		1	19A	176
	2	26A	185		2	18A	174
	3	25A	42		3	17A	31
	4	28A	47		4	20A	36
	5	31A	194		5	23A	183
	6	30A	192		6	22A	181
	7	29A	49		7	21A	38
U19	0	8A	18	U20	0	0A	7
	1	11A	165		1	3A	154
	2	10A	163		2	2A	152
	3	9A	20		3	1A	9
	4	12A	25		4	4A	14
	5	15A	172		5	7A	161
	6	14A	170		6	6A	159
	7	13A	27		7	5A	16



## I<sub>DD</sub> Specifications

**Table 4: DDR5 I<sub>DD</sub> Specifications and Conditions – 32GB (Die Revision A)**

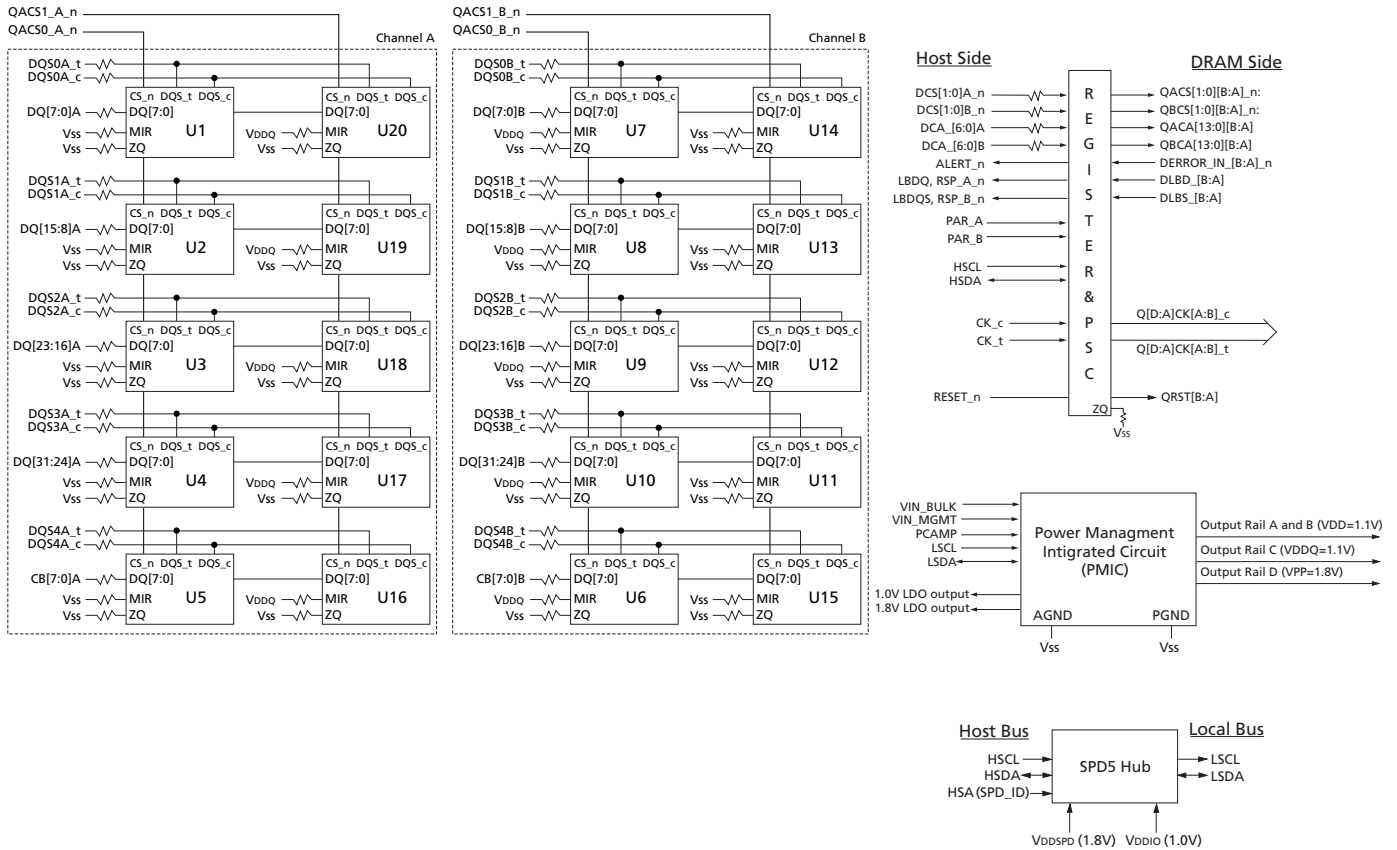
Module I<sub>DD</sub> is based on PMIC VIN\_BULK 12V input current and typical operating range of temperature. Each I<sub>DD</sub> parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V<sub>DD</sub>, V<sub>DDQ</sub>, and V<sub>PP</sub>).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub> <sup>1</sup>	309	mA
Operating four bank ACTIVATE-PRECHARGE current	I <sub>DD0F</sub> <sup>1</sup>	359	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	295	mA
Precharge standby non-target command	I <sub>DD2NT</sub> <sup>1</sup>	417	mA
Precharge power-down current	I <sub>DD2P</sub> <sup>2</sup>	280	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	300	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	288	mA
Operating burst read current	I <sub>DD4R</sub> <sup>1</sup>	602	mA
Operating burst write current	I <sub>DD4W</sub> <sup>1</sup>	717	mA
Operating burst write with write CRC current	I <sub>DD4WC</sub> <sup>1</sup>	675	mA
Burst refresh (normal refresh mode) current	I <sub>DD5B</sub> <sup>1</sup>	498	mA
Burst refresh (fine granularity refresh mode) current	I <sub>DD5F</sub> <sup>1</sup>	375	mA
Burst refresh (same bank refresh mode) current	I <sub>DD5C</sub> <sup>1</sup>	324	mA
Self refresh current	I <sub>DD6N</sub> <sup>2</sup>	128	mA
Operating bank interleave read current	I <sub>DD7</sub> <sup>1</sup>	638	mA
Maximum power saving deep power down mode current	I <sub>DD8</sub> <sup>2</sup>	144	mA

- Notes: 1. One module rank in this I<sub>DD</sub>/I<sub>DDQ</sub>/I<sub>PP</sub> condition, the other rank in I<sub>DD2N</sub>/I<sub>DDQ2N</sub>/I<sub>PP2N</sub>.  
2. Both ranks in this I<sub>DD</sub>/I<sub>DDQ</sub>/I<sub>PP</sub> condition.

## Functional Block Diagram

Figure 2: Functional Block Diagram



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external  $240\Omega \pm 1\%$  resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
  2. Functional block diagram is for reference only.



## **Revision History**

### **Rev. F – 12/2022**

- Update IDD specifications. Prior versions included erroneously copied specs from Die Rev A 1Rx8 RDIMM data sheet.

### **Rev. E – 08/2021**

- Production Release

### **Rev. D – 02/2021**

- Preliminary Release

### **Rev. C – 01/2021**

- Preliminary Release

### **Rev. B – 06/2020**

- Preliminary Release

### **Rev. A – 06/2020**

- Preliminary Release

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