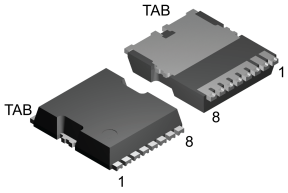
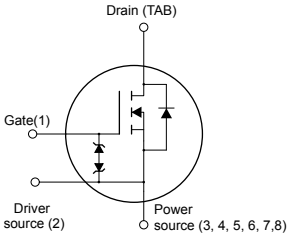
STO68N65DM6

Datasheet

N-channel 650 V, 53 mΩ typ., 55 A MDmesh DM6 Power MOSFET in a TO-LL package



TO-LL type A2



N-chG1DS2PS345678DTABZ

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO68N65DM6	650 V	65 mΩ	55 A

- Fast-recovery body diode
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link
STO68N65DM6

Product summary	
Order code	STO68N65DM6
Marking	68N65DM6
Package	TO-LL type A2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D[(1)]	Drain current (continuous) at T_C = 25 °C	55	A
	Drain current (continuous) at T_C = 100 °C	35	
I_{DM}[(2)]	Drain current (pulsed)	172	A
P_{TOT}	Total power dissipation at T_C = 25 °C	240	W
dv/dt[(3)]	Peak diode recovery voltage slope	100	V/ns
di/dt[(3)]	Peak diode recovery current slope	1000	A/µs
dv/dt[(4)]	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 55 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.52	°C/W
R_{thJB}	Thermal resistance, junction-to-board[(1)]	43	°C/W
	Thermal resistance, junction-to-board[(2)]	22	

1. *When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.*
2. *When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	930	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 27.5 A		53	65	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	3528	-	pF
C_{oss}	Output capacitance		-	258	-	pF
C_{rss}	Reverse transfer capacitance		-	1.5	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	609	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.25	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 48 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	80	-	nC
Q_{gs}	Gate-source charge		-	21.5	-	nC
Q_{gd}	Gate-drain charge		-	35	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d\ (on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 34 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	23	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	69	-	ns
t_f	Fall time		-	7.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		55	A
I_{SDM}(1)	Source-drain current (pulsed)		-		172	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 48 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 48 A, di/dt = 100 A/µs,	-	135		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	0.641		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.5		A
t_{rr}	Reverse recovery time	I_{SD} = 48 A, di/dt = 100 A/µs,	-	245		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	2.45		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

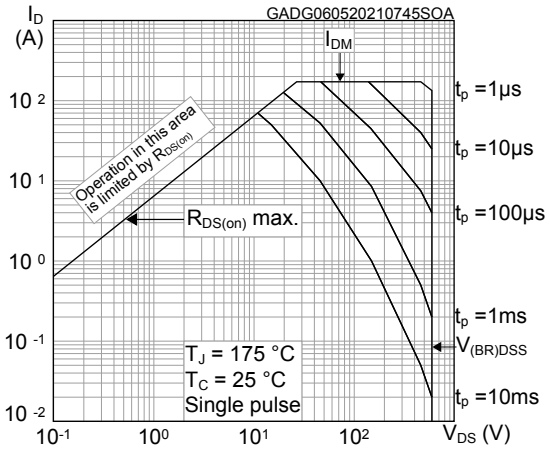


Figure 2. Maximum transient thermal impedance

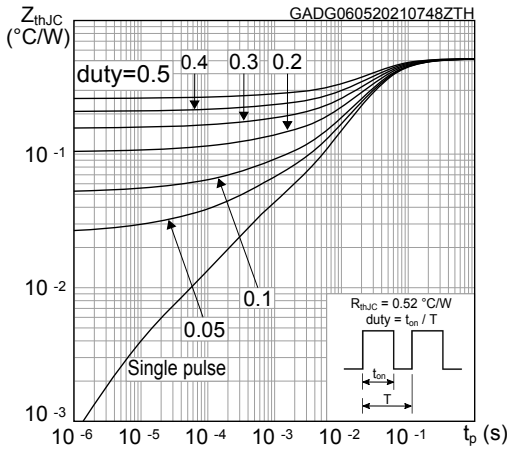


Figure 3. Typical output characteristics

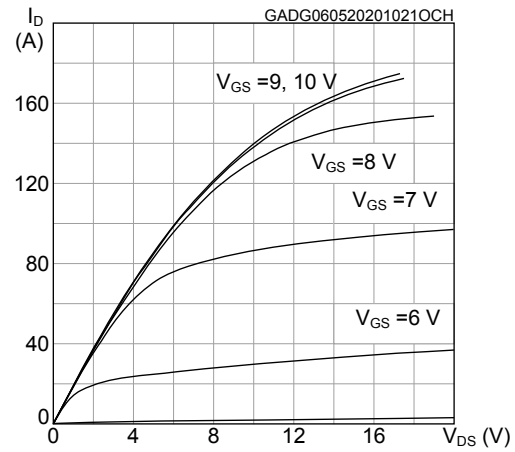


Figure 4. Typical transfer characteristics

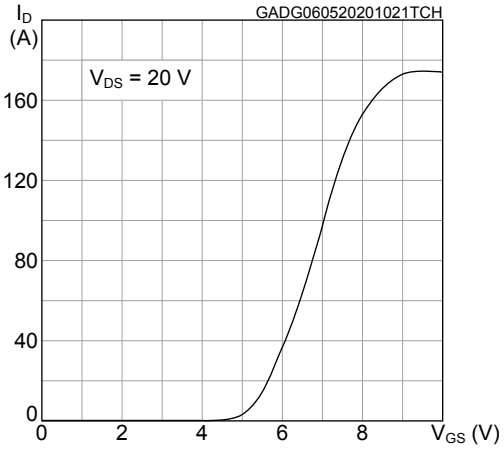


Figure 5. Typical gate charge characteristics

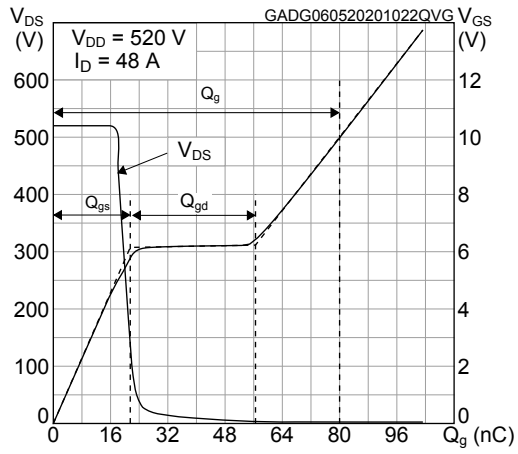


Figure 6. Typical drain-source on-resistance

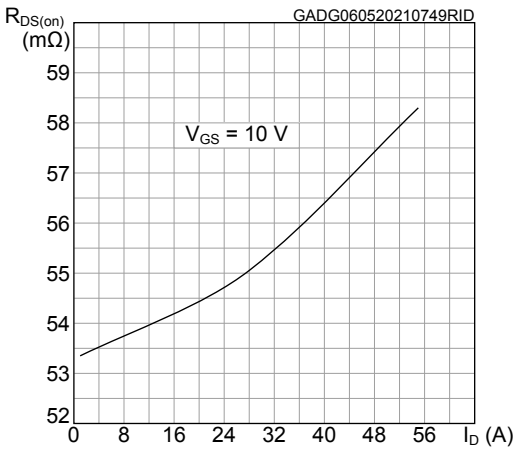


Figure 7. Typical capacitance characteristics

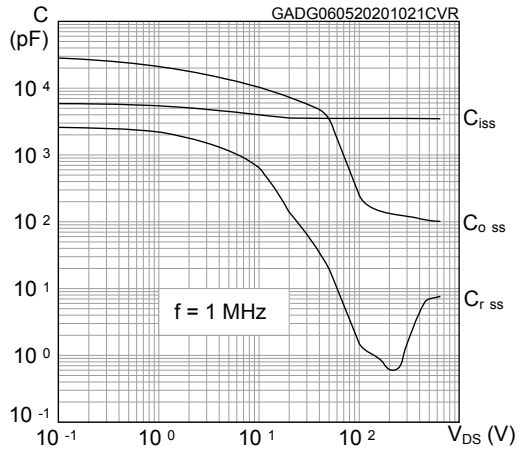


Figure 8. Normalized gate threshold vs temperature

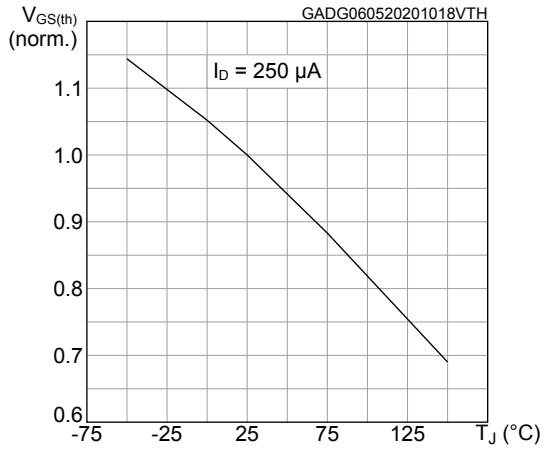


Figure 9. Normalized on-resistance vs. temperature

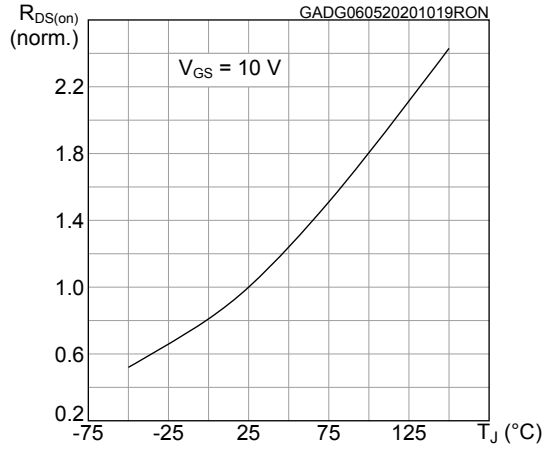


Figure 10. Normalized breakdown voltage vs temperature

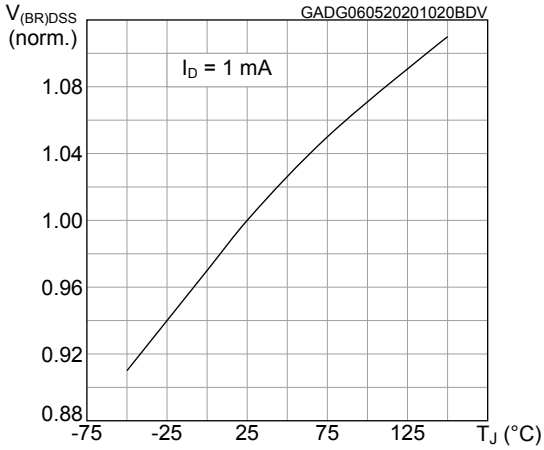


Figure 11. Typical output capacitance stored energy

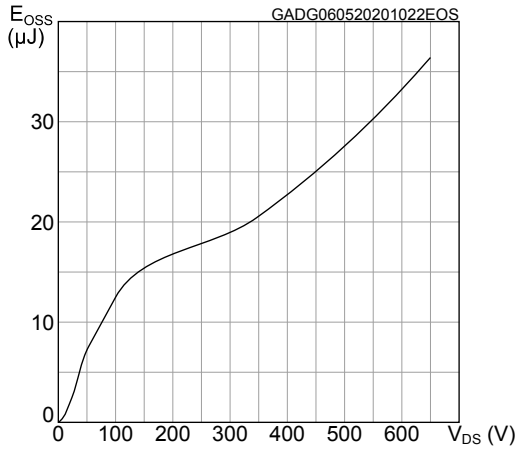
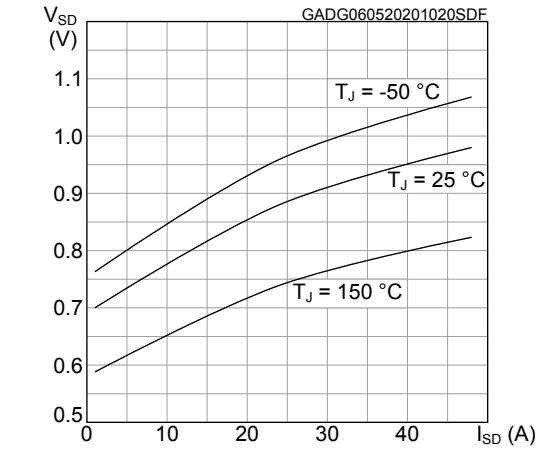


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

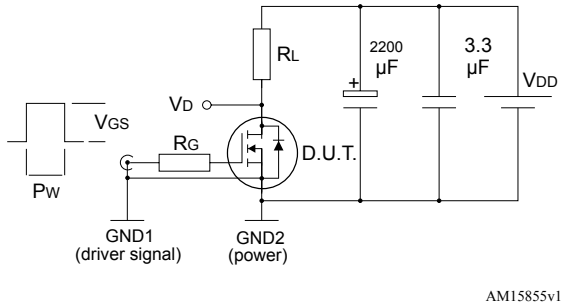


Figure 14. Test circuit for gate charge behavior

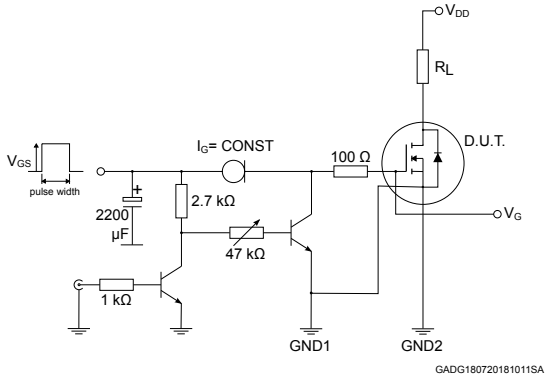


Figure 15. Test circuit for inductive load switching and diode recovery times

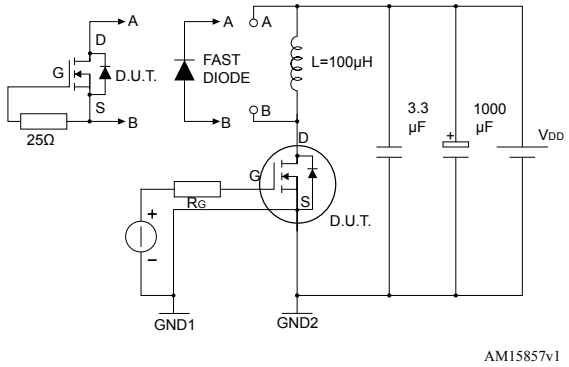


Figure 16. Unclamped inductive load test circuit

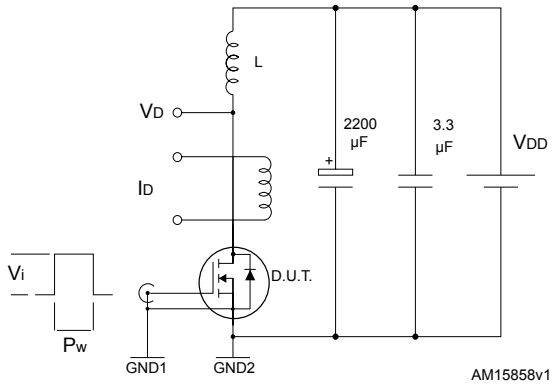


Figure 17. Unclamped inductive waveform

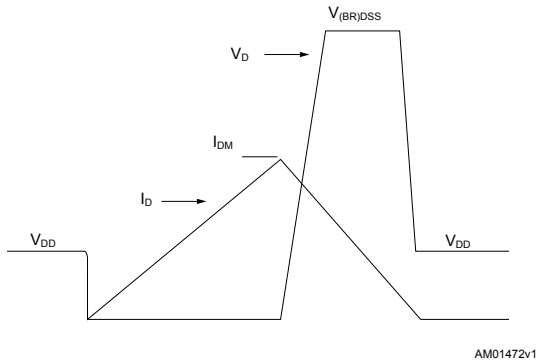
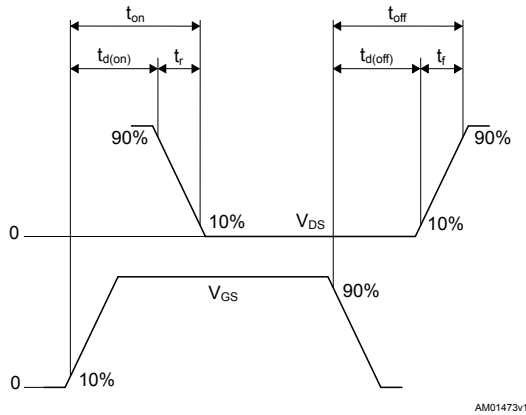


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL type A2 package information

Figure 19. TO-LL type A2 package outline

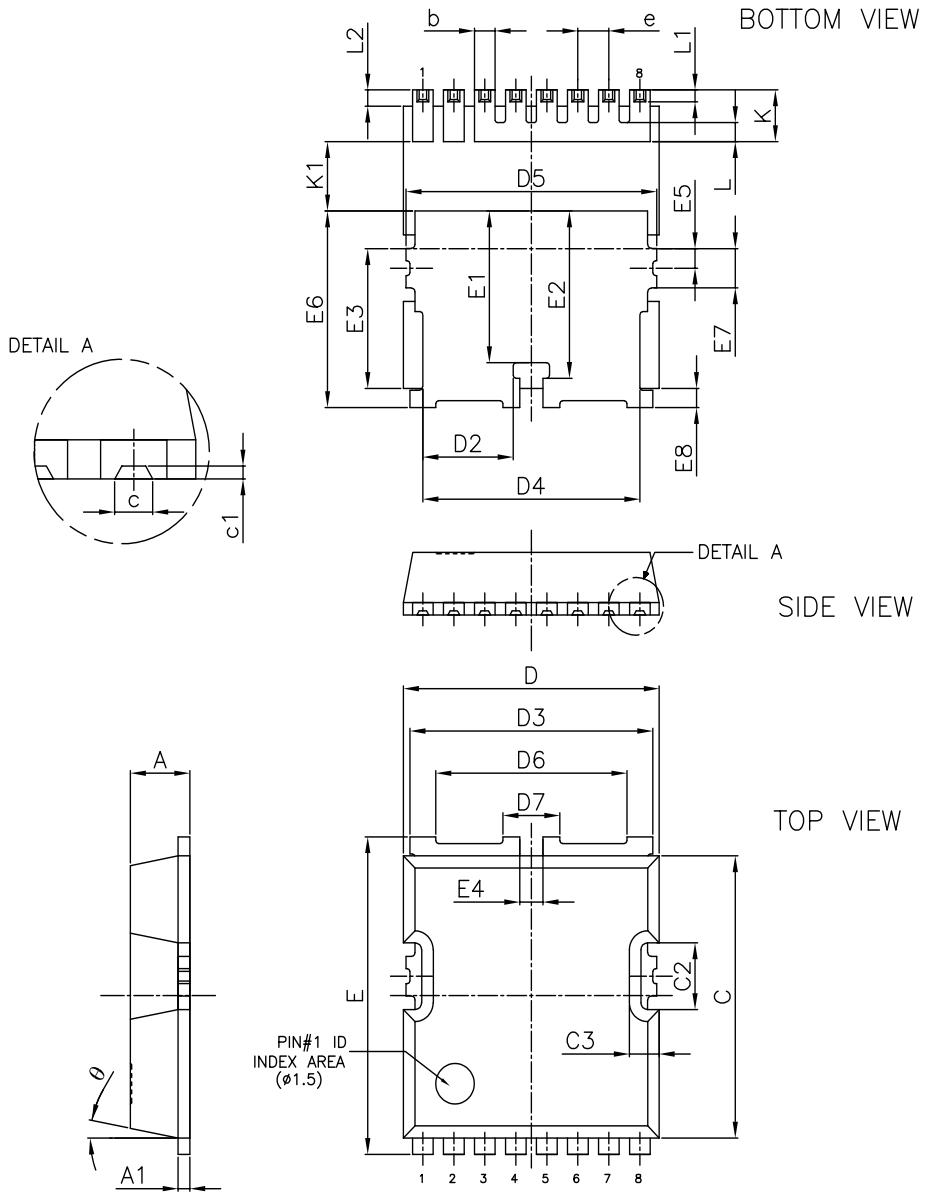


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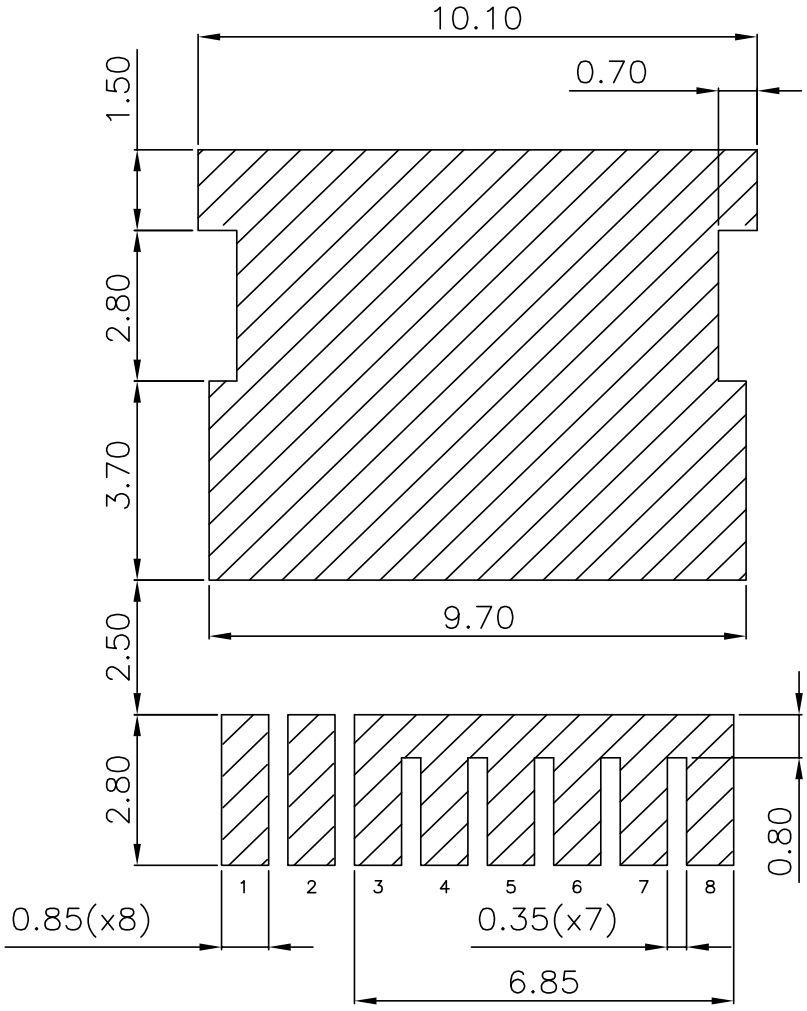
Table 8. **TO-LL type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b	0.70	0.80	0.90
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		1.16	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		5.58	
E2		6.15	
E3		5.14	
E4		0.90	
E5		0.72	
E6	7.03	7.23	7.43
E7		1.44	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
K1	2.40		
L		0.70	
L1		0.44	
L2	0.40	0.60	0.80
θ		11°	

Figure 20. TO-LL type A2 recommended footprint (dimensions are in mm)



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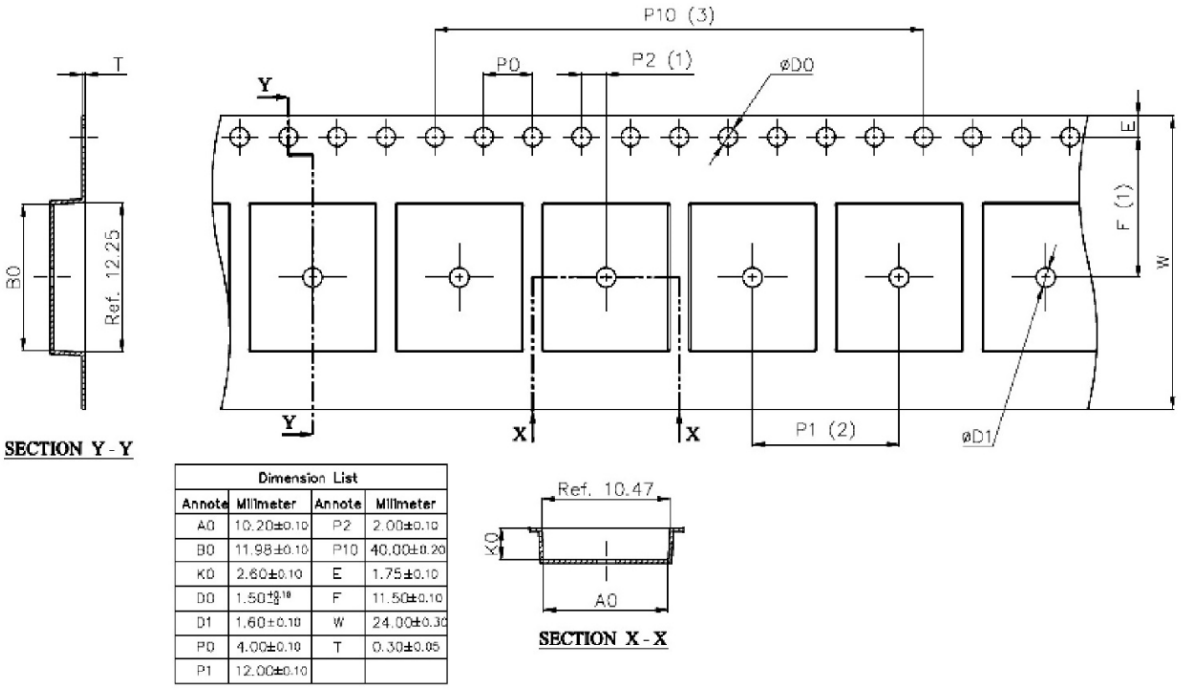
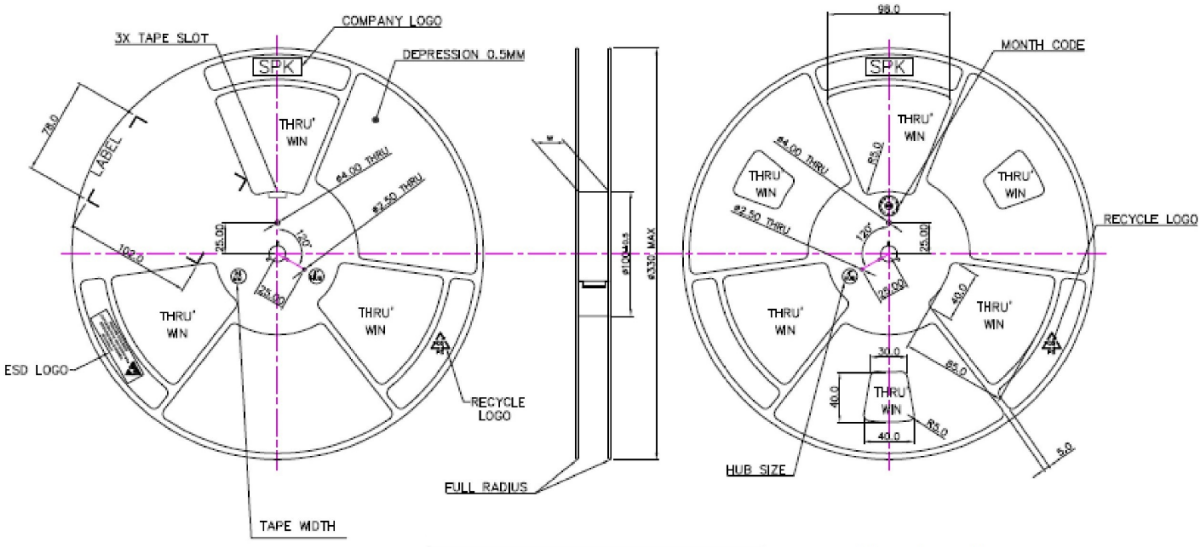
4.2 TO-LL packing information

Figure 21. **Carrier tape outline and dimensions**



Dimension List			
Annote	Millimeter	Annote	Millimeter
A0	10.20±0.10	P2	2.00±0.10
B0	11.98±0.10	P10	40.00±0.20
K0	2.60±0.10	E	1.75±0.10
D0	$1.50^{+0.10}_{-0}$	F	11.50±0.10
D1	1.60±0.10	W	24.00±0.30
P0	4.00±0.10	T	0.30±0.05
P1	12.00±0.10		

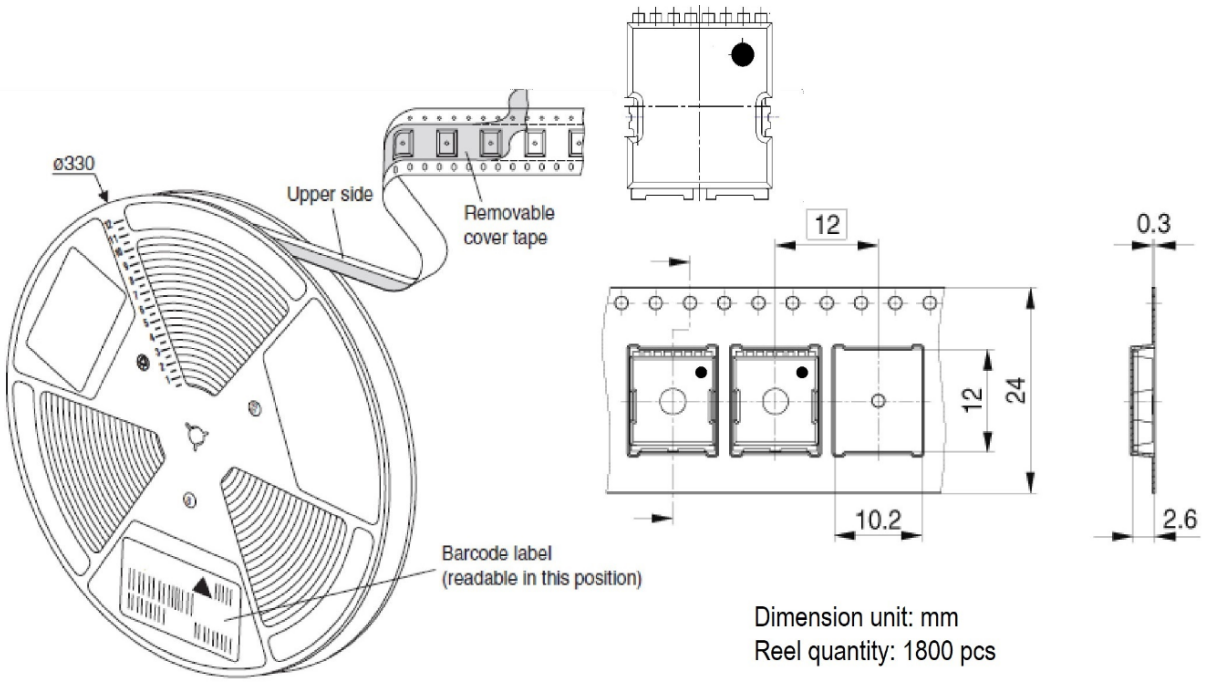
Figure 22. **Reel outline and dimensions**



SPECIFICATION							
TAPE WIDTH	W	U	X	V	Y	Z	P
24mm	24.4	1.50	24.5	20.0	0.55	6.00	2

Dimension unit: mm

Figure 23. **TO-LL orientation in tape pocket**



Revision history

Table 9. **Document revision history**

Date	Version	Changes
06-May-2021	1	First release.

Contents