User's Guide

TPS566231P and TPS566238P Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS566231P and TPS566238P as well as support documentation for the TPS566231PEVM and TPS566238PEVM. Included are the performance specifications, schematic, and the list of materials of the TPS566231PEVM.

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1 Introduction

The TPS566231P is a single, D-CAP3™ mode, synchronous buck converter that requires a very low external component count. The TPS566231P is a cost-effective, high-voltage input, synchronous buck converter with integrated FETs. One of the key features of the TPS566231P is its ULQ (Ultra Low Quiescent), which is extremely beneficial for long battery life in low-power operation. The TPS566231P operates with wider supply input voltage ranging from 3 V to 18 V. The device uses DCAP3 control mode to provide the following:

- Fast transient response
- Good line
- Load regulation
- No requirement for external compensation
- Support to low-ESR output capacitors

The TPS566231P is a high-efficiency converter, and provides complete protection (OVP, UVP, OCP, OTP), and with PGOOD indicator. The TPS566238P is in continuous current mode. Others are same with the TPS566231P. Table 1-1.

The TPS566231PEVM and TPS566238PEVM are single, synchronous buck converter evaluation modules that provide 1 V at 6 A from a 3-V to 18-V input. This user's guide describes the TPS566231PEVM performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) RANGE	OUTPUT CURRENT (I_{OUT}) RANGE
TPS566231PEVM	3 V to 18 V	0 A to 6 A

2 Performance Specification Summary

A summary of the TPS566231PEVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of 12 V and an output voltage of 1 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS566231PEVM Performance Specifications Summary

Specifications		Test Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input voltage		3	12	18	V
CH1	Output voltage			1		V
	Operating frequency	V_{IN} = 12 V, I_{OUT} =6 A		600		kHz
	Output current range		0		6	A
	Over current limit	V_{IN} = 12 V, L_{OUT} = 1 µH		7.4		A
	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 6 A		10		mV_{PP}

3 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R4 (Rupper) and R5 (Rlower). The value of R4 and R5 for a specific output voltage can be calculated using Equation 1 and refer to Table 3-1 for some recommendation values.

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}}) \quad (1)$$

Table 3-1. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)			C_{OUT} (µF)		C_{FF} (PF)
			MIN	TYP	MAX	MIN	MAX	
0.6	10	0	0.68	1	4.7	44	220	-
1	30	20	0.68	1	4.7	44	220	-
1.8	20	40	1	1.5	4.7	44	220	0-50
3.3	20	90	1.5	2.2	4.7	44	220	10-100
5.0	30	220	1.5	2.2	4.7	44	220	10-100

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS566231PEVM. The section also includes test results typical for the evaluation modules, includes power on/off, voltage ripple.

4.1 Input/Output Connections

The TPS566231PEVM is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 6 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 6 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP2 provides a place to monitor the V_{IN} input voltages with TP7 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP13 as the ground reference.

Table 4-1. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1V with DC 6-A maximum current
JP1	Two resistor dividers connected to V_{IN} to enable EN.
JP2	En Control, short pin1 and pin2 to make EN on, short pin2 and pin3 to make EN off.
TP1	V_{IN} positive monitor point
TP2	V_{IN} positive monitor point
TP3	Switch node test point
TP4	V_{OUT} positive monitor point
TP5	V_{OUT} positive monitor point
TP6	GND monitor test point
TP7	GND monitor test point
TP8	V_{CC} monitor test point
TP9	EN Test point
TP10	PGOOD monitor test point
TP11	GND monitor test point
TP12	Loop test point
TP13	GND monitor test point
TP14	GND monitor test point
TP15	GND monitor test point

4.2 Start-Up Procedure

1. Ensure that the jumper at JP2 (Enable control) pins 2 and 3 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate input voltage to VIN (J1-1) or TP1 and GND (J1-2) or TP6. and be noted that the board can't support hot plug-in. The input lines should be connected between J1 and external power source first before turning on the external input power supply.
3. Move the jumper at JP2 (Enable control) from pins 2(EN) and 3(OFF), to pins 1(ON) and 2(EN) and make JP1 pin 1 and pin 2 are covered, then the output can be enabled.
4. Apply the loading to Vout (J2-1) or TP4 and GND (J2-2) or TP10.

4.3 Start-Up

The TPS566231PEVM start-up waveform relative to EN is shown in Figure 4-1.

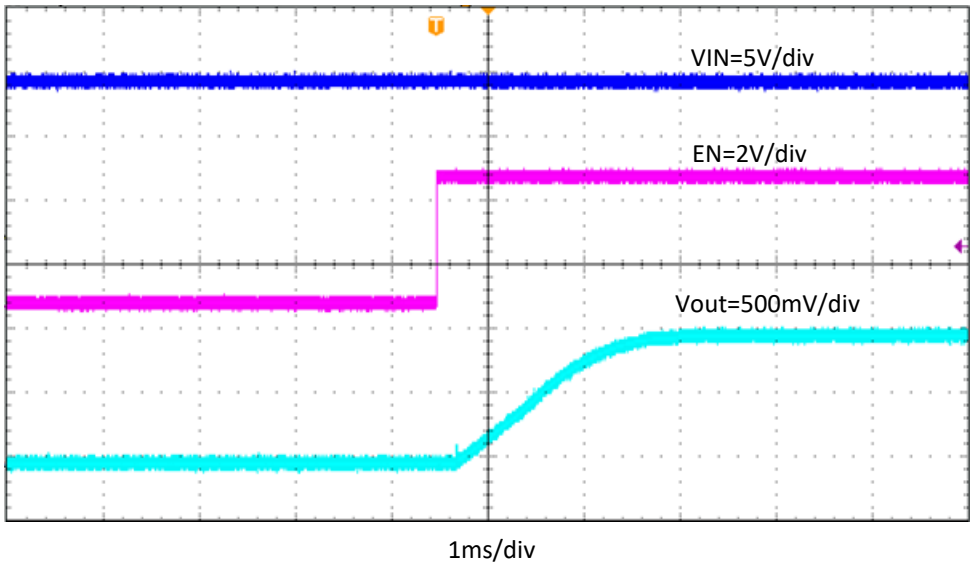

Figure 4-1. Start-Up Relative to EN, I_{OUT}= 3A

4.4 Shut-Down

The TPS566231PEVM shut-down waveform relative to EN is shown in Figure 4-2.

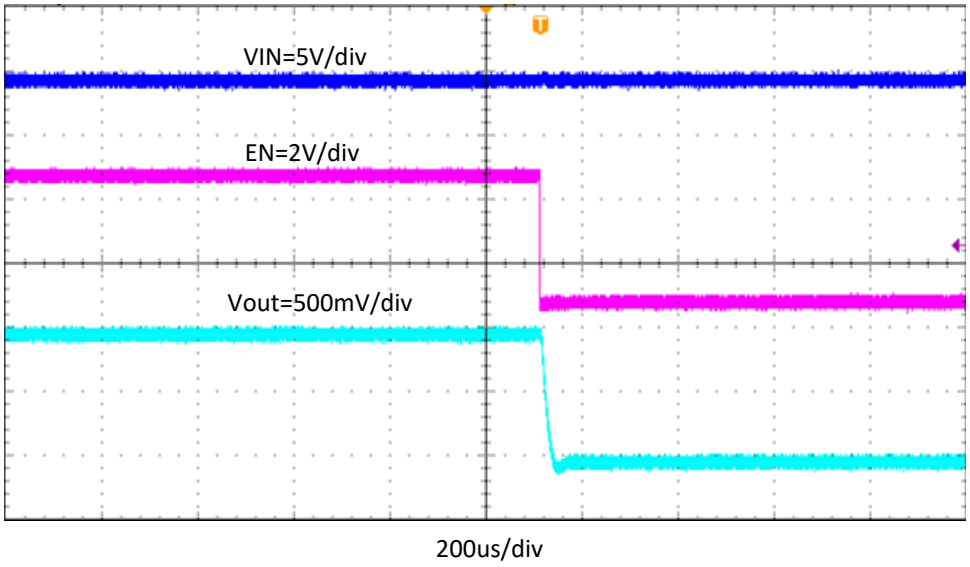

Figure 4-2. Shut-Down Relative to EN, I_{OUT}= 3A

4.5 Output Voltage Ripple

The TPS566231PEVM output voltage ripple is shown in Figure 4-3 and Figure 4-4. The output currents are as indicated.

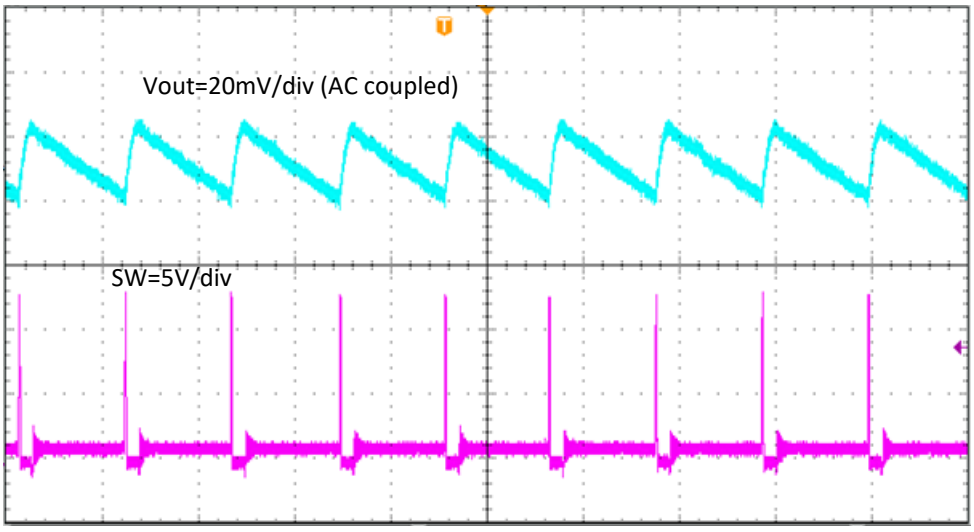

Figure 4-3. TPS566231P Output Voltage Ripple, I_{OUT} = 0.01A

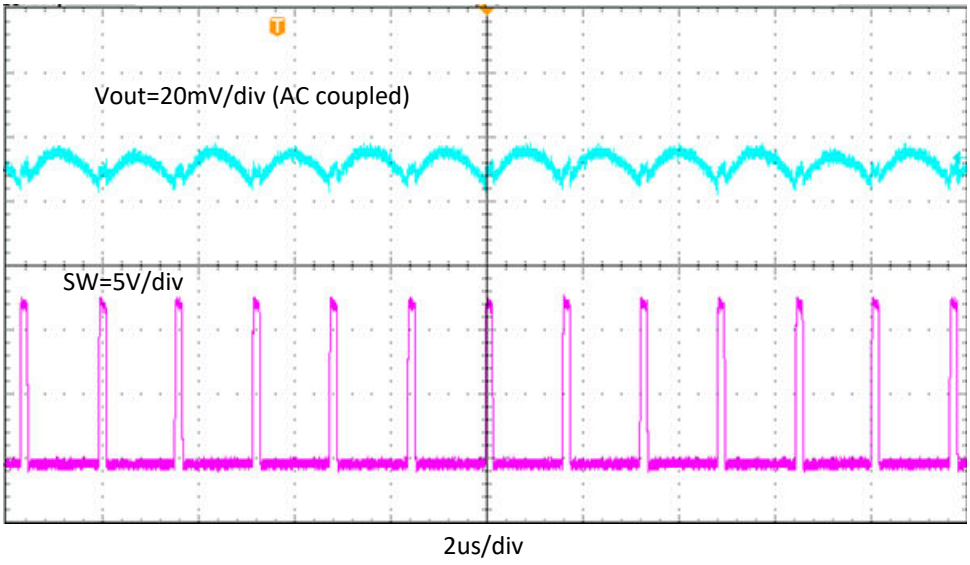

Figure 4-4. TPS566231P Output Voltage Ripple, I_{OUT} = 6A

5 Board Layout

This section provides a description of the TPS566231PEVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS566231PEVM is shown in Figure 5-1 and Figure 5-2 to Figure 5-5.

TPS566231PEVM is with four layers, The top layer contains the main power traces for VIN, VOUT and GND. Also on the top layer are connections for the pins of the TPS566231P and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, C3 and C4 are located as close to Vin pins and PGND pins of the IC as possible. The input and output connectors, test points and all of the components are located on the top side.

The bottom layer is a ground plane along with signal ground copper fill and the feed back trace from the point of regulation to the top of the resistor divider network.

Two inner layers are ground plane.

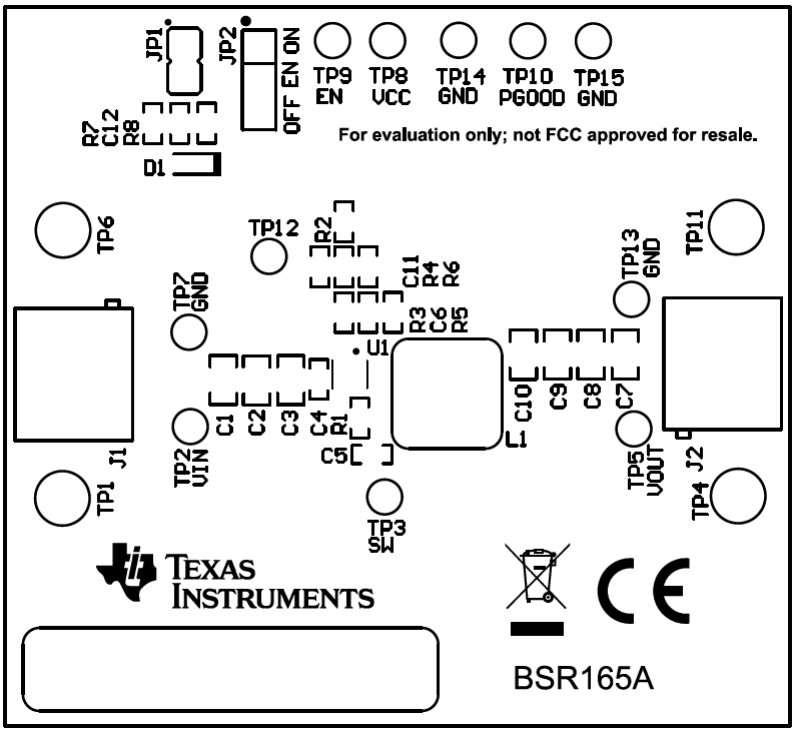

Figure 5-1. Top Assembly

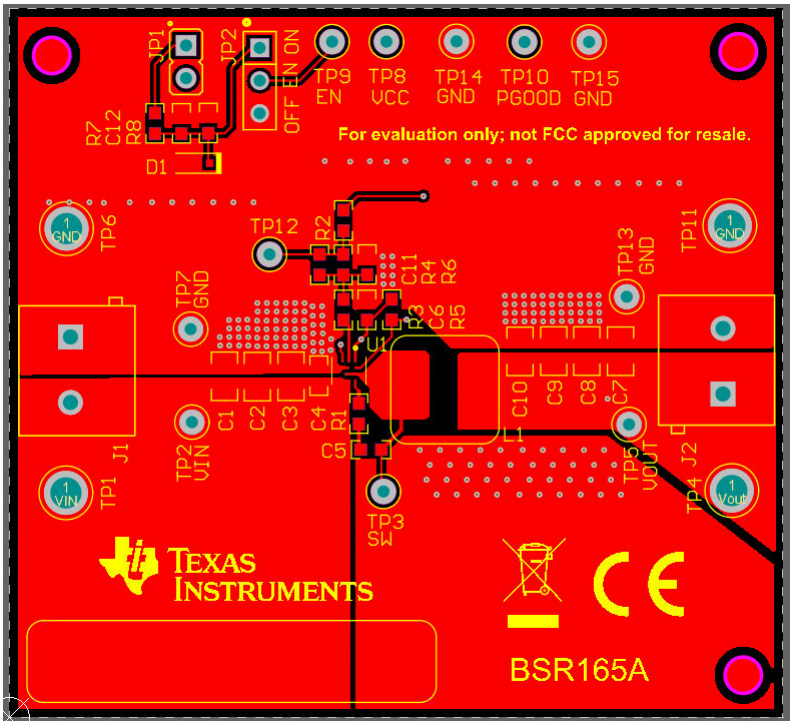

Figure 5-2. Top Layer

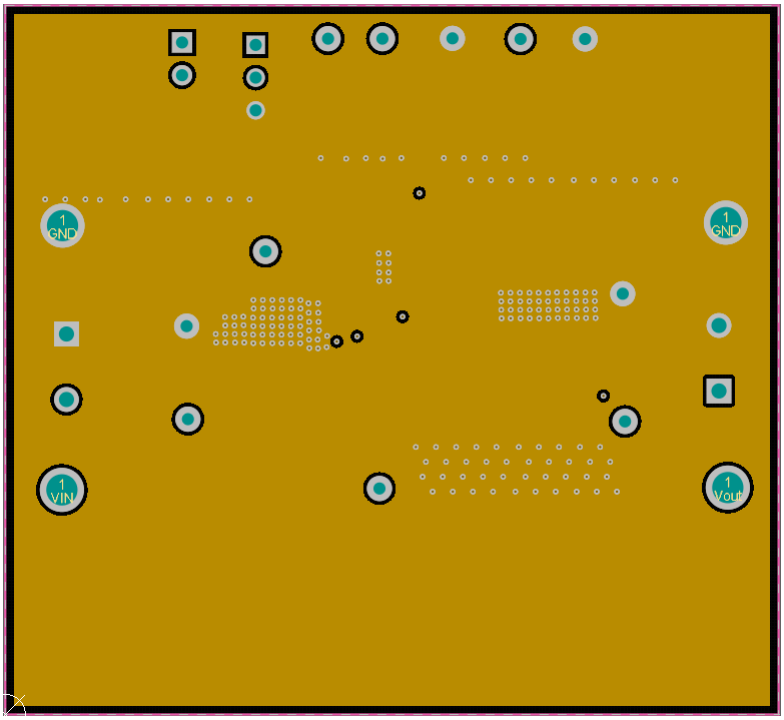

Figure 5-3. Inner1 Layer

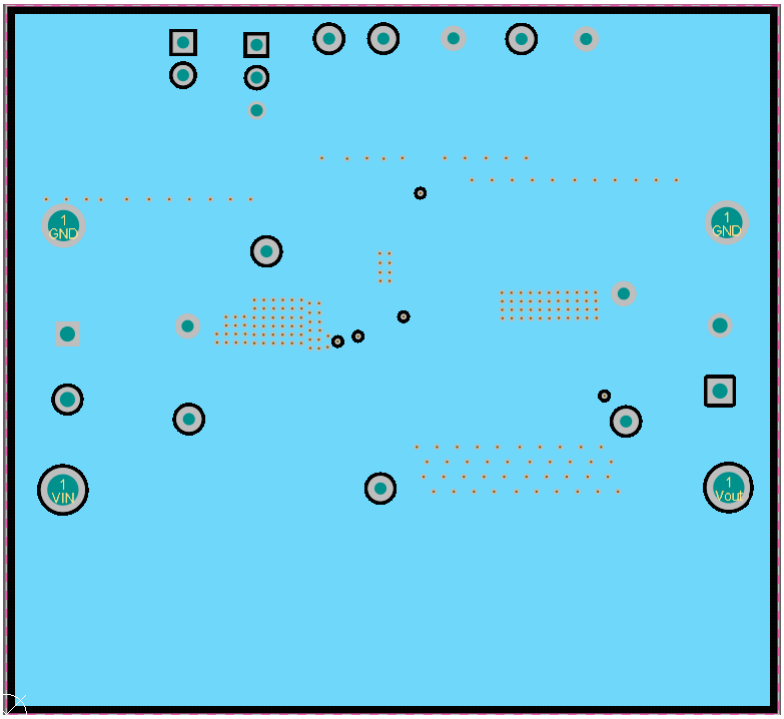

Figure 5-4. Inner2 Layer

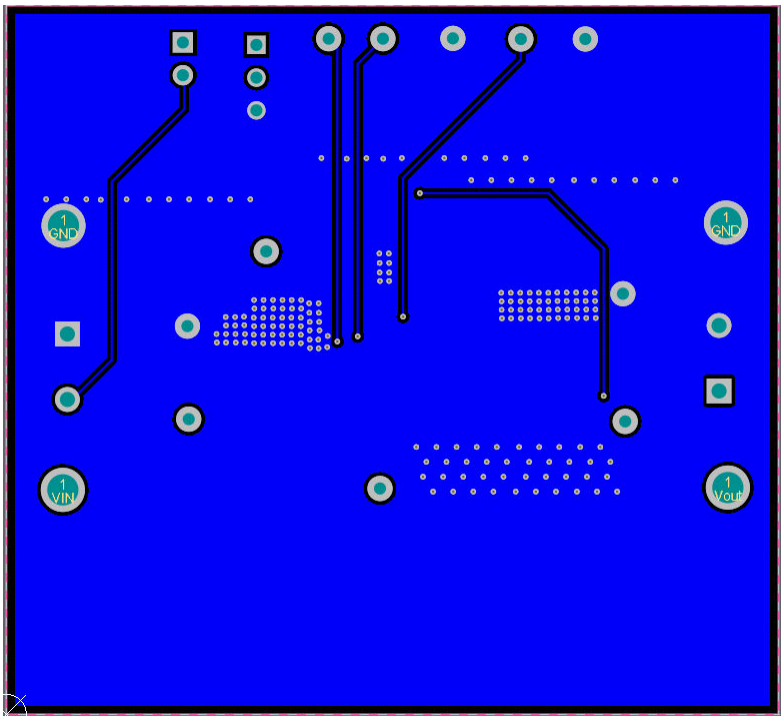

Figure 5-5. Bottom Layer

6 Board Profile, Schematic, List of Materials, and Reference

6.1 Board Profile

Figure 6-1 is the top view for the TPS566231PEVM.

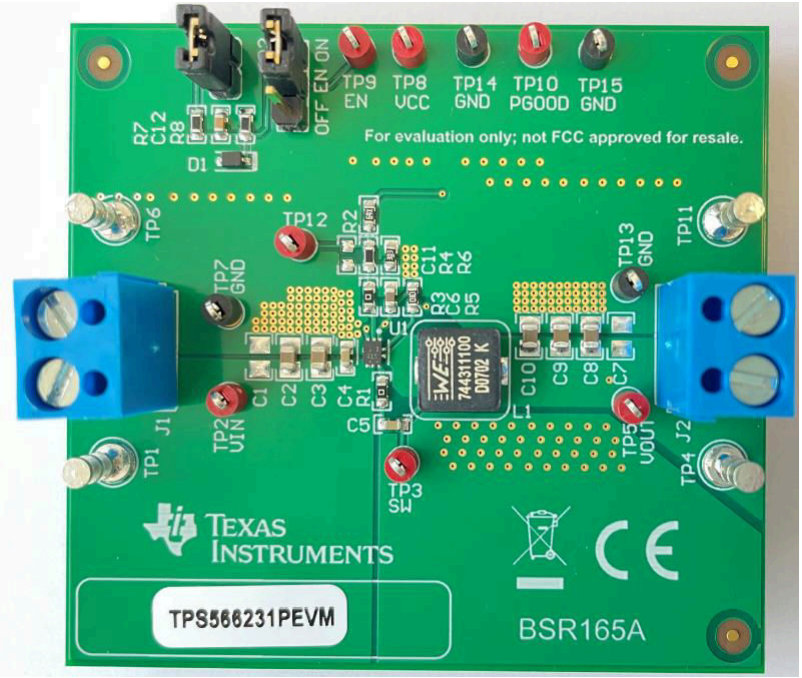

Figure 6-1. Top View of TPS566231PEVM

Figure 6-2 is the bottom view for the TPS566231PEVM.

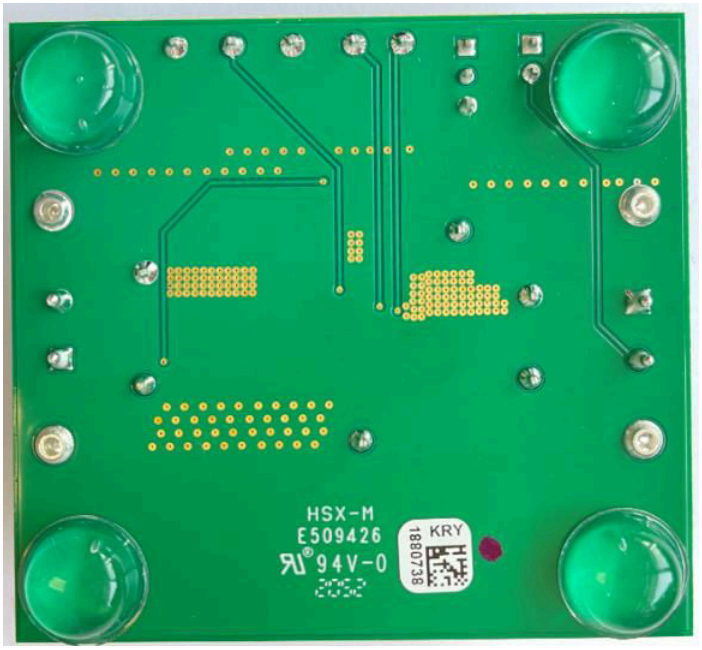

Figure 6-2. Bottom View of TPS566231PEVM

6.2 Schematic

Figure 6-3 is the schematic for the TPS566231PEVM.

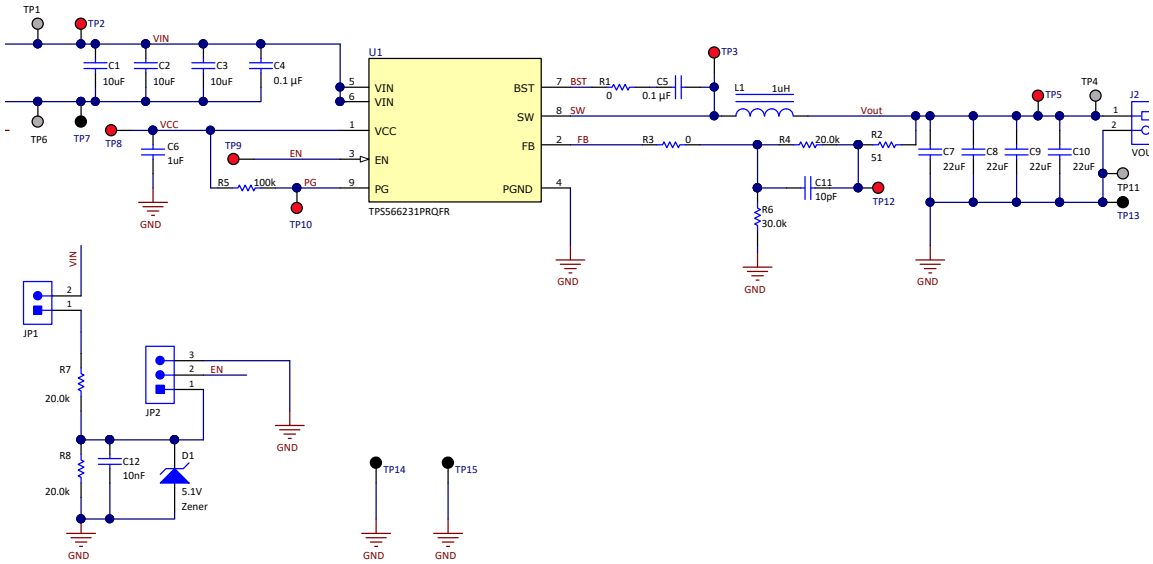

Figure 6-3. TPS566231PEVM Schematic Diagram

6.3 List of Materials

Table 6-1 displays the TPS566231PEVM list of materials.

Table 6-1. List of Materials(1)

Designator	Qty	Description	Part Number	Manufacturer
PCB1	1	Printed Circuit Board	BSR106	
C2, C3	2	Capacitor, ceramic, 10 uF, 25 V, +/- 20%, X5R, 0805	GRM21BR61E106MA73L	MuRata
C4, C5	2	Capacitor, ceramic, 0.1 µF, 25 V,+/- 10%, X5R, 0603	CL10A104KA8NNNC	Samsung Electro-Mechanics
C6	1	Capacitor, ceramic, 1 uF, 10 V, +/- 10%, X5R, 0603	C1608X5R1A105K080AC	TDK
C8, C9, C10	3	Capacitor, ceramic, 22 uF, 10 V, +/- 20%, X5R, 0805	GRM21BR61A226ME44L	MuRata
C12	1	Capacitor, ceramic, AP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	C0603C103K4RACTU	Kemet
D1	1	Diode, Zener, 5.1 V, 200 mW, SOD-323	MMSZ5231BS-7-F	Diodes Inc.
H1, H2, H3, H4	4	Bumpon, Hemisphere, 0.44 X 0.20, Clear, Transparent	SJ-5303 (CLEAR)	3M
J1, J2	2	Terminal Block, 5.08 mm, 2x1, Brass, TH	ED120/2DS	On-Shore Technology
JP1	1	Header, 100mil, 2x1, Gold, TH, 230 mil above insulator	PBC02SAAN	Sullins Connector Solutions
JP2	1	Header, 100mil, 3x1, Tin, TH, 3 PIN	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, Shielded Drum Core, WE-Superflux200, 1 uH, 15 A, 0.0046 ohm, SMD, 6.9x3.8x6.9mm	744311100	Wurth Elektronik
LBL1	1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	THT-13-457-10	Brady
R1, R3	2	Resistor, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R2	1	Resistor, 51, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060351R0JNEA	Vishay-Dale
R4, R7, R8	3	Resistor, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
R6	1	Resistor, 30.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3EKF3002V	Panasonic
R5	1	RES, 100 k, 5%, 0.1 W, 0603	CRCW0603100KJNEAC	Vishay-Dale
SH-JP1, SH-JP2	2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G or 969102-0000-DA	Samtec or 3M
TP1, TP4, TP6, TP11	4	Terminal, Turret, TH, Triple	1598-2	Keystone
TP2, TP3, TP5, TP8, TP9, TP10, TP12	7	Test Point, Miniature, Red, TH	5000	Keystone
TP7, TP13, TP14, TP15	4	Test Point, Miniature, Black, TH	5001	Keystone
U1	1	TPS566231PRQFR, RQF0009A (VQFN-HR-9)	TPS566231PRQFR	Texas Instruments
C1	0	Capacitor, ceramic, 10 uF, 25 V, +/- 20%, X5R, 0805	GRM21BR61E106MA73L	MuRata
C7	0	Capacitor, ceramic, 22 uF, 10 V, +/- 20%, X5R, 0805	GRM21BR61A226ME44L	MuRata
C11	0	Capacitor, ceramic, 10 pF, 10 V, +/- 10%, X7R, 0603	0603ZC100KAT2A	AVX
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

(1) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts may be substituted with equivalents.

6.4 Reference

1. Texas Instruments, *TPS566231 3 V to 18 V Input, 6-A Synchronous Step-Down Voltage Regulator* data sheet.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (April 2021)	Page
• Updated user's guide title	3

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265