CML Microcircuits
COMMUNICATION SEMICONDUCTORS

EV9750
Evaluation Kit for CMX975

UM9750/1 December 2017

USER MANUAL

Advance Information

Features

- **Demonstrates the CMX975 Fractional-N RF PLL, IF PLL and associated VCOs**
- **On-board reference oscillator with options for an external source.**
- **Flexible configuration allows use of off-chip VCOs.**
- **Divided LO outputs**
- **VHF IF to 1 to 2.7 GHz Up-converter**
- **1 to 2.7 GHz to VHF IF Down-converter**
- **CMX973 RF Quadrature Transceiver for full demonstration of IF / baseband conversion**
- **Receiver LNA**
- **Option for IF SAW filter**
- **Powered by external 6.0V power supply**

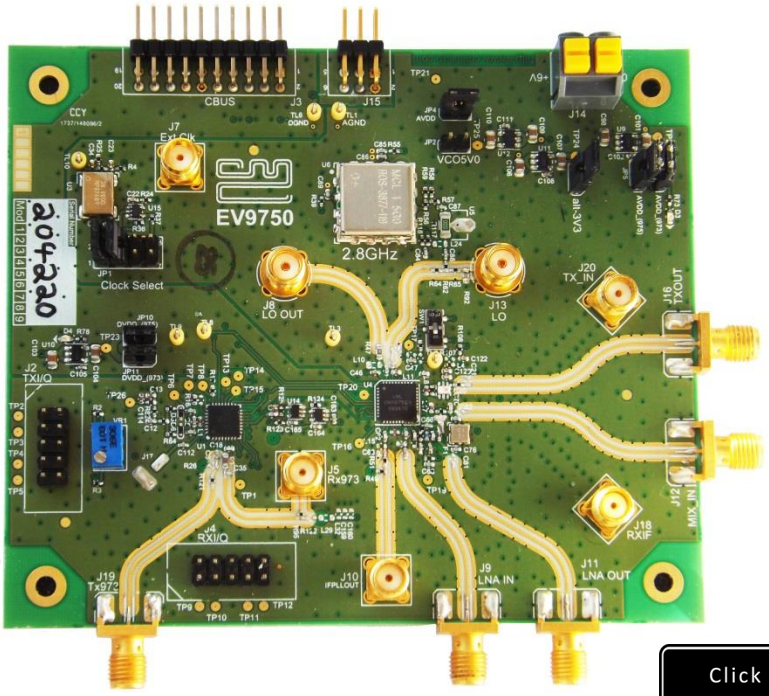

Figure 1 EV9750 board

Click here for:
- Latest Datasheet
- Product Data Resource

1 Brief Description

The EV9750 is a demonstration and evaluation platform for the CMX975. The CMX975 provides functionality consisting of RF PLL/VCO + IF PLL/VCO + Transmit Up-convert Mixer + Receive Down-convert Mixer + LNA. It has been designed to interface with the CMX973 to provide a simple and cost effective RF transceiver for operation in the range 1 to 2.7 GHz. The EV9750 design incorporates a CMX973 to allow conversion to and from the CMX975 IF frequencies to I/Q baseband signals.

The CMX975 provides a 700MHz to 6GHz 24-bit Fractional-N RF PLL and an internal RF VCO covering 2.8 to 3.6 GHz. A separate integer-N IF PLL and VCO for 900MHz is also provided. An inductor value change can configure the IF VCO to cover other frequencies.

The board includes all necessary voltage regulators and is operated from an external 6V dc supply. The EV9750 provides a 38.4MHz reference oscillator together with an additional off-chip VCO module. External frequency sources can also be configured to provide local oscillator signals for the CMX975 mixers.

The EV9750 interfaces to the PE0003 Universal Interface Card, to allow read and write access to the CMX975 and CMX973 C-BUS registers. A PC user interface is available for operational set-up and provides for use of control scripts.

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Figure Page

It is recommended that you check for the latest product datasheet version from the Products page of the CML website: www.cmlmicro.com.

This is Advance Information; changes and additions may be made to this document. Parameters marked TBD or left blank will be included in later issues of this document. Information in this advance document should not be relied upon for final product design.

2 History

Version	Changes	Date
1	First Issue	19th December 2017

3 Block Diagram

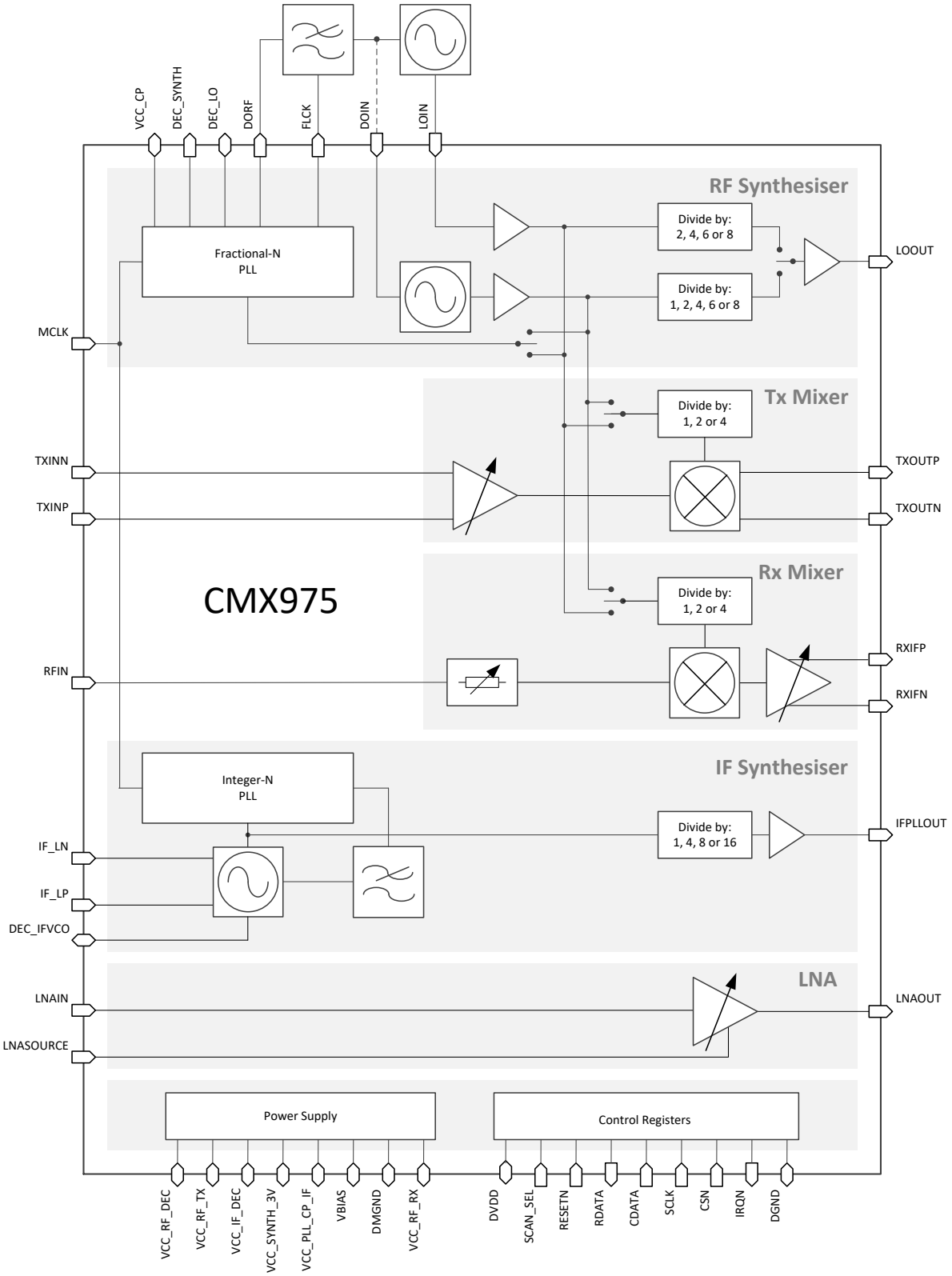

Figure 2 CMX975 Block Diagram

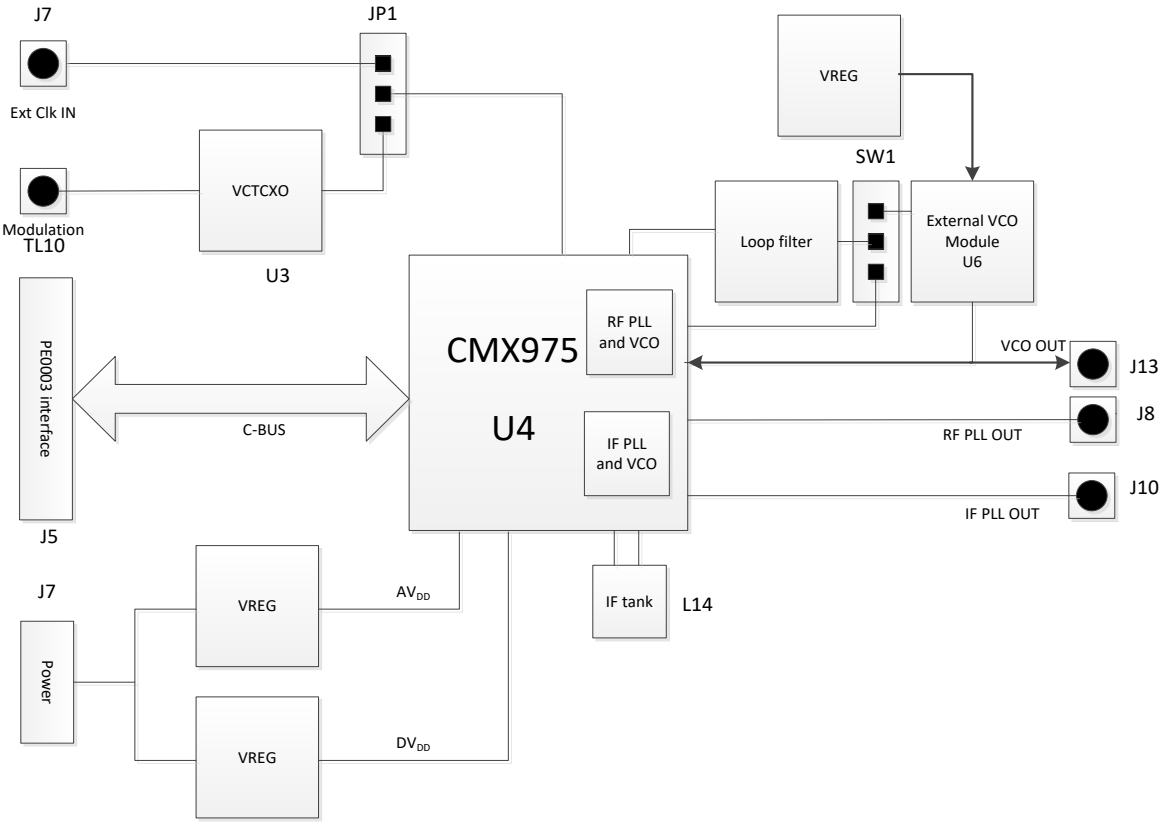

Figure 3 EV9750 PLL Block Diagram

4 Preliminary Information

The EV9750 provides a complete platform for demonstrating and evaluating the CMX975 (device U4).
This document refers to revision C of the EV9750 PCB (PCB593C).

4.1 Laboratory Equipment

The following items are recommended for evaluation of the EV9750:

- Laboratory power supply
- PE0003 controller
- Personal computer
- RF spectrum analyser
- RF signal generator
- Oscilloscope
- Baseband I/Q signal source (optional, if CMX973 is used)

For more detailed design or investigation work, additional RF test equipment may be required.

4.1.1 Power Supply

The input voltage to the PCB at J14 is nominally 6.0V. The 6.0V power supply should be rated at 300mA. On-board regulators provide the 3.3V and 5V supplies to the circuits used on the PCB.

NOTE: Care should be exercised with the 6.0V supply as there is the option to power the EV9750 directly from the PE0003 +5V supply via J15, although this is not fitted as standard. If J15 and L28 are fitted, an external supply should not be connected to J14. Operation of the VCO modules may be affected when the EV9750 is powered from the PE0003 due to the lower supply voltage. In order to apply an external supply with J15 fitted, L28 should be removed. Alternatively, the PE0003 could be run from the 6.0V supply.

4.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

4.2.1 SSD Devices

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

4.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK9750) and notify CML within seven working days if the delivery is incomplete.

4.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

5 Quick Start

This section provides instructions for users who wish to experiment immediately with this Evaluation Kit. A more complete description of the kit and its uses appears later in this document. The user should also read the appropriate CMX975 and CMX973 datasheets before using the EV9750 board.

Note: The EV9750 default configuration, as supplied, is as follows:

- CMX975 (U4): On-chip RF VCO
- U3: 38.4MHz on-board VCTCXO frequency reference without buffer
- CMX975 225MHz IF input / output to SMA connectors (J20 TXIF, J18 RXIF)
- CMX973 225MHz IF input / output to SMA connectors (J5 RXIF, J19 TXIF)
- 1.5GHz RF LNA input (J9), LNA output routed via SAW filter F1 to the RX mixer input
- 1.5/1.6GHz RF Tx mixer output (J16)

5.1 Setting-Up

The following procedure is recommended:

1. Connect the boards as shown in Figure 4.
2. Ensure that the power supply and reference oscillator selection links are correctly configured.
3. LO Output signals can be monitored by a spectrum analyser connected to J8 (LO Out), J13 (VCO module output) or J10 (IF PLL Out).
4. Apply power to the boards.

The boards are now ready for operation.

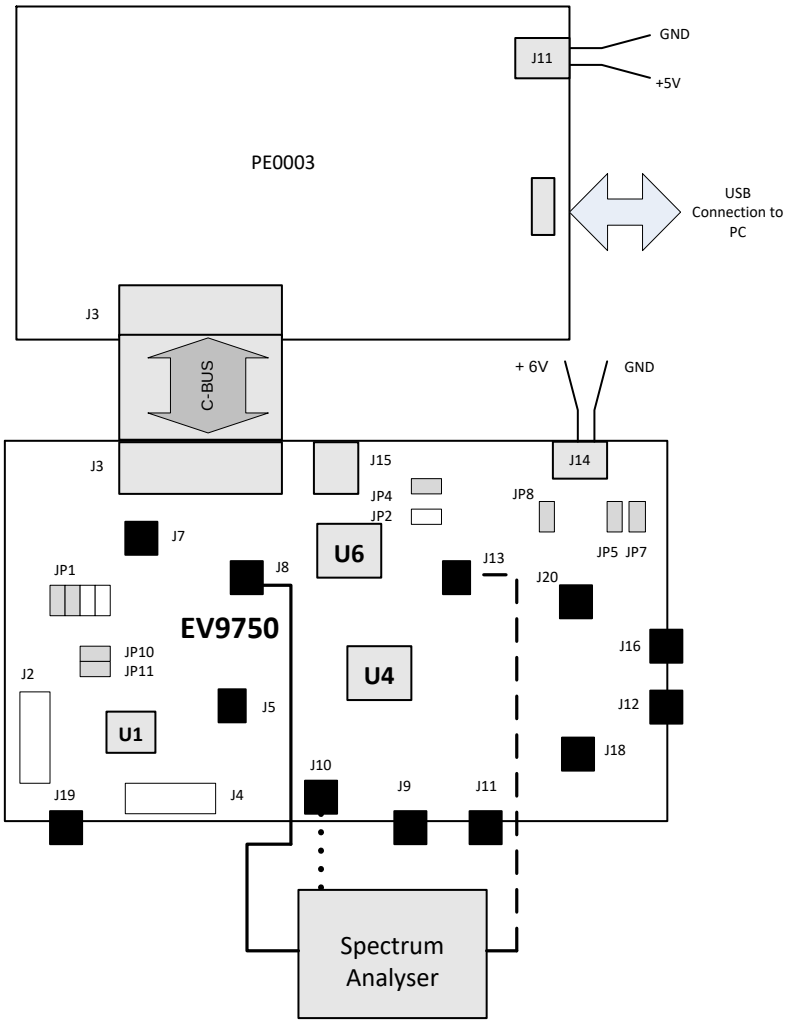

Figure 4 Typical PLL Evaluation Connections for EV9750

5.2 Adjustments

VR1 is a variable resistor used to adjust the dc bias voltage on two of the I/Q modulation inputs of the CMX973. VR1 has been adjusted for maximum carrier null during production testing and should not require user adjustment.

5.3 Operation

When power is applied to the EV9750, the CMX973 and CMX975 are both in reset. The C-BUS is common to both devices, each having a separate register set.

5.3.1 Receive down-converter

To evaluate the receiver system, connect the EV9750 as follows:

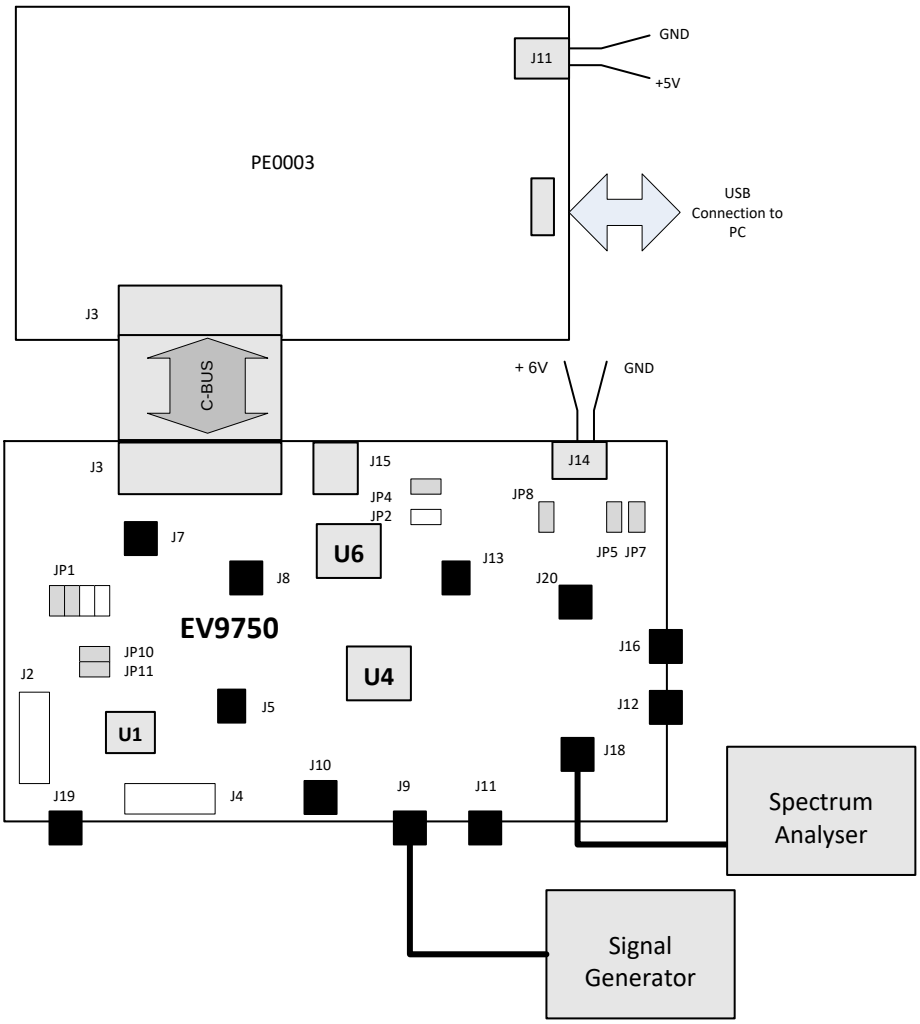

Figure 5 Typical Receiver Evaluation Connections for EV9750

This is for evaluation of the combined LNA, local oscillator and receive down-converter subsystem. The RF input is applied to the LNA input J9 with the IF output at J18. The LO is provided by the CMX975 on-chip VCO and PLL. Alternatively, an external LO source can be applied via J13 (with suitable configuration). In addition, the IF output at J18 can be connected to J5 to allow evaluation of a complete CMX975 /CMX973 RF to baseband receiver (see 7.1.10).

5.3.2 Transmit up-converter

To evaluate the transmitter system, connect the EV9750 as Figure 6.

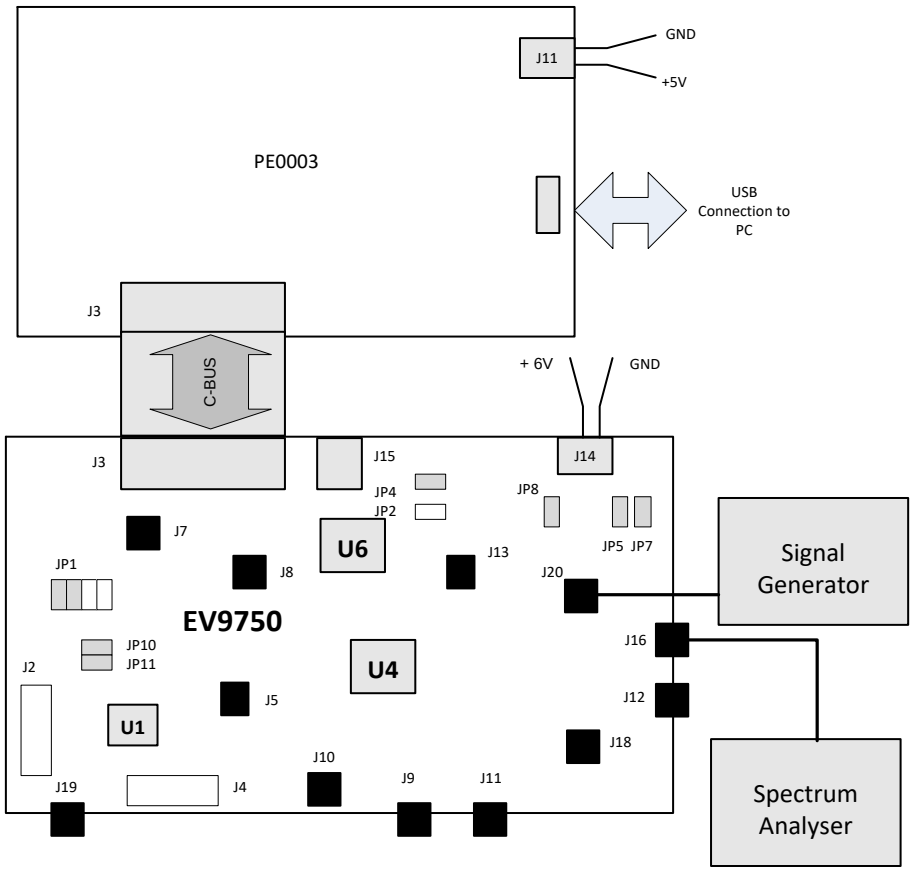

Figure 6 Typical Transmitter Evaluation Connections for EV9750

This is for evaluation of the combined LO and transmit up-converter subsystem. The RF input is applied to the IF input J20, with the RF output at J16. The LO is provided by the CMX975 on-chip VCO and PLL. Alternatively, an external LO source can be applied via J13 (with suitable configuration). In addition, the IF input at J20 can be connected to J19 to allow evaluation of a complete CMX975/CMX973 baseband-to-RF transmitter (see 7.1.10). Note the LO for the CMX973 modulator should be provided by the CMX975 IF PLL (or an external LO source).

5.3.3 Signal Lists

Connector Ref.	Signal Name	Signal Type	Description
J5	RX 973	RF	Input Rx IF signal to the CMX973
J7	EXT_CLK	RF I/P	External PLL reference clock input
J8	LOOUT	RF O/P	Output from the CMX975 RF PLL / dividers
J9	LNA_IN	RF I/P	Input to the LNA
J10	IFPLLOUT	RF O/P	Output from the IF PLL / dividers
J11	LNA_OUT	RF O/P	Port for testing the LNA output / input to SAW filter
J12	MIX_IN	RF I/P	Input to the CMX975 Down-convert Mixer
J13	LO	RF	Output from the VCO module (s) For use with an off-board VCO, this can also be configured to provide an input to the CMX975 RFPLL input dividers
J16	TXOUT	RF O/P	Output from the Tx Up-convert Mixer
J17	RXLO	RF I/P	Optional input for CMX973 RXLO
J18	RXIF	RF	Output from the CMX975 Down-convert Mixer
J19	TX 973	RF	Output Tx IF signal from the CMX973
J20	TX_IN	RF	Input to the CMX975 Up-convert Mixer

Table 1 RF Connector List

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J3	-	-	I/P & O/P	C-BUS control connection (see Table 3)
J14	1	+V	DC	6.0V Power supply input
J14	2	GNDA	DC	Power supply ground
J15	3-6 (C-F)	+5V_PE0003	DC	Connection to +5V supply from PE0003
J15	1-2 (A-B)	DGND	DC	Connection to Digital Ground for PE0003

Table 2 DC / Control Connector List

CONNECTOR PINOUT for J3				
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**	
1	RESETN	I/P	Hardware reset	Low to reset, pulled high by R48
2	CSN	O/P	Chip Select	
3	N/C		No Connection	
4	CDATA	O/P	Command Data	
5	N/C		No Connection	
6	SCLK	O/P	Serial Clock	
7	N/C		No Connection	
8	RDATA	I/P	Reply Data	
9	N/C		No Connection	
10	IRQN	I/P	Interrupt Request (open-drain)	
11	GNDD	Power	Connection to Digital Ground	
12	GNDD	Power	Connection to Digital Ground	
13 to 20	N/C		No Connection	

Table 3 External C-BUS Host Interface

CONNECTOR PINOUT for J15			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
A/1	DGND_PE0003	Power	Connection to Digital Ground for PE0003
B/2	DGND_PE0003	Power	Connection to Digital Ground for PE0003
C/3	+5V_PE0003	Power	Connection to +5V supply from PE0003
D/4	+5V_PE0003	Power	Connection to +5V supply from PE0003
E/5	+5V_PE0003	Power	Connection to +5V supply from PE0003
F/6	+5V_PE0003	Power	Connection to +5V supply from PE0003

Table 4 Optional J15 PE0003 Host DC connector

TEST POINTS		
Test Point Ref.	**Default Measure -ment**	**Description**
TP1		VCC for CMX973
TP2	-	Unused
TP3	-	Unused
TP4	-	Unused
TP5	-	Unused
TP6		CMX973 OA1O – Op Amp 1 output
TP7		CMX973 OA1N – Op Amp 1 - input
TP8		CMX973 OA1P – Op Amp 1 + input
TP9	-	Unused
TP10	-	Unused
TP11	-	Unused
TP12	-	Unused
TP13		CMX973 OA2O – Op Amp 1 output
TP14		CMX973 OA2N – Op Amp 1 - input
TP15		CMX973 OA2P – Op Amp 1 + input
TP16	-	VCC_PLL_CP_IF
TP17	-	DORF – RF PLL Charge pump output voltage
TP18	-	Unused
TP19	1.2 V	VBIAS
TP20	-	Unused
TP21	~ 6V	+V Input supply voltage
TP22	3.3 V	U9 Regulator Output (AVDD) for analogue supplies
TP23	3.3 V	U10 Regulator Output (DVDD) for digital supplies
TP24	3.3 V	U11 Regulator Output (AVDD) for Alt_3v3 analogue supply
TP25	5.0 V	U12 Regulator Output (VCO +5V) for the VCO module supply
TP26	-	CMX973 PLL Tuning voltage

Table 5 Test Points

TEST LOOPS		
Test Point Ref.	**Default Measurement**	**Description**
TL1, TL2, TL3, TL4	AGND	Connection to Analogue Ground
TL5, TL6	DGND	Connection to Digital Ground
TL7		FLCK – Fast Lock output
TL8		IRQN
TL9		RDATA
TL10		Modulation input for VCTCXO U3

Table 6 Test Loops

JUMPERS / SWITCHES		
Ref.	**Default Setting**	**Description**
JP1	Link pin 1 – 2 and pin 3 – 4	2 x 4 Pin field for selecting the clock reference source and buffering options. To use the on-board VCTCXO, un-buffered, link pins 1-2 & 3-4. To use the on-board VCTCXO, buffered, link pins 2-4 & 7-8. To use an external clock applied to J7, un-buffered, link pins 5-6 & 3-4. To use an external clock applied to J7, buffered, link pins 4-6 & 7-8.
JP2	Not linked	VCO5V0 – Analogue Supply - Link to enable VCO module
JP4	Linked	AVDD – Analogue Supply - Link to enable VCTCXO and buffer supplies
JP5	Linked	AVDD_975 – Link to enable CMX975 analogue supplies
JP7	Linked	AVDD_973 – Link to enable CMX973 analogue supplies
JP10	Linked	DVDD – Link to enable CMX975 digital supplies (C-BUS interface)
JP11	Linked	DVDD – Link to enable CMX973 digital supplies (C-BUS interface)
SW1	1	Surface mount switch to select routing of the PLL tuning voltage after the loop filter. To use the CMX975 internal VCO, select position 1. To use the external / off-chip VCO module, select position 2.

Table 7 Jumpers and Switches

Notes:

I/P	=	Input
O/P	=	Output
TL	=	Test Loop
TP	=	Test Point

6 Circuit Schematics and Board Layouts

For clarity, the circuit schematic diagrams are available as separate high-resolution files, which can be downloaded from the CML website. The layout on each side of the PCB is shown in Figure 7 and Figure 8.

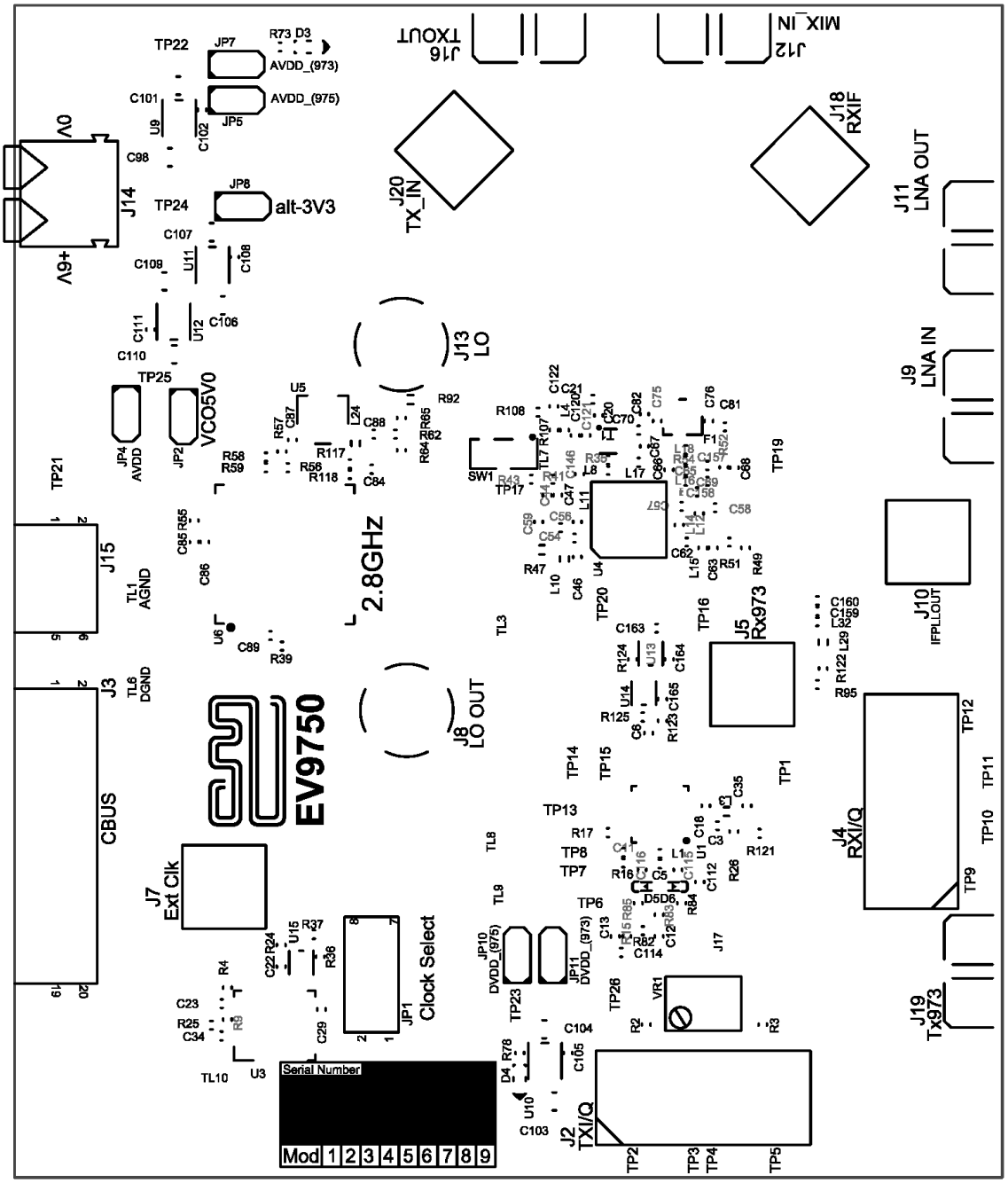

Figure 7 PCB Layout: top

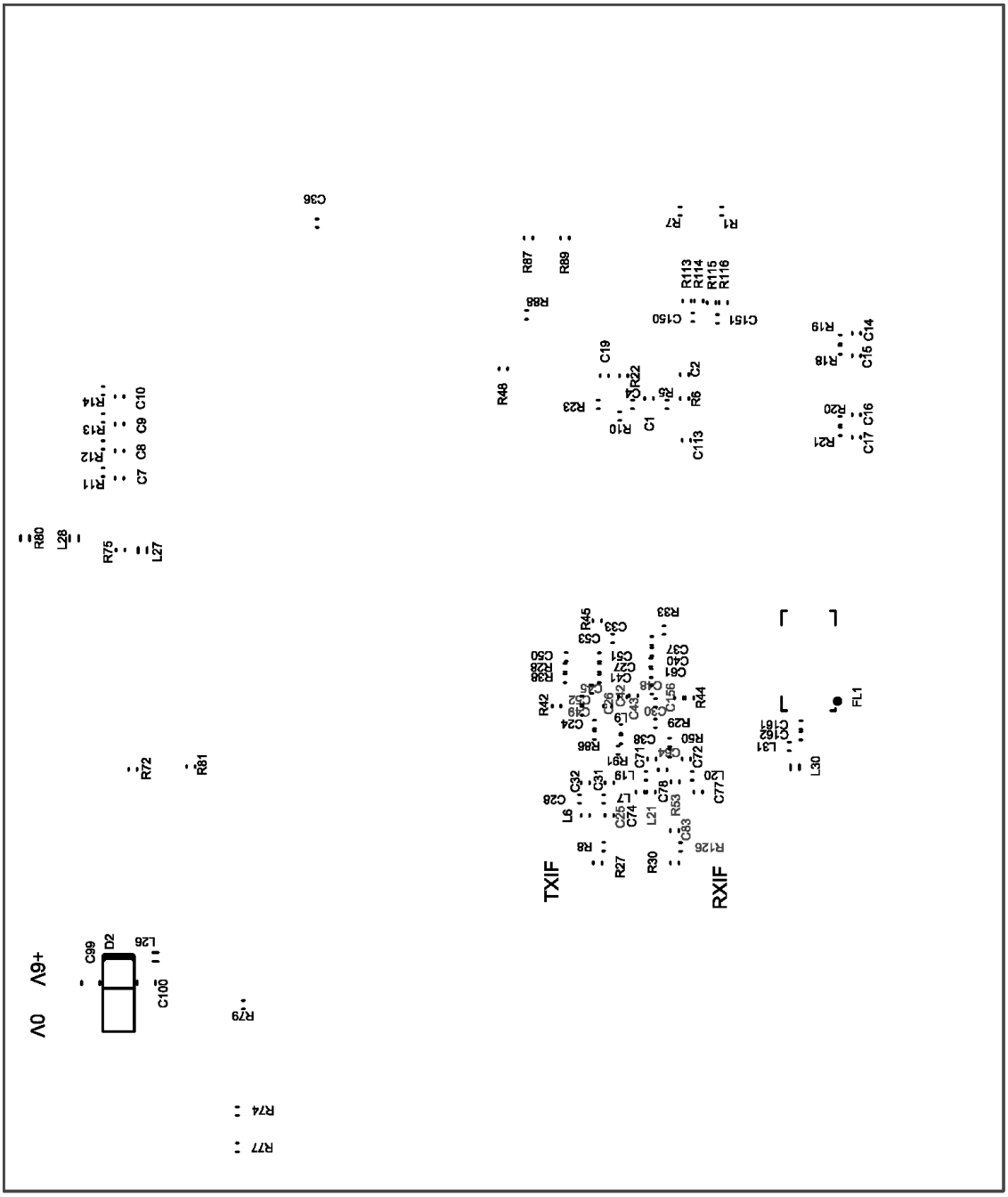

Figure 8 PCB Layout: bottom

7 Detailed Description

The EV9750 serves as a demonstrator for the CMX975, a 40-lead VQFN device at location U4.
EV9750 functionality includes:

- A VHF IF to 1 to 2.7 GHz Up-converter (tuned to ~1.6GHz output)
- A 1 to 2.7 GHz to VHF IF Down-converter (tuned to ~1.5GHz input)
- LNA tuned for 1.5GHz operation
- CMX973 up/down-conversion between I/Q baseband and the VHF IF.
- A 700 – 6000 MHz 16-/24-bit Fractional-N PLL
- VCOs for 2800 – 3600 MHz on-chip and 2800 - 2900 MHz or 3650 - 3800 MHz off-chip (dependent on module fitted).
- An IF VCO and Integer-N PLL centred at 900MHz (to provide a LO source for the CMX973).
- A 38.4MHz VCTCXO, plus external reference input.
- USB Interface via a PE0003 to a CML standard GUI, to allow script control.

7.1 Hardware Description

Full details of the silicon functionality are contained within the CMX973 and CMX975 datasheets. The EV9750 is assembled on a 111 x 93.5mm, 1.6mm thick 6 layer PCB (reference PCB593C), with the upper layer having a Rogers RO4003C ceramic substrate for low loss and consistent high frequency performance. The other layers use FR4 / VT481 2116 dielectric.

In general, high frequency (>1GHz) RF components, connectors and configuration links have been placed on the top layer, with lower RF frequency components, voltage regulators, supplies and decoupling for the CMX973 and CMX975 on the bottom layer. The layout has been optimised for low ground impedance and short RF tracking for operation at high frequencies. Gerber and Bill of Material data can be downloaded from the CML website.

High frequency SMA edge connectors are used for the J9 and J12 inputs and J8, J16 and J19 outputs with Grounded Co-Planar Wave Guide transmission lines. J8 and J13 are also high-frequency SMA types.

7.1.1 Tx Up-Convert Mixer

The Tx up-convert mixer within the CMX975 takes the Tx IF input (as default tuned for 225MHz) at J20 and translates this to 1 to 2.7 GHz (default tuned for 1.5 to 1.6 GHz). The mixer input is provided as a differential signal via a discrete balun network. The differential mixer output is provided as a single ended output at J16 via a wide band ceramic balun T1 and a matching network. This balun also provides dc supply to the mixer output pins. As supplied, the mixer is configured to operate in image reject mode. With changes to the input matching values, a lower current 'normal mode' mixer setting can be used. The mixer has three gain settings available. Note that for optimum performance at 2.7GHz, T1 should be changed for a different value (refer to Datasheet).

7.1.2 LNA

The CMX975 incorporates a Low Noise Amplifier with an input at J9. With the default component values on the EV9750, the amplifier is tuned for 1.54GHz. As supplied, the capacitor C158 is connected between C157 and VBIAS (to the pad P51 provided) to improve higher frequency stability. An additional 100Ω resistor across the track to/from the LNAOUT pin (between L16 and the C22 input) is also fitted for unconditional stability at higher frequencies. The LNA has 4 gain settings and a noise figure around 1.8dB. With a change in component links, the output can be monitored at J11. The default configuration however is for the output to go to the SAW filter F1.

7.1.3 SAW filter

A SAW filter (location F1) from Golledge (MP04630), covering 1525 to 1560 MHz, provides further image and spurious filtering between the LNA output and the down-convertor mixer input. This can be removed and bypassed with a 0Ω 0603 across the input to output pads if required.

7.1.4 Rx Down-Convert Mixer

The Rx down-convert mixer within the CMX975 takes the Rx RF input at 1 to 2.7 GHz and translates this to a VHF IF. The default configuration is for a single-ended input from the SAW filter F1, with the input match tuned for 1.5GHz operation. Note that the RFIN pin must have a dc path to ground on its input as part of the matching arrangement. By moving C75 to the C82 location, the signal routing can be reconfigured to apply the mixer input at J12 rather than from F1. The differential output plus dc feed arrangement is tuned for 225MHz via a discrete balun arrangement. The mixer can operate in normal or image reject modes, with four gain settings available. The output is available at J18.

7.1.5 Local Oscillator

The LO (Local Oscillator) source for the up and down mixers can use the on-chip VCO/PLL, an off chip VCO (U6) locked using the PLL or an external LO source via J13. It is possible to configure one mixer to use the on-chip VCO as an LO and

configure the other mixer to use an external LO source. A number of possible LO modes or combinations are available (see datasheet). Note that the LOIN pin must have a dc path to ground on its input as part of the matching arrangement. The input J13 can serve as either an LO input for the mixers or as an input from an off-board VCO to be locked with the CMX975 PLL.

7.1.6 RF VCO /PLL

The CMX975 contains a 16- or 24-bit Fractional-N PLL synthesiser, which can be used with the on-chip 2800 to 3600 MHz VCO or with an external VCO module. The loop filter is external to the IC and (optionally) can incorporate a fast locking function, see Figure 9. The loop filter output can be routed back to the tuning input of the internal VCO, or either external VCO module, via switch SW1. The on-chip VCO output is available off-chip either as a fundamental or divided by 2, 4, 6 or 8 at J8.

Note that, if used with an off-chip VCO, the LOIN pin must have a dc path to ground on its input as part of the matching arrangement.

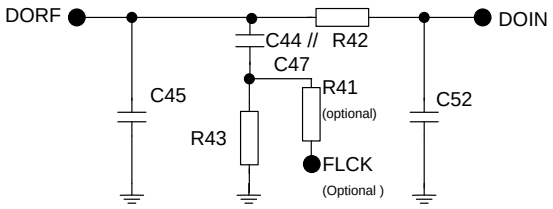

Figure 9 Example External Components – VCO External Loop Filter

VCO Frequency	C45	C44 // C47	C52	R43	R42	R41 (optional FLCK)
2.925GHz	750pF	6.2nF	27pF	1.6kΩ	5.1kΩ	See Datasheet section 7.3.4
3.5GHz	470pF	3.6nF	22pF	2.4kΩ	6.8kΩ	See Datasheet section 7.3.4
3.2GHz	680pF	5.6nF	27pF	2.2kΩ	5.6kΩ	See Datasheet section 7.3.4
3.2GHz Values Fitted (wider loop)	39pF	390pF	10pF	5.6kΩ	12kΩ	See Datasheet section 7.3

Note: C44, C45, C52, R42 and R43 assume a Kvco=70MHz/V, Icp=400µA, FComp=19.2MHz. The 3.2GHz values shown are a compromise for mid-band operation, with a nominal loop bandwidth of 60kHz. The values fitted give a wider loop bandwidth of nominally 200kHz, showing improved in-loop noise. These values may require modification for use with other off-chip VCOs.

Table 8 3rd Order Loop Filter values for a VCO frequency of 2.925GHz/3.5GHz

7.1.7 IF PLL/VCO

The CMX975 incorporates an additional IF VCO and PLL with internal loop filter. The VCO is tuned by external inductor L14; with the default value fitted the tuning range is centred around 900MHz. The output is available at the SMA connector J10. This signal is used as the LO source for the CMX973 with R49 fitted.

7.1.8 Reference Oscillator

U3 is a low phase noise GTXO-74V/JI 38.4MHz VCTCXO reference, part number MP07489, supplied by Golledge (www.golledge.com). This is used as the reference for the RF and IF PLLs within the CMX975 (MCLK). Options are provided to use an external reference signal applied to the SMA connector J7. These inputs can also be buffered via U2. The selection of this buffering is via the link configuration field JP1. The VCTCXO tuning input can be accessed via the test loop TL10, to allow the addition of a modulating signal within the PLL bandwidth.

To minimise spurious when using an external reference source, the on-board reference U3 can be disabled by removing the jumper link JP4.

The 38.4MHz reference is divided by 2 using U14 to provide a 19.2MHz reference to the CMX973.

7.1.9 External VCOs

The EV9750 has a 0.5" / 16-pin footprint for an external VCO module (U6). The type fitted is either a Mini-Circuits ROS-3000-619+, tuning approximately 2750 to 2925 MHz, or a ROS-3877-119+, tuning approximately 3650 to 3800 MHz with the available tuning voltage. The VCO can be selected via link JP2 (power) and SW1 (tuning voltage routed to the VCO

module in position 2) to operate with the CMX975 RFPLL. The output from the VCO module can be monitored after an attenuator, optional amplifier, and 6dB resistive splitter at connector J13. A divided version can also be available from the LOOUT pin at connector J8. Note that, with an external LO or off-chip VCO, either Rx or Tx also needs to be enabled in the General Control Register ($31) to enable LOOUT. Feedback to the CMX975 RFPLL is via a matching network for optimum input sensitivity.

In order to use an off-board VCO, JP2 should be removed to disable the VCO module. TP17 can then be used as a tuning voltage output. A screened connection is recommended to reduce noise pick-up. The final pole of the loop filter should be applied at the VCO tuning input. The feedback to the RFPLL input dividers can be applied to J13. Note that the resistive splitter (R62, R64, R65) may need to be configured as a 0Ω through link from J13 to C59, depending on the signal level present and the loading by the on-board VCO module. Alternative matching values to the LOIN pin (L12, C56, C59) will be required for higher frequency operation; for details refer to the CMX975 datasheet.

7.1.10 CMX973

The CMX973 RF quadrature transceiver (U1) allows conversion of the CMX975 Rx down-convert mixer IF output (supplied configured for 225MHz) to baseband I/Q. The input at J5 is matched to the CMX973 input by the Pi network around L3. The received I/Q differential baseband signals are available on connector J4.

Similarly, the CMX973 allows conversion from a baseband I/Q input to a VHF IF signal which can then drive the CMX975 Tx up-convert mixer. Single ended transmit I and Q signals should be applied to J2:2 (TXI_P) and J2:8 (TXQ_P). The TXI_N and TXQ_N have dc bias applied via VR1 and R2 / R3. If R2 and R3 are removed, true differential I and Q signals can be applied to J2. There is an option to filter the I/Q input signals via the networks R113 to R116. The VHF output is then available at J19.

Note that the CMX973 TX IF output can be linked to the CMX975 TX IF input by fitting R8 and R26 as an alternative to connecting J19 to J20 via coaxial cable. Similarly, the CMX975 RX IF output can be linked to the CMX973 RX input via the optional 225MHz SAW filter FL1 (Vectron TFS225E). FL1 and the associated matching components are however not fitted as standard.

The CMX973 has an on-chip VCO and PLL operational at 450MHz for receive operation. This should be disabled and an IF LO provided by the CMX975 IF VCO / PLL at 900MHz for improved transmit performance. This requires the fitting of R49 (0Ω fitted as default). The 19.2MHz reference for the CMX973 can be disabled by removing R123.

7.1.11 Power Supplies

The input to the PCB is nominally 6.0V (absolute limits: 5.5V to 8V) applied to J4. Reverse polarity protection is provided by D2. On-board regulators (U9, U10, U11, U12) are provided to generate the 3.3V and 5V supplies used on the EV9750. A green LED on the digital supply (D3) can confirm that power is correctly applied.

7.1.12 Inductors

All inductors used in the RF sections of the design are manufactured by Coilcraft (www.coilcraft.com). Performance of the circuits with inductors from other manufacturers may vary.

7.2 Adjustments and Controls

7.3 Script/GUI Control

To investigate the performance and features of the EV9750 in more detail, a Windows GUI can be used to control the CMX975 and CMX973 via a PE0003 Universal Interface Card – either by manual register accesses or by running scripts. The GUI can be found in 'ES9750xx.zip'.

Setting-Up

- Copy the file 'ES9750xx.zip', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect a dc supply to the PE0003 Interface Card and set supply voltage level to 5V / 500mA current limit.
- Connect a dc supply to the EV9750 Evaluation Board and set the voltage level to 6V / 250mA current limit.
- Attach a USB cable between the PE0003 Interface Card and the USB port of the PC.
- Turn on the power supplies.

Install the USB driver when requested. The driver is in the same folder as the 'ES9750xx.zip' files were extracted to (..\Driver). Follow instructions on the screen to install the USB driver.

The executable ES9750xx.EXE can now be run. This software allows the user to select between Evaluation Kits for the CMX975 and CMX979 devices. Select the radio button for the EV9750.

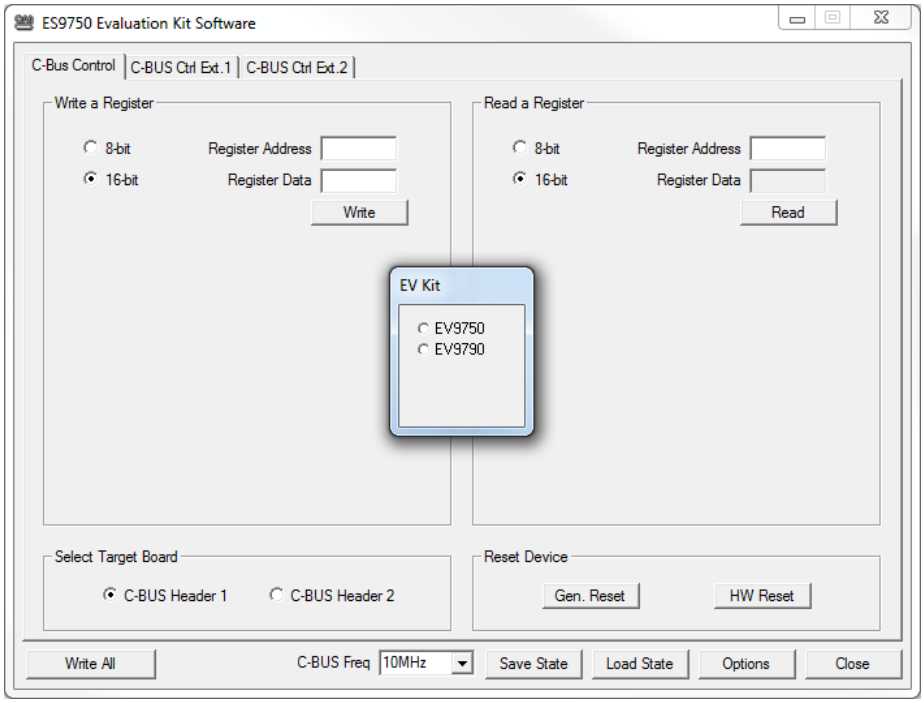

Figure 10 CMX975/CMX979 Selection

There are nine sheets within the tabbed dialog box structure. These are described in the following sections.

7.3.1 The C-BUS Control Tab

This tab provides basic C-BUS read, write and general reset functions. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The radio buttons select an 8-bit or 16-bit read/write operation. The lengths of the entered values are limited to 2 characters (1 byte) for read or write register addresses and 2 or 4 characters (1 or 2 bytes) for the register write data. The General Reset button writes 00H to the CMX975 device.

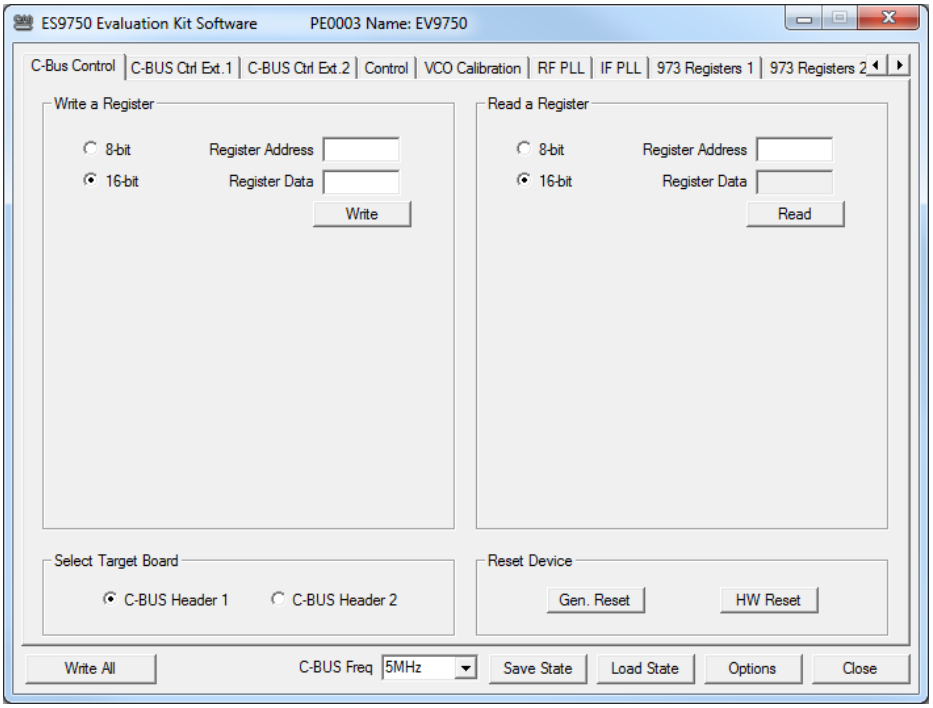

Figure 11 C-BUS Control Tab

7.3.2 The C-BUS Control Extended Tab (C-BUS Ctrl Ext. 1 and C-BUS Ctrl Ext. 2)

These tabs provide multiple C-BUS read and write functions. Each row in the table represents a single action on a C-BUS register. Select the C-BUS register type from the drop down list. The Update button and the Data edit box will be configured according to the selection. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The lengths of the entered values are limited to 2 characters (1 byte) for register addresses and 2 or 4 characters (1 or 2 bytes) for the register data. Click the Update button to read or write a single C-BUS register. For multiple C-BUS read or write operations, select the C-BUS registers using the Enable check boxes and click on the 'Wr all', 'Rd all' or 'Wr\Rd all' buttons. Click on the 'Wr all' button to write all the selected write type C-BUS registers. Click on the 'Rd all' button to read all the selected read type C-BUS registers. Click on the 'Wr\Rd all' button to read or write all of the selected C-BUS registers.

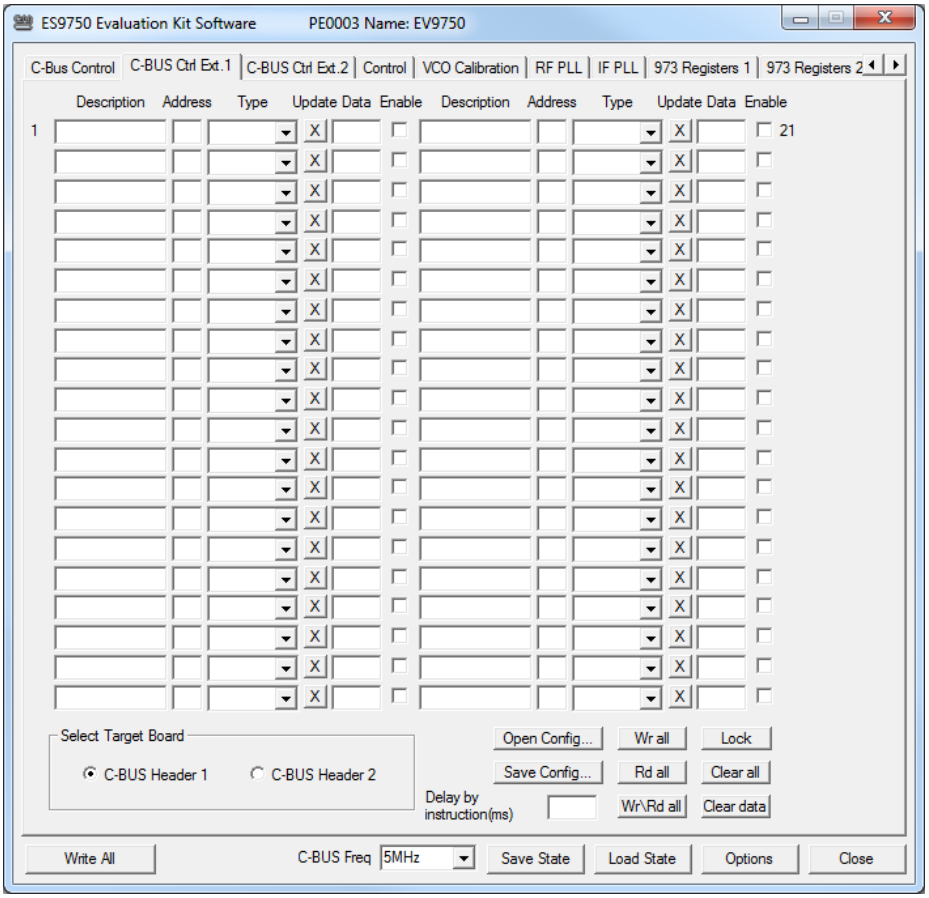

Figure 12 C-BUS Control Extended 1 Tab

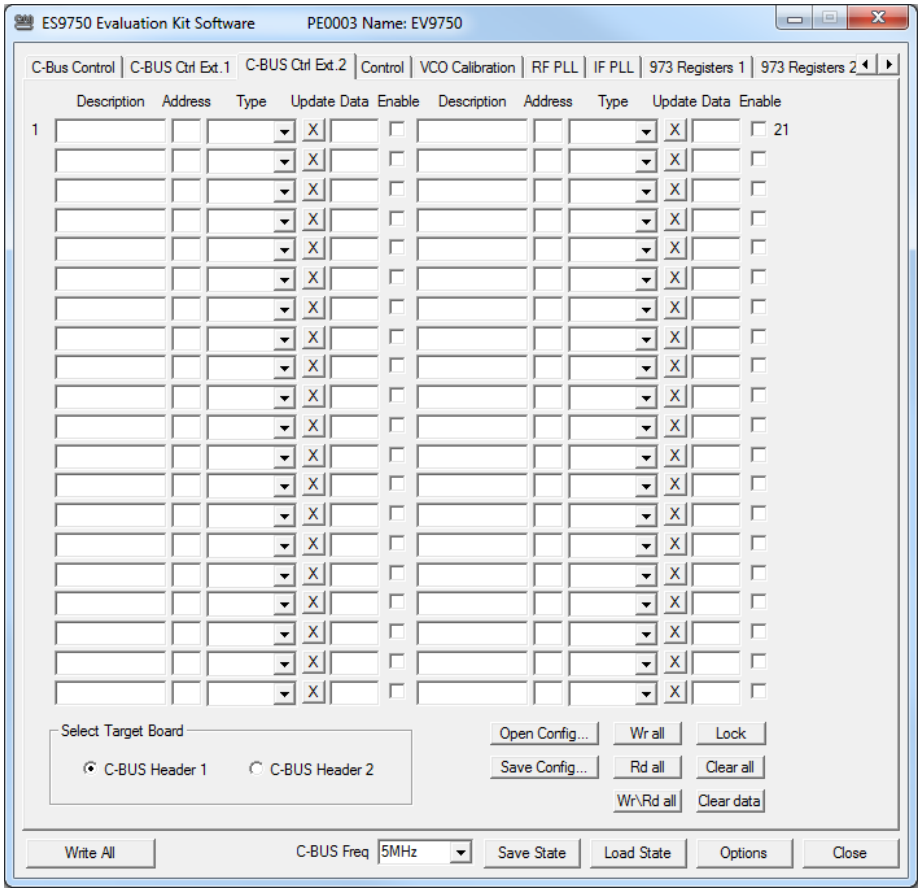

Figure 13 C-BUS Control Extended 2 Tab

The C-BUS actions in the table are executed sequentially, starting at "1" (top left of the table). The 'Delay by instruction (ms)' box (in the 'Extended 1' tab) introduces a delay between the execution of each C-BUS action (default = no delay).

Click on the 'Clear all' button to reset the table. Click on the 'Clear data' button to reset the Data edit boxes.

The 'Lock' button may be used to disable the Description, Address and Type controls, preventing accidental changes. Click on the 'Lock' button again to re-enable these controls.

Use the 'Save Config…' button to save the current table. The Description, Address, Type, Data and Select columns are saved in the specified file. Use the 'Open Config…' button to load a previously saved table.

7.3.3 The General Control Tab

This tab provides access to registers for general control of the device functions, e.g. to write to the General Control register and read back from the Device Status register.

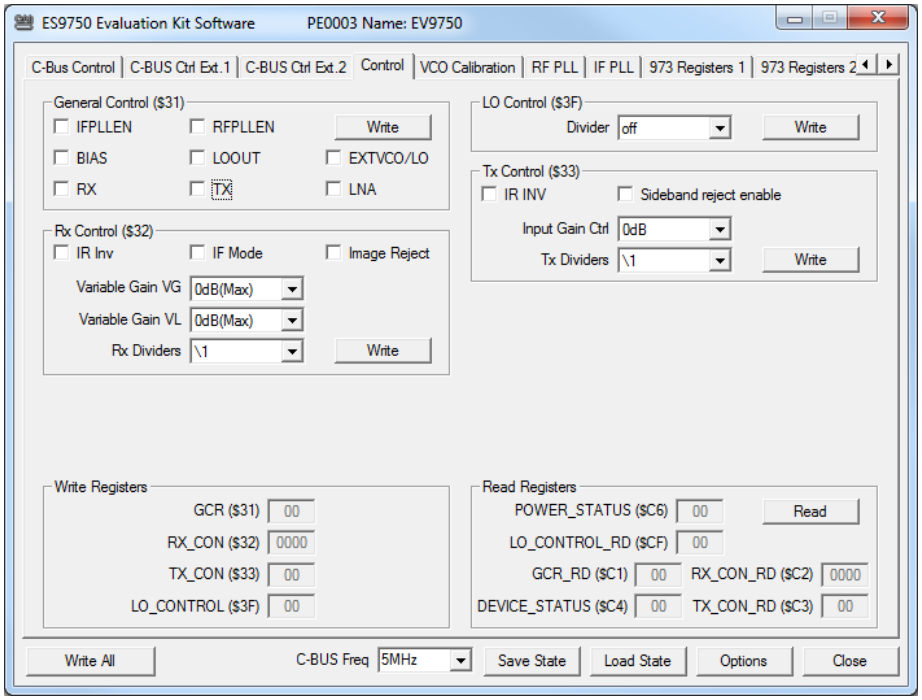

Figure 14 General Control Tab

7.3.4 The VCO Calibration Tab

This tab provides access to the RF and IF VCO calibration controls.

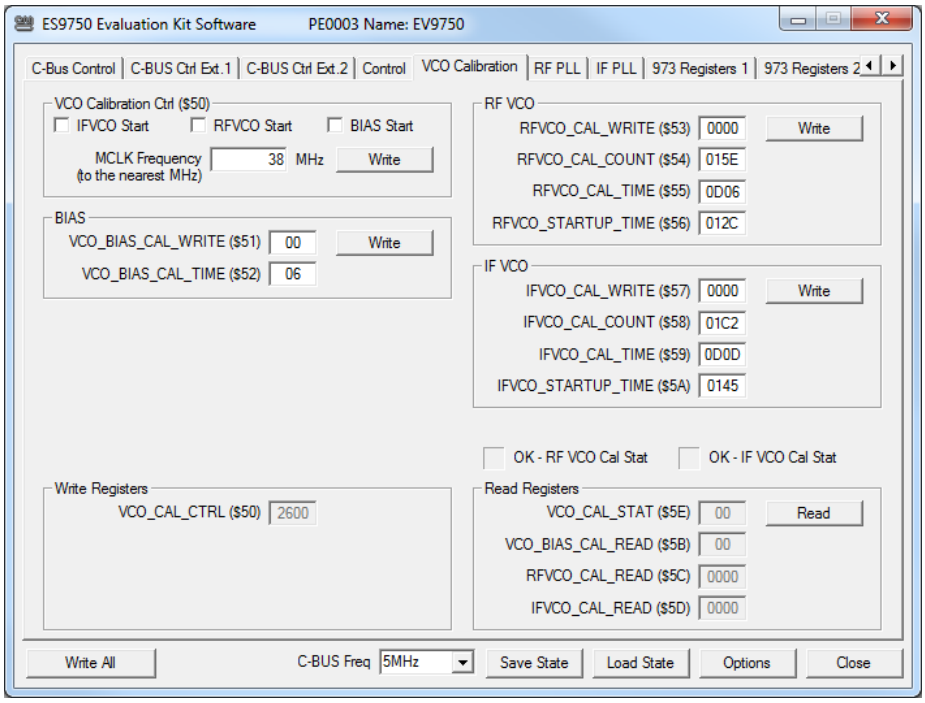

Figure 15 VCO Calibration Tab

7.3.5 The RF PLL Tab

This tab provides access to the RF PLL functions. This includes a calculator to determine the register values for a given reference (MCLK), comparison and wanted VCO output frequency.

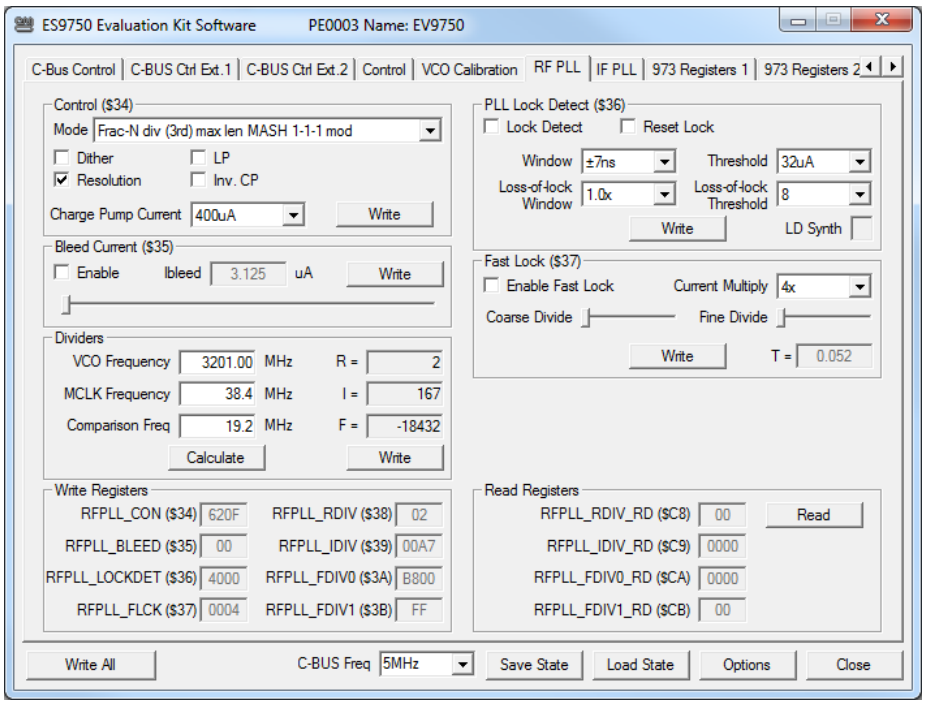

Figure 16 RF PLL Tab

7.3.6 The IF PLL tab

This tab provides access to the IF PLL functions. This includes a calculator to determine the register values for a reference (MCLK), comparison and wanted VCO output frequency.

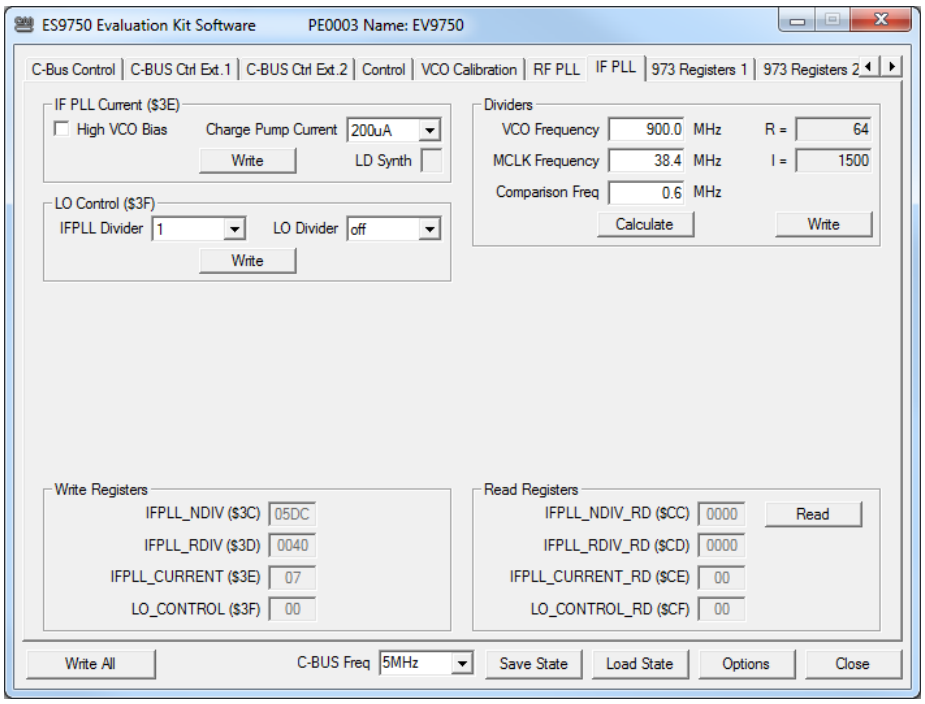

Figure 17 IF PLL Tab

7.3.7 The CMX973 tabs

These two tabs provide access to the CMX973 registers and include the ability to control parameters such as the Tx LO frequency and I/Q DC offsets.

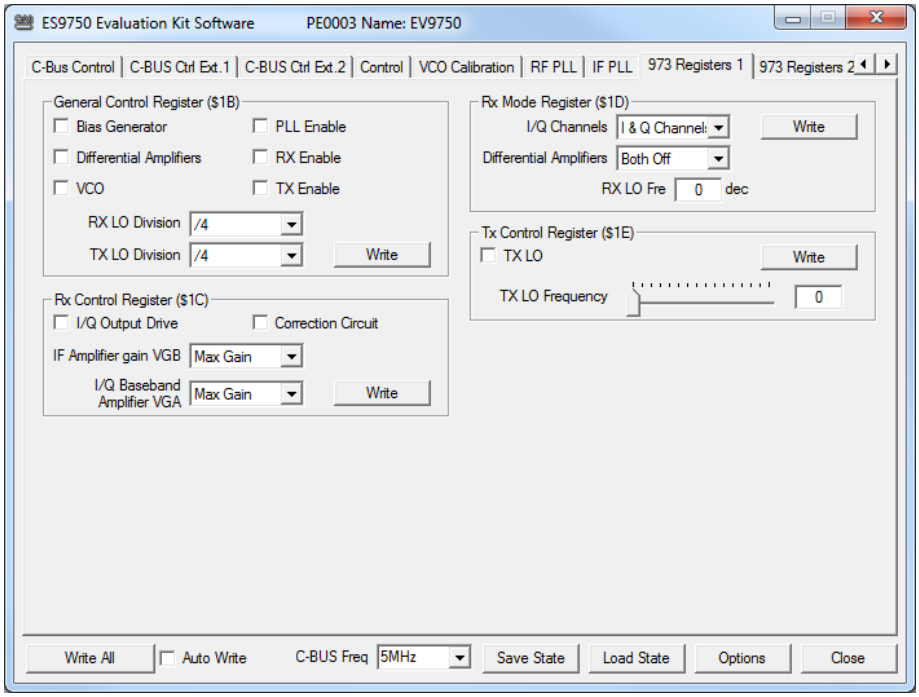

Figure 18 CMX 973 Registers Tab 1

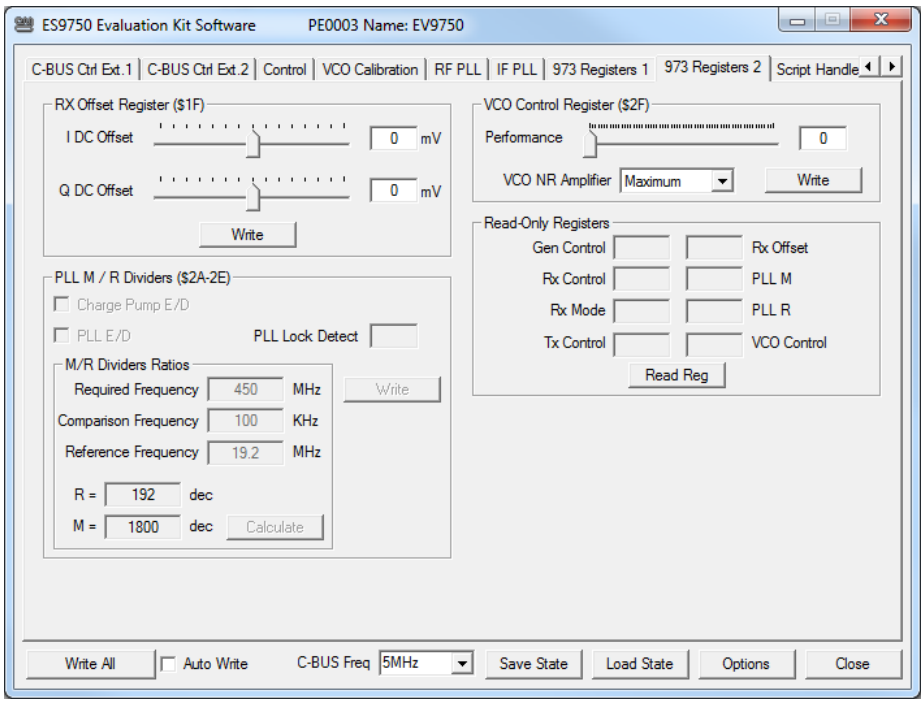

Figure 19 CMX973 Registers Tab 2

7.3.8 The Script Handler tab

The Script Handler tab allows the execution of scripts. These are plain text files on the host PC which are compiled by the GUI, but executed on the ARM Microprocessor on the PE0003. The script language is documented separately in the "Script Language Reference" document, which can be downloaded with the PE0003 support package from the CML website at www.cmlmicro.com. The following are demonstration scripts developed for the EV9750 Evaluation Kit:

EV9750_RFPLLtest.pes

This script enables the CMX975 internal RF VCO, performs a calibration and locks the RF PLL at 3580MHz. The output is available, divided by two (i.e. 1790MHz) on connector J8.

EV9750_IFPLLtest.pes

This script enables the CMX975 IF VCO, performs a calibration and locks the IF PLL at 901.2MHz.

EV9750 Tx1 .pes

This script enables the CMX975 internal RF VCO, performs a calibration and locks the RF PLL at 3510MHz. This provides an LO of 1755MHz for the image reject mixer. The IF at 225MHz mixes with this to produce an output of 1530MHz.

Rx System_975_01.pes

This script programs the CMX975 LNA, Rx Mixer and RF PLL + VCO for use as a receiver front end sub-system with a 1.5425GHz RF input and a 225MHz IF output. The LNA and Rx Mixer will be programmed for maximum gain with the Rx Mixer acting as an image reject mixer. The Rx Mixer obtains its local oscillator input from the 975's RF PLL synthesiser + VCO operating in 16-bit fractional-N mode. The LO is high side relative to the 1.5425GHz RF input. It is necessary to connect the EV9750 board in default configuration with the LNA output connected through the 1542.5MHz SAW filter to the Rx Mixer input.

Tx system_975_01.pes

This script programs the CMX975 Tx Mixer and RF PLL + VCO for use as a transmitter upconverter sub-system with a 225MHz IF input and a 1.626GHz RF output. The Tx Mixer will be programmed for maximum gain as an image reject mixer and obtains its local oscillator input from the 975's RF PLL synthesiser + VCO. The RF PLL will operate in 16-bit fractional-N mode and will provide a LO which is low side relative to the 1.626GHz RF output. The EV9750 board hardware is required to be connected in default configuration.

To select a script file, click on the 'Select Script' button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the '>' button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the 'Save Results' or 'Clear Results' buttons, respectively. When a script file is being executed, the 'Run Script' button will change to be the 'Abort' button, the rest of the tab will be disabled and the other tabs cannot be selected.

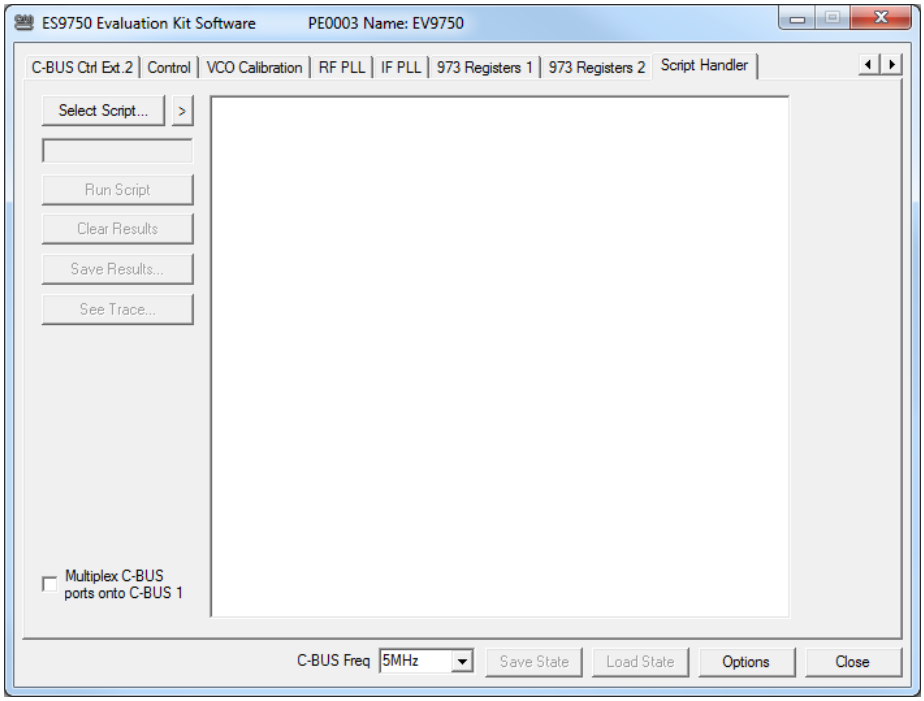

Figure 20 Script Handler Tab

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Click on the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.

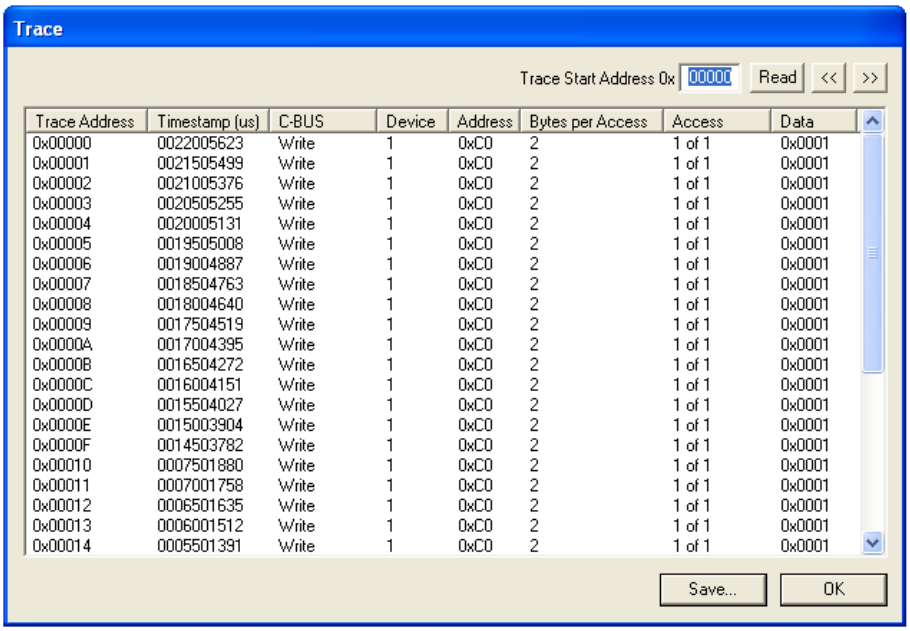

Figure 21 Trace Dialog Box

Click on the '>>' or '<<' buttons to upload and display the next or previous C-BUS transaction data block. Click on the 'Read' button to upload and display the C-BUS transaction data block starting at the address displayed in the Trace Start Address edit box. Use the 'Save…' button to save the trace data to a file.

7.4 Application Information

See Section 5.1 for board setup details and Section 5.3 for operation of the EV9750.

7.4.1 Typical Performance

Typical performance for the EV9750 is shown below.

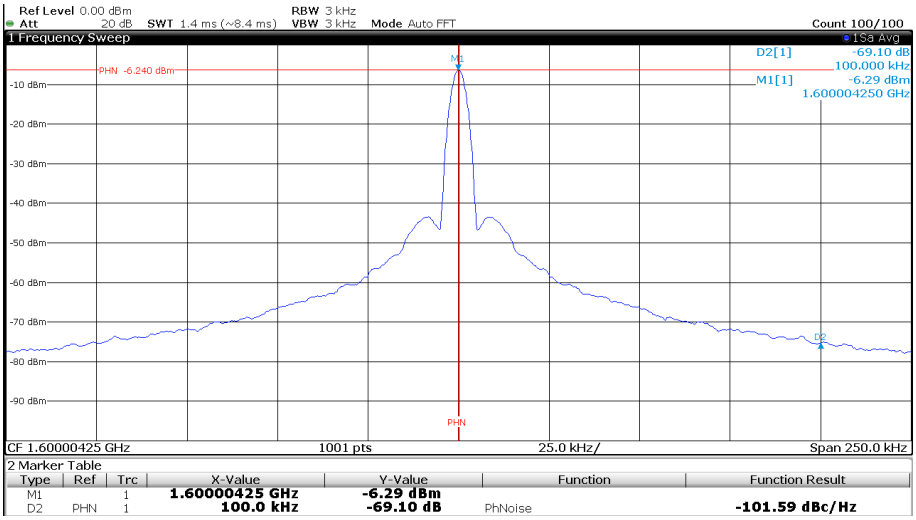

Figure 22 Typical RF VCO phase noise, J8 output at 1.6GHz, 100kHz offset, Fractional-N mode using 3.2GHz loop filter values, 50µA charge pump current

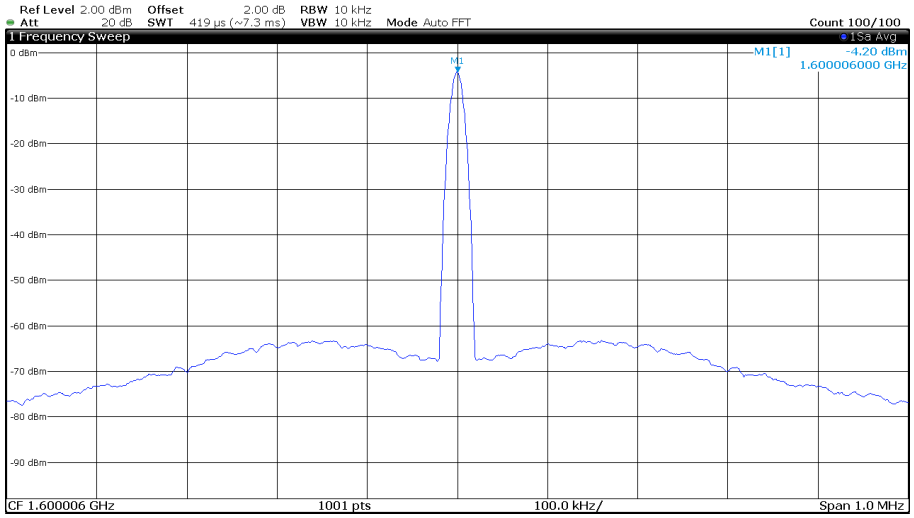

Figure 23 Typical RF VCO output at J8, 1.6GHz, Fractional-N mode using 3.2GHz wide loop filter values, 400µA charge pump current, 38.4MHz comparison frequency

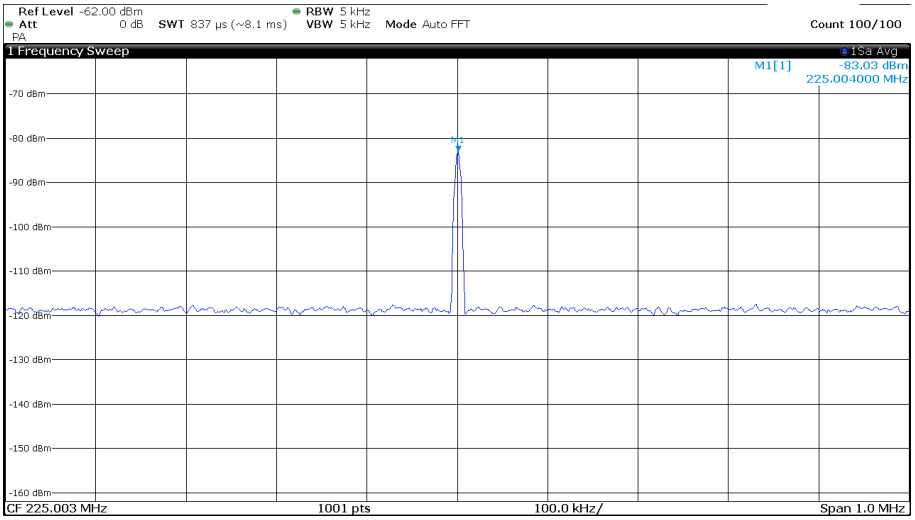

Figure 24 Typical Rx IF output (J18), 225MHz from 1542MHz /-100dBm input to the LNA (J9), showing 17dB gain from the LNA, SAW filter and image reject mixer cascaded.

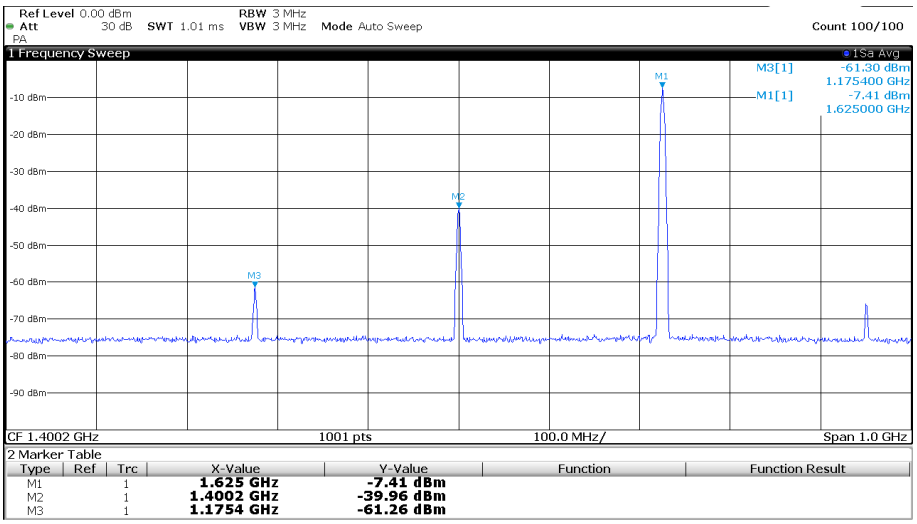

Figure 25 Tx Image Reject mixer output at 1.6GHz (J16), -10dBm input to J20 showing LO and image rejection, output at 1.625GHz

7.5 Troubleshooting

The EV9750 is a complex RF system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the CMX975 datasheet, along with the User Manuals, associated schematics and layout drawings for the EV9750 board when troubleshooting. This section provides suggestions to help users resolve application issues that may be encountered.

7.5.1 RF PLL Operation

Error Observed	Possible Cause	Remedy
On-chip VCO calibrating but not locking.	SW1 not in the correct position.	Ensure SW1 is in position 1 for using the internal CMX975 RF VCO.
External VCO module not locking	SW1 not in the correct position.	Ensure SW1 is in position 2 for using the external VCO module U6.
PLL output unstable/ noisy but on frequency	Unstable/low reference level	Check input reference levels and level. Check operation using the default on-board reference.
	Loop instability	The programmed values may give a high gain peak. Check the loop components fitted and reprogram with a higher charge pump current or comparison frequency.
No RF output or significantly off frequency	RFVCO calibration not performed	Perform calibration
RF output significantly off frequency but RF VCO Cal Status OK and locking	Fractional N mode not selected where RF frequency is not an integer multiple of comparison frequency	Select a Fractional N mode
No RF output or significantly off frequency and RF VCO Cal Stat not OK	Selected comparison frequency less than 4.8MHz	Choose comparison frequency to be a minimum of 4.8MHz for calibration.
LO Out is selected but no output from LO Out when using an off-chip VCO or External LO	Rx or Tx mixers not selected in General Control Register	Select either Rx enable or Tx enable in General Control Register

Table 9 RF PLL – Possible Errors

7.5.2 IF PLL Operation

Error Observed	Possible Cause	Remedy
PLL output unstable/ noisy but on frequency	Loop instability	The programmed values may give a high gain peak. Check the loop components fitted and reprogram with a higher charge pump current or comparison frequency.
IF output significantly off frequency but RF VCO Cal Stat OK and locking	Programmed IF frequency is not an integer multiple of comparison frequency	Choose appropriate comparison frequency
No IF output or significantly off frequency	IFVCO calibration not performed	Perform calibration

Table 10 IF PLL – Possible Errors

7.5.3 LNA Operation

Error Observed	Possible Cause	Remedy
Low output	Rx mode parameters (e.g. VG, VL) incorrectly selected in Rx Control Register	Select and re-write appropriate parameters

Table 11 LNA - Possible Errors

7.5.4 Rx Operation

Error Observed	Possible Cause	Remedy
No IF output	LO Source not selected (if using external) or LO at incorrect frequency or Rx dividers not correctly selected for Rx mode	Check selection of LO source and frequency. Check dividers.
Low IF output	Rx mode parameters incorrectly selected, e. g. gain, IR Invert, Image Reject	Select and re-write appropriate parameters

Table 12 Rx Operation - Possible Errors

7.5.5 Tx Operation

Error Observed	Possible Cause	Remedy
No RF output	LO Source not selected (if using external) or LO at incorrect frequency or Tx dividers not correctly selected for Tx mode	Check selection of LO source and frequency. Check dividers.
Low RF output	Tx mode parameters incorrectly selected, e. g. gain, IR Invert, Sideband Reject enable	Select and re-write appropriate parameters

Table 13 Tx Operation - Possible Errors

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (V_{IN} - V_{SS})	0	8.0	V
Current into or out of V_{IN} and V_{SS} pins	0	+0.5	A
Current into or out of any other connector pin	-20	+20	mA
Maximum Input Level		+10	dBm

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{IN} - V_{SS})		5.5	8.0	V

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 38.4MHz, V_{IN} = 6.0 V, T_{AMB} = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{IN} (Regulators and reference on, CMX975 in reset)	1	–	8	–	mA
I_{IN} (CMX975 RF PLL and Internal VCO enabled)	1	–	38	–	mA
I_{IN} (IF PLL enabled)	1	–	14	–	mA
I_{IN} (CMX975 IF and RF PLLs and VCOs enabled)	1	–	42	–	mA
I_{IN} (CMX975 RF PLL with Ext.VCO module U6)	1,6	–	47	–	mA
I_{IN} (CMX975 RX LNA, Image Reject Mixer, RF PLL and VCO enabled)	1	–	74	–	mA
I_{IN} (CMX975 TX Image Reject Mixer, RF PLL and VCO enabled)	1	–	108	–	mA
RF PLL / VCO Parameters					
Frequency Range		2800	–	3600	MHz
RF output, J8	2	–	+0	–	dBm
Output Impedance		–	50	–	Ω
Phase Noise (typical) at 1600MHz, 1MHz offset	5	–	-126	–	dBc/Hz
Frequency Range (VCO Module U6)	6 7	3650 2800	–	3800 2900	MHz
Nominal RF output level, J13	2	–	-8	–	dBm
Output Impedance		–	50	–	Ω
Phase Noise (typical) at 3750MHz, 1MHz offset	6	–	-135	–	dBc/Hz
Phase Noise (typical) at 2850MHz, 1MHz offset	7	–	TBD	–	dBc/Hz
IF PLL / VCO Parameters					
Nominal Frequency		-	900	-	MHz
RF output, J10	2,3	–	-10	–	dBm
Nominal Output Impedance (unmatched)		–	8k // 0.6	–	Ω/pF
RX LNA / Image reject mixer Parameters					
Conversion Gain (J9 – J18)	8	–	15	–	dB
Noise Figure (J9 – J18)	8	-	3	-	dB
TX Image reject mixer Parameters					
Conversion Gain (J20 – J16)	9	–	5	–	dB
Reference input (Ext Clk)					
Input Impedance		–	High	–	Ω
Sensitivity	4	–	-20	–	dBm
Microcontroller Interface					
For timings see CMX975 Datasheet					

Notes:

1. PCB current consumption, not current consumption of the CML devices.
2. Without additional matching (broadband output).
3. With R49 disconnected.
4. Measured at TBD
5. Using LO output divider set to 2.
6. Mini-Circuits ROS-3877-119+ module fitted.
7. Mini-Circuits ROS-3000-619+ module fitted.
8. 1.5425GHz RF input, 225MHz IF output.
9. 225MHz IF input, 1.626GHz RF output

This is Advance Information; changes and additions may be made to this document. Parameters marked TBD or left blank will be included in later issues of this document. Information in this advance document should not be relied upon for final product design.

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