DS50PCI402 2.5 Gbps / 5.0 Gbps 4 Lane PCI Express Repeater with Equalization and De-Emphasis

Check for Samples: DS50PCI402

FEATURES

- **Input and Output signal conditioning increases PCIe reach in backplanes and cables**
- **0.09 UI of residual deterministic jitter at 5Gbps after 42" of FR4 (with Input EQ)**
- **0.11 UI of residual deterministic jitter at 5Gbps after 7m of PCIe Cable (with Input EQ)**
- **0.09 UI of residual deterministic jitter at 5Gbps with 28" of FR4 (with Output DE)**
- **0.13 UI of residual deterministic jitter at 5Gbps with 7m of PCIe Cable (with Output DE)**
- **Adjustable Transmit VOD 800 to 1200mVp-p**
- **Automatic and manual Receiver Detection and input termination control circuitry**
- **Automatic power management on an individual lane basis via SMBus**
- **Adjustable electrical idle detect threshold.**
- **Data rate optimized 3-stage equalization to 27 dB gain**
- **Data rate optimized 6-level 0 to 12 dB transmit de-emphasis**
- **Flow-thru pinout in 10mmx5.5mm 54-pin leadless WQFN package**
- **Single supply operation at 2.5V**
- **>6kV HBM ESD rating**
- **-10 to 85°C operating temperature range**

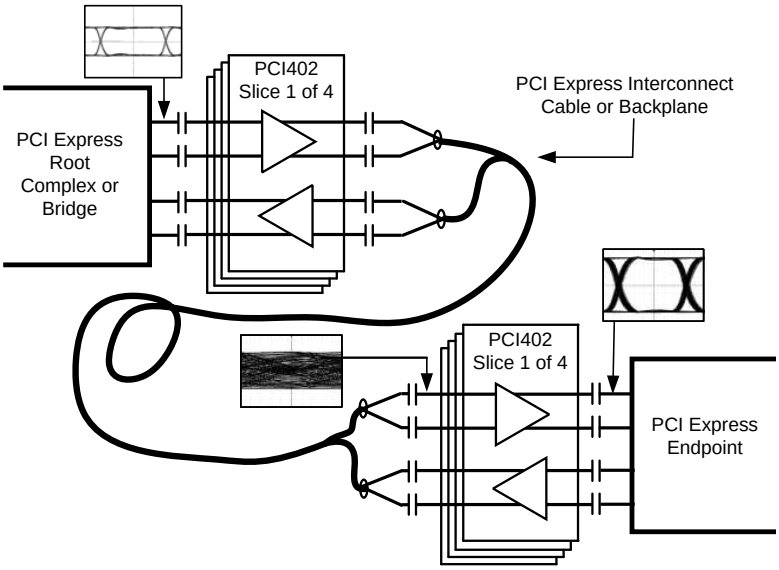
DESCRIPTION

The DS50PCI402 is a low power, 4 lane bidirectional buffer/equalizer designed specifically for PCI Express Gen1 and Gen2 applications. The device performs both receive equalization and transmit de-emphasis, allowing maximum flexibility of physical placement within a system. The receiver is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) induced by the interconnect medium.

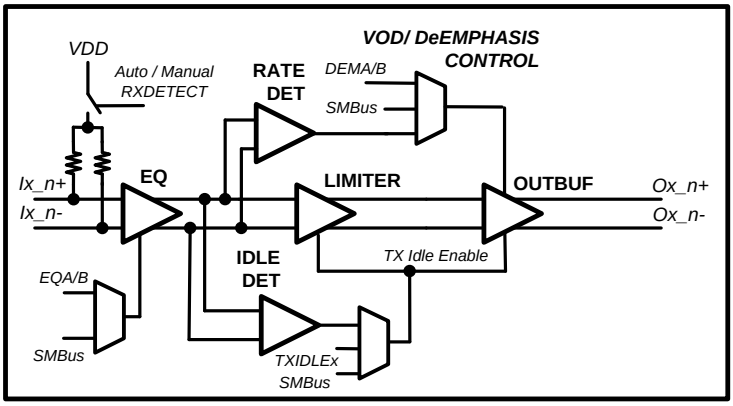
The transmitter de-emphasis level can be set by the user depending on the distance from the DS50PCI402 to the PCI Express endpoint. The DS50PCI402 contains PCI Express specific functions such as Transmit Idle, RX Detection, and Beacon signal pass through.

The device provides automatic receive detection circuitry which controls the input termination impedance. By automatically reflecting the current load impedance seen on the outputs back to the corresponding inputs the DS50PCI402 becomes completely transparent to both the PCIe root complex and endpoint. An internal rate detection circuit is included to detect if an incoming data stream is at Gen2 data rates, and adjusts the de-emphasis on it's output accordingly. The signal conditioning provided by the device allows systems to upgrade from Gen1 data rates to Gen2 without reducing their physical reach. This is true for FR4 applications such as backplanes, as well as cable interconnect.

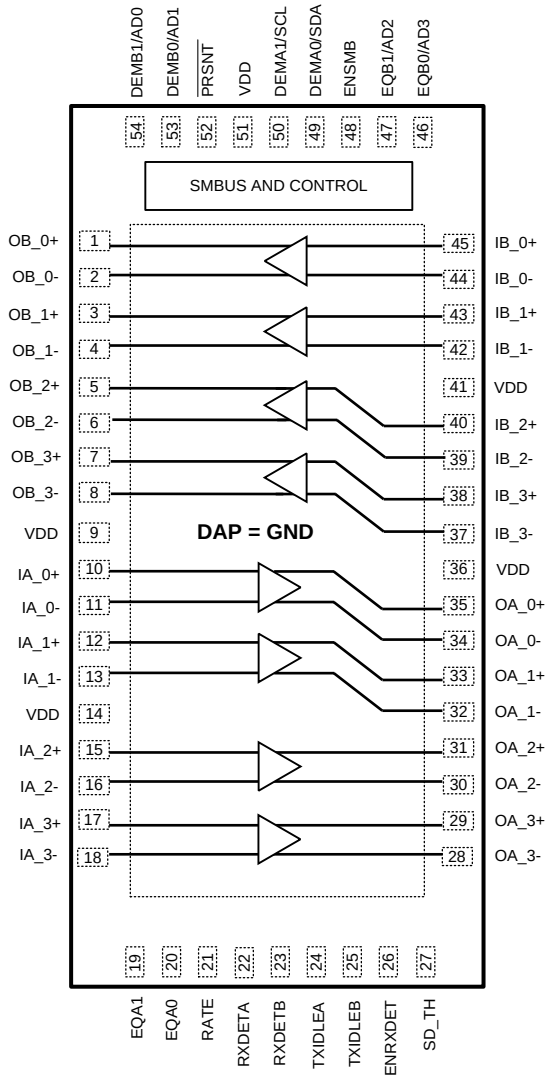
Typical Application



Block Diagram - Detail View Of Channel (1 of 8)



Pin Diagram



The center DAP on the package bottom is the device GND connection. This pad must be connected to GND through multiple (minimum of 8) vias to ensure optimal electrical and thermal performance.

DS50PCI402 Pin Diagram 54 lead

Table 1. Pin Descriptions

Pin Name	Pin Number	I/O, Type[1][2][3][4]	Pin Description
Differential High Speed I/O's			
IA_0+, IA_0- , IA_1+, IA_1-, IA_2+, IA_2-, IA_3+, IA_3-	10, 11 12, 13 15, 16 17, 18	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INA_0+ to VDD and INA_0- to VDD when enabled.
OA_0+, OA_0-, OA_1+, OA_1-, OA_2+, OA_2-, OA_3+, OA_3-	35, 34 33, 32 31, 30 29, 28	O,LPDS	Inverting and non-inverting low power differential signal (LPDS) 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs.
IB_0+, IB_0- , IB_1+, IB_1-, IB_2+, IB_2-, IB_3+, IB_3-	45, 44 43, 42 40, 39 38, 37	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INB_0+ to VDD and INB_0- to VDD when enabled.
OB_0+, OB_0-, OB_1+, OB_1-, OB_2+, OB_2-, OB_3+, OB_3-	1, 2 3, 4 5, 6 7, 8	O,LPDS	Inverting and non-inverting low power differential signal (LPDS) 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins — Shared (LVCMOS)			
ENSMB	48	I, LVCMOS w/internal pulldown	System Management Bus (SMBus) enable pin. When pulled high provide access internal digital registers that are a means of auxiliary control for such functions as equalization, de-emphasis, VOD, rate, and idle detection threshold. When pulled low, access to the SMBus registers are disabled and SMBus function pins are used to control the Equalizer and De-Emphasis. Please refer to SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS and Electrical Characteristics — Serial Management Bus Interface for detail information.
ENSMB = 1 (SMBUS MODE)			
SCL	50	I, LVCMOS	ENSMB = 1 SMBUS clock input pin is enabled. External pull-up resistor maybe needed. Refer to R_{TERM} in the SMBus specification.
SDA	49	I, LVCMOS, O, Open Drain	ENSMB = 1 The SMBus bi-directional SDA pin is enabled. Data input or open drain output. External pull-up resistor is required. Refer to R_{TERM} in the SMBus specification.
AD0-AD3	54, 53, 47, 46	I, LVCMOS w/internal pulldown	ENSMB = 1 SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. See section — SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS for additional information.
ENSMB = 0 (NORMAL PIN MODE)			
EQA0, EQA1 EQB0, EQB1	20, 19 46, 47	I,FLOAT, LVCMOS	EQA/B ,0/1 controls the level of equalization of the A/B sides as shown in Table 2. The EQA/B pins are active only when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes high the SMBus registers provide independent control of each lane, and the EQB0/B1 pins are converted to SMBUS AD2/AD3 inputs.
DEMA0, DEMA1 DEMB0, DEMB1	49, 50 53, 54	I,FLOAT, LVCMOS	DEMA/B ,0/1 controls the level of de-emphasis of the A/B sides as shown in Table 5. The DEMA/B pins are only active when ENSMB is de-asserted (Low). Each of the 4 A/B channels have the same level unless controlled by the SMBus control registers. When ENSMB goes High the SMBus registers provide independent control of each lane and the DEM pins are converted to SMBUS AD0/AD1 and SCL/SDA inputs.

(1) FLOAT = 3rd input state, don't drive pin. Pin is internally biased to mid level with 50 kΩ pull-up/pull-down. If high Z output not available, drive input to VDD/2 to assert mid level state.
(2) Internal pulldown = Internal 30 kΩ pull-down resistor to GND is present on the input.
(3) LVCMOS inputs without the “Float” conditions must be driven to a logic Low or High at all times or operation is not ensured.
(4) Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.

Table 1. Pin Descriptions (continued)

Pin Name	Pin Number	I/O, Type[1][2][3][4]	Pin Description
RATE	21	I,FLOAT, LVCMOS	RATE control pin controls the pulse width of de-emphasis of the output. A Low forces Gen1 (2.5Gbps), High forces Gen 2 (5Gbps), Open/Floating the rate is internally detected after each exit from idle and the pulse width is set appropriately. When ENSMBUS= 1 this pin is disabled and the RATE function is controlled internally by the SMBUS registers. Refer to Table 5.
Control Pins — Both Modes (LVCMOS)			
RXDETA,RXDETB	22,23	I, LVCMOS w/internal pulldown	The RXDET pins in combination with the ENRXDET pin controls the receiver detect function. Depending on the input level, a 50Ω or >50KΩ termination to the power rail is enabled. Refer to Table 7.
$\overline{\text{PRSNT}}$	52	I, LVCMOS	Cable Present Detect input. High when a cable is not present per PCIe Cabling Spec. 1.0. Puts part into low power mode. When low (normal operation) part is enabled.
ENRXDET	26	I, LVCMOS w/internal pulldown	Enables pin control of receiver detect function. The default is automatic RXDET using the internal pulldown. Pin must be pulled high for manual RXDETA/B operation. Controls individual A and B sides. Refer to Table 7.
TXIDLEA,TXIDLEB	24,25	I, FLOAT, LVCMOS	Controls the electrical idle function on corresponding outputs when enabled. H= electrical Idle, Float=autodetect (Idle on input passed to output), L=Idle squelch disabled as shown in Table 6.
Analog			
SD_TH	27	I, ANALOG	Threshold select pin for electrical idle detect threshold. Float pin for default 130mV DIFF p-p, otherwise connect resistor from SD_TH to GND to set threshold voltage as shown in Table 7.
Power			
VDD	9, 14,36, 41, 51	Power	Power supply pins CML/analog.
GND	DAP	Power	Ground pad (DAP - die attach pad).

FUNCTIONAL DESCRIPTION

The DS50PCI402 is a low power media compensation 4 lane repeater optimized for PCI Express Gen 1 and Gen 2 media including lossy FR-4 printed circuit board backplanes and balanced cables. The DS50PCI402 operates in two modes: Pin Control Mode (ENSMB = 0) and SMBus Mode (ENSMB = 1).

Pin Control Mode:

When in pin mode (ENSMB = 0) , the repeater is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically increased per the De-Emphasis table below for improved performance over lossy media. The receiver detect pins RXDETA/B provide manual control for input termination (50Ω or >50KΩ). Rate optimization is also pin controllable, with pin selections for 2.5Gbps, 5Gbps, and auto detect. The receiver electrical idle detect threshold is also programmable via an optional external resistor on the SD_TH pin.

SMBUS Mode:

When in SMBus mode the equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by sides as in the pin mode case. Upon assertion of ENSMB the RATE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low. On powerup and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 24 possible equalization settings. The tables show a typical gain for each gain stage (GST[1:0]) and boost level (BST[2:0]) combination. When using SMBus mode, the Equalization and De-Emphasis levels are set using registers.

Table 2. Equalization Settings with GST=1 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[1:0]	BST[2:0]	1.25 GHz	2.5 GHz	
F	F	00	000	0	0	Bypass - Default Setting
		01	000	1.6	3.2	
		01	001	2.1	4.2	
1	1	01	010	2.6	5.0	8" FR4 (6-mil trace) or < 1m (28 AWG) PCIe cable
		01	011	3.2	5.9	
		01	100	4.0	7.3	
		01	101	4.9	7.9	
		01	110	5.4	8.5	
		01	111	5.6	9.0	

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

Table 3. Equalization Settings with GST=2 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[1:0]	BST[2:0]	1.25 GHz	2.5 GHz	
0	0	10	000	3.8	7.6	14" FR4 (6-mil trace) or 1m (28 AWG) PCIe cable
		10	001	5.1	9.9	
F	0	10	010	6.4	11.6	20" FR4 (6-mil trace) or 5m (26 AWG) PCIe cable
		10	011	7.6	13.5	
		10	100	9.5	16.1	
F	1	10	101	11.3	17.5	40" FR4 (6-mil trace) or 9m (24 AWG) PCIe cable

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

Table 3. Equalization Settings with GST=2 for Pins or SMBus Registers (continued)

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[1:0]	BST[2:0]	1.25 GHz	2.5 GHz	
		10	110	12.3	18.6	
0	1	10	111	12.8	19.8	50" FR4 (6-mil trace) or 10m (24 AWG) PCIe cable

Table 4. Equalization Settings with GST=3 for Pins or SMBus Registers

EQ1(1)	EQ0(1)	EQ Setting		EQ Gain (dB)		Suggested Use
		GST[1:0]	BST[2:0]	1.25 GHz	2.5 GHz	
		11	000	6.4	12.2	
1	0	11	001	8.5	15.6	30" FR4 (6-mil trace) or 7m (24 AWG) PCIe cable
		11	010	10.4	18.3	
0	F	11	011	12.4	21.3	15m (24 AWG) PCIe cable
		11	100	15.2	25.0	
1	F	11	101	18.1	27.2	> 15m (24 AWG) PCIe cable
		11	110	19.6	28.8	
		11	111	20.2	30.7	

(1) F=Float (don't drive pin, each float pin has an internal 50K Ohm resistor to VDD and GND), 1=High, 0=Low

The De-Emphasis level must be set when in SMBus mode. See SMBus TRANSACTIONS section and Table 10 for specific De-Emphasis values.

Table 5. De-Emphasis Input Select Pins for A and B ports (3–Level Input)

RATE	DEM1 (1)	DEM0 (1)	Typical De-Emphasis Level	Typical DE Pulse Width	Typical VOD	Suggested Use
0/F	0	0	0dB	0ps	1000mV	
0/F	0	1	-3.5dB	400ps	1000mV	8 inches FR4 (6-mil trace) or less than 1 meter (28 AWG) PCIe cable
0/F	1	0	-6dB	400ps	1000mV	
0/F	1	1	-6dB	400ps enhanced	1000mV	15 inches FR4 (6-mil trace)
0/F	0	F	-9dB	400ps enhanced	1000mV	
0/F	1	F	-12dB	400ps enhanced	1000mV	
0/F	F	0	-9dB	400ps enhanced	1200mV	30 inches FR4 (6-mil trace)
0/F	F	1	-12dB	400ps enhanced	1400mV	40 inches FR4 (6-mil trace)
0/F	F	F	Reserved, don't use			
1/F	0	0	0dB	0ps	1000mV	
1/F	0	1	-3.5dB	200ps	1000mV	
1/F	1	0	-6dB	200ps	1000mV	
1/F	1	1	-6dB	200ps enhanced	1000mV	10 inches FR4 (6-mil trace)
1/F	0	F	-9dB	200ps enhanced	1000mV	
1/F	1	F	-12dB	200ps enhanced	1000mV	
1/F	F	0	-9dB	200ps enhanced	1200mV	20 inches FR4 (6-mil trace)
1/F	F	1	-12dB	200ps enhanced	1400mV	30 inches FR4 (6-mil trace)
1/F	F	F	Reserved, don't use			

(1) F=Float (don't drive pin - (each float pin has an internal 50K Ohm resistor to VDD and GND). Enhanced DE Pulse width provides additional de-emphasis on second bit. VOD = Voltage Output Differential amplitude. When RATE is floated (F=Auto Rate Detection Active) DE Level and Pulse Width settings follow detected RATE. RATE=0 is 2.5GBps, RATE=1 is 5 GBps

Table 6. Idle Control (3–Level Input)

TXIDLEA/B	Function
0	This state is for lossy media, dedicated Idle threshold detect circuit disabled, output follows input based on EQ settings. Idle state not ensured.
Float	Float enables automatic idle detection. Idle on the input is passed to the output. This is the recommended default state. Output driven to Idle if diff input signal less than value set by SD_TH pin.
1	Manual override, output forced to Idle. Diff inputs are ignored.

Table 7. Receiver Electrical Idle Detect Threshold Adjust (Analog input - Connect Resistor to GND or Float)

SD_TH resistor value (Ω) (connect from pin to GND)(1)	Typical Receiver Electrical Idle Detect Threshold (DIFF p-p)
Float (no resistor required)	130mV (default condition)
0	225mV
80K	20mV

(1) SD_TH resistor value can be set from 0 through 80K Ohms to achieve desired idle detect threshold, see Figure 1. 8K Ohm is approx 130mV.

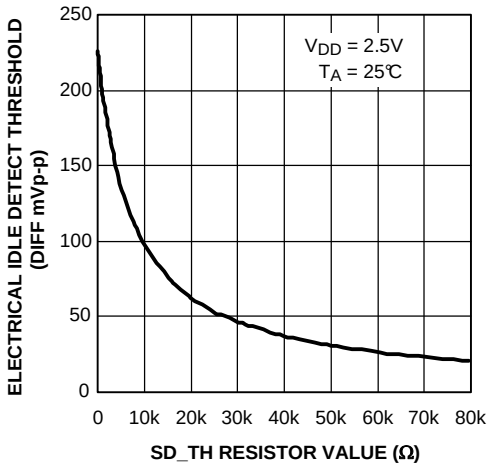


Figure 1. Typical Idle threshold vs SD_TH resistor value

Receiver Detection

The Rx detection process is a feature that can set the number of active channels on the DS50PCI402. By sensing the presence of a valid PCIe load on the output, the channel can be automatically enabled for operation. This allows the DS50PCI402 to configure inself to the proper lane width, whether it is a 4-lane, 2-lane, or 1-lane PCIe link.

Automatic Rx Detection is enabled by a combination of PRSNT# and ENRXDET inputs. When these inputs are set low, Automatic Rx Detection is enabled, cycling of the PRSNT# pin will reset the Rx detection circuitry, initiating a new receiver detection sequence. Pulling the ENRXDET input to logic 1, allows for manual control of the input termination.

The table below summarizes control pin and receiver detect operation for the DS50PCI402.

Table 8. Receiver Detect Pins for A and B ports (LVCMOS inputs)

PRSNT#	ENRXDET	RXDETA/B	Input Termination	Termination sensed on Output	Function
0	0	0	>50KΩ to VDD	Hi - Z	Automatic RXDET: Rx detection state machine enabled. Outputs will test for the presence of a receiver input every 12 msec until detection occurs. Input termination remains >50KΩ to VDD until receiver is detected. Once receiver is detected, input impedance to VDD is 50Ω.
			50Ω	PCIe Input	
0	0	1	>50KΩ to VDD	Hi - Z	Automatic RXDET: Rx detection state machine enabled. Outputs will test for the presence of a receiver input every 12 msec for 600 msec and then stop. Input termination remains >50KΩ to VDD until receiver is detected. Once receiver is detected, input impedance to VDD is 50Ω. Restart detection if RXDETA/B is pulsed low-high.
			50Ω	PCIe Input	
0	1	0	>50KΩ to VDD	X	Manual RXDET: Rx detection state machine disabled. Input termination >50KΩ. Associated output channels in low power idle mode.
0	1	1	50Ω	X	Manual RXDET: Rx detection state machine disabled. Input termination 50Ω. Associated output channels set to active.
1	X	X	>50KΩ to VDD	X	Power down mode: Input termination >50KΩ. Associated output channels off. Part in power saving mode. PRSNT# should be held high for a minimum of 5 us to ensure complete analog power down. The Automatic RXDET functionality will be re-initialized on the falling edge of PRSNT#.

RX Detect: Range of Operation

The Rx detection process used in the DS50PCI402 is designed to be fully compliant with the PCIe 2.0 base specification. The receiver detection circuitry will accurately detect a receiver when both conditions listed below are true:

- DS50PCI402 within Recommended Operating Range for Temperature and Supply Voltage
- For receiver $Z_{RX\text{-}DC}$ = 40 (min) to 60 (max) Ohms

Note: To ensure robust system operation, the DS50PCI402 will only signal a valid receiver detection if both halves of the differential output pair detect a proper 40 - 60 Ohm receiver impedance. If the receiver detection circuitry senses a load impedance greater than $Z_{RX\text{-}DC}$ on either trace of a differential pair, it will be interpreted as no termination load present (i.e. the corresponding DS50PCI402 input termination will remain High-Z).

Manual Control Of RXDETA/B In A PCIe Environment

In some cases manual control of RXDETA/B may be desirable. In order for upstream and downstream PCIe subsystems to communicate in a cabling environment, the PCIe specification includes several auxiliary or sideband signals to manage system-level functionality or implementation. Similar methods are used in backplane applications, but the exact implementation falls outside the PCIe standard. Initial communication from the downstream subsystem to the upstream subsystem is done with the CPRSNT# auxiliary signal. The CPRSNT# signal is asserted Low by the downstream componentry after the "Power Good" condition has been established. This mechanism allows for the upstream subsystem to determine whether the power is good within the downstream subsystem, enable the reference clock, and initiate the Link Training Sequence.

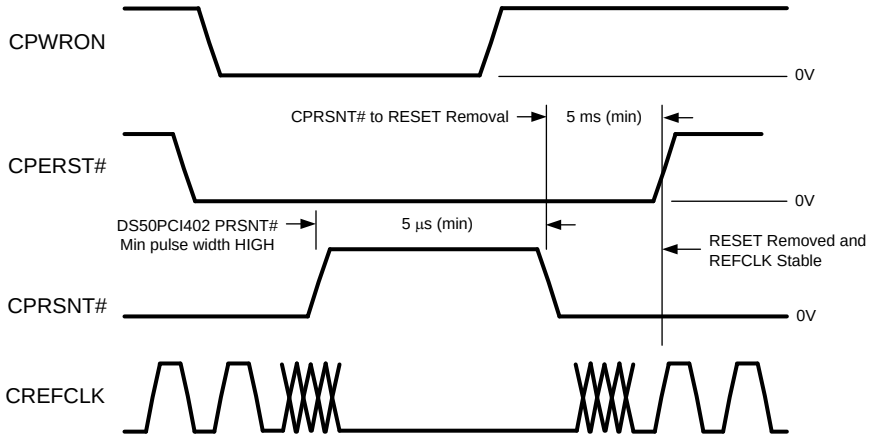


Figure 2. Typical PCIe System Timing

The signals shown in the graphic could be easily replicated within the downstream subsystem and used to externally control the common mode input termination impedance on the DS50PCI402. Often an onboard microcontroller will be used to handle events like power-up, power-down, power saving modes, and hot insertion. The microcontroller would use the same information to determine when to enable and disable the DS50PCI402 input termination. In applications that require SMBus control, the microcontroller could also delay any response to the upstream subsystem to allow sufficient time to correctly program the DS50PCI402 and other devices on the board.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (VDD)	-0.5V to +3.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5V)
CML Input Current	-30 to +30 mA
LPDS Output Voltage	-0.5V to (VDD+0.5V)
Analog (SD_TH) (3)	-0.5V to (VDD+0.5V)
Junction Temperature	+125°C
Storage Temperature	-40°C to +125°C
Lead Temperature Range	
Maximum Package Power Dissipation at 25°C	
NJY Package	4.21 W
Derate NJY Package	52.6mW/°C above +25°C
ESD Rating	
HBM, STD - JESD22-A114C	≥6 kV
MM, STD - JESD22-A115-A	≥250 V
CDM, STD - JESD22-C101-C	≥1250 V
Thermal Resistance	
θ_{JC}	11.5°C/W
θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W
For soldering specifications: see product folder at www.ti.com http://www.ti.com/lit/SNOA549	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are specified for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

(3) Measured at default SD_TH settings

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to GND	2.375	2.5	2.625	V
Ambient Temperature	-10	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise Tolerance up to 50Mhz (1)			100	mV pp

(1) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified. (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER (3)						
PD	Power Dissipation	EQX=Float, DEX=0, VOD=1Vpp ,$\overline{\text{PRSNT}}$=0		800	1000	mW
		$\overline{\text{PRSNT}}$=1, ENSMB=0		4	8	mW
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	(4)	2		3.6	V
V_{IL}	Low Level Input Voltage	(4)	0		0.8	V
V_{OH}	High Level Output Voltage	SMBUS open drain V_{OH} set by pullup Resistor				V
V_{OL}	Low Level Output Voltage	I_{OL} = 4mA			0.4	V
I_{IH}	Input High Current	V_{IN} = 3.6V , LVCMOS	-15		+15	µA
		V_{IN} = 3.6V , w/ FLOAT,PULLDOWN input	-15		+120	
I_{IL}	Input Low Current	V_{IN} = 0V	-15		+15	µA
		V_{IN} = 0V, w/FLOAT input	-80		+15	
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$RL_{RX-DIFF}$	Rx package plus Si differential return loss	0.05GHz – 1.25GHz (5)		-21		dB
		1.25GHz – 2.5GHz (5)		-20		
RL_{RX-CM}	Common mode Rx return loss	0.05GHz - 2.5GHz (5)		-11.5		dB
Z_{RX-DC}	Rx DC common mode impedance	Tested at VDD=0	40	50	60	Ω
$Z_{RX-DIFF-DC}$	Rx DC differential impedance	Tested at VDD=0	85	100	115	Ω
$V_{RX-DIFF-DC}$	Differential Rx peak to peak voltage	Tested at DC, TXIDLEx=0	0.10		1.2	V
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM impedance for V>0	Vin = 0 to 200 mV, RXDETA/B = 0, ENSMB = 0, VDD=2.625	50			KΩ
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle detect threshold	SD_TH = float, see Table 5, (6)	40		175	mV_{P-P}
LPDS OUTPUTS (OUT_n+, OUT_n-)						
$V_{TX-DIFF-PP}$	Output Voltage Swing	Differential measurement with OUT_n+ and OUT_n- terminated by 50Ω to GND AC-Coupled, Figure 4, (3)	800	1000	1200	mV_{P-P}
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, (1)		V_{DD} - 1.4		V

(1) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Measured with DEM Select pins configured for 1000mV VOD, see De-emphasis table.
(4) Input edge rate for LVCMOS/FLOAT inputs must be 50ns minimum from 10-90%.
(5) Input Return Loss also uses the setup shown in Figure 6. The blocking / biasing circuit is replaced with a simple AC coupling capacitor for each input to emulate a typical PCIe application.
(6) Measured at package pins of receiver. Less than 40mV is IDLE, greater than 175mV is ACTIVE. SD_TH pin connected with resistor to GND overrides this default setting.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.
(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{TX-DE-RATIO-3.5}$	Tx de-emphasis level ratio	VOD = 1000 mV, DEM1 = GND, DEM0 = VDD, (1), (7)		3.5		dB
$V_{TX-DE-RATIO-6}$	Tx de-emphasis level ratio	VOD = 1000 mV, DEM1 = VDD, DEM0 = GND, (1), (7)		6		dB
$T_{TX-HF-DJ-DD}$	Tx Dj > 1.5 Mhz	(8)			0.15	UI
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5Mhz	(8)			3.0	ps RMS
$T_{TX-RISE-FALL}$	Transmitter Rise/ Fall Time	20% to 80% of differential output voltage, Figure 3 (1) (9)	50	67		ps
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	20% to 80% of differential output voltage (1) (9)		0.01	0.1	UI
$RL_{TX-DIFF}$	Differential Output Return Loss	0.05- 1.25 Ghz, See Figure 6		-23		dB
		1.25- 2.5 Ghz, See Figure 6		-20		dB
RL_{TX-CM}	Common Mode Return Loss	0.05- 2.5 Ghz, See Figure 6		-11		dB
$Z_{TX-DIFF-DC}$	DC differential Tx impedance			100		Ω
$V_{TX-CM-AC-PP}$	Tx AC common mode voltage				100	mVpp
$I_{TX-SHORT}$	transmitter short circuit current limit	Total current transmitter can supply when shorted to VDD or GND			90	mA
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and electrical Idle				40	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between Tx+ and Tx-				25	mV
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to transition to valid diff signaling after leaving Electrical Idle	VIN = 800 mVp-p, 5 Gbps, Figure 5		6.5	9.5	nS
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to transition to valid diff signaling after leaving Electrical Idle	VIN = 800 mVp-p, 5 Gbps, Figure 5		5.5	8	nS
T_{PDEQ}	Differential Propagation Delay	EQ = 11, +4.0 dB @ 2.5 GHz , Figure 4 (10)	150	200	250	ps
T_{PD}	Differential Propagation Delay	EQ = FF, Equalizer Bypass, Figure 4 (10) (11)	120	170	220	ps
T_{LSK}	Lane to Lane Skew in a Single Part	T_A = 25C,V_{DD} = 2.5V (12) (11)			27	ps

(7) Measured with a repeating K28.5 pattern at a data rate of 2.5 Gbps and 5.0 Gbps.
(8) PCIe 2.0 transmit jitter specifications - actual device jitter is much less. Actual device Rj and Dj has been characterized and specified with test loads outlined in the EQUALIZATION and DE-EMPHASIS sections of the Electrical Characteristics table.
(9) Specified by device characterization
(10) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ Bypass will result in the shortest propagation delays.
(11) Propagation Delay measurements for Part to Part skew are all based on devices operating under indentical temperature and supply voltage conditions.
(12) Specified by device characterization

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.
(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{PPSK}	Part to Part Propagation Delay Skew	T_A = 25C,V_{DD} = 2.5V			35	ps
EQUALIZATION						
DJE1	Residual Deterministic Jitter at 5 Gbps	42” of 5 mil stripline FR4, EQ1,0=F,1; K28.5 pattern, DEMx=0, Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (13) (14)		0.02	0.09	UI_{P-P}
DJE2	Residual Deterministic Jitter at 2.5 Gbps	42” of 5 mil stripline FR4, EQ1,0=F,1; K28.5 pattern, DEMx=0, Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (13) (14)		0.02	0.04	UI_{P-P}
DJE3	Residual Deterministic Jitter at 5 Gbps	7 meters of 24 AWG PCIe cable, EQ1,0=1,0; K28.5 pattern, DEMx=0, Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (13) (14)		0.02	0.11	UI_{P-P}
DJE4	Residual Deterministic Jitter at 2.5 Gbps	7 meters of 24 AWG PCIe cable, EQ1,0=1,0; K28.5 pattern, DEMx=0, Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (13) (14)		0.03	0.07	UI_{P-P}
RJ	Random Jitter	Tx Launch Amplitude 1.0 Vp-p, SD_TH=F, Repeating 1100b (D24.3) pattern. (13)		<0.5		psrms
DE-EMPHASIS						
DJD1	Residual Deterministic Jitter at 5 Gbps	28” of 5 mil stripline FR4, EQ1,0=F,F; K28.5 pattern, DEM1,0=F,1; Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (13) (14)		0.02	0.09	UI_{P-P}
DJD2	Residual Deterministic Jitter at 2.5 Gbps	28” of 5 mil microstrip FR4, EQ1,0=F,F; K28.5 pattern, DEM1,0=F,0; Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (15) (16)		0.03	0.05	UI_{P-P}
DJD3	Residual Deterministic Jitter at 5 Gbps	7 meters of 24 AWG PCIe cable, EQ1,0=F,F; K28.5 pattern, DEM1,0=F,1; Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (15) (16)		0.03	0.13	UI_{P-P}
DJD4	Residual Deterministic Jitter at 2.5 Gbps	7 meters of 24 AWG PCIe cable, EQ1,0=F,F; K28.5 pattern, DEM1,0=F,0; Tx Launch Amplitude 1.0 Vp-p, SD_TH=F. (15) (16)		0.04	0.06	UI_{P-P}

(13) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(14) Residual DJ measurements subtract out deterministic jitter present at the generator outputs. For 2.5 Gbps generator Dj = 0.0275 UI and for 5.0 Gbps generator Dj = 0.035 UI.
(15) Typical values represent most likely parametric norms at V_{DD} = 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(16) Residual DJ measurements subtract out deterministic jitter present at the generator outputs. For 2.5 Gbps generator Dj = 0.0275 UI and for 5.0 Gbps generator Dj = 0.035 UI.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V

Electrical Characteristics — Serial Management Bus Interface (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, (1) (2) (3)		2000		Ω
		Pullup V_{DD} = 2.5V, (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS. See Figure 7						
FSMB	Bus Operating Frequency	(4)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	(5)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	(5)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	(5)			2	ms
t_F	Clock/Data Fall Time	(5)			300	ns
t_R	Clock/Data Rise Time	(5)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	(5)			500	ms

(1) Recommended value. Parameter not tested in production.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

TIMING DIAGRAMS

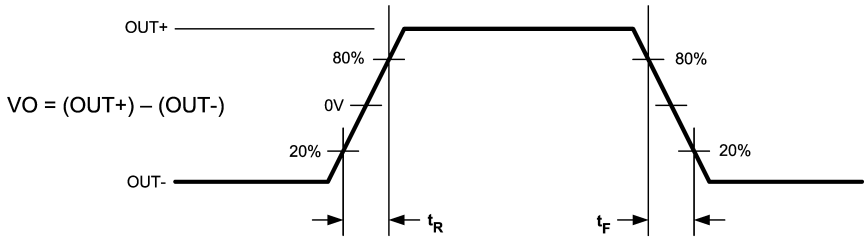


Figure 3. CML Output Transition Times

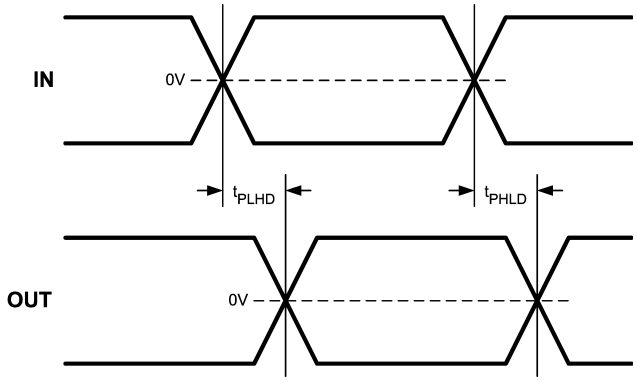


Figure 4. Propagation Delay Timing Diagram

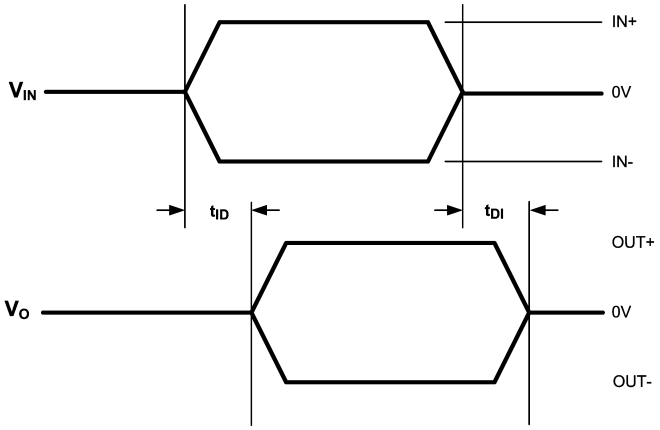


Figure 5. Idle Timing Diagram

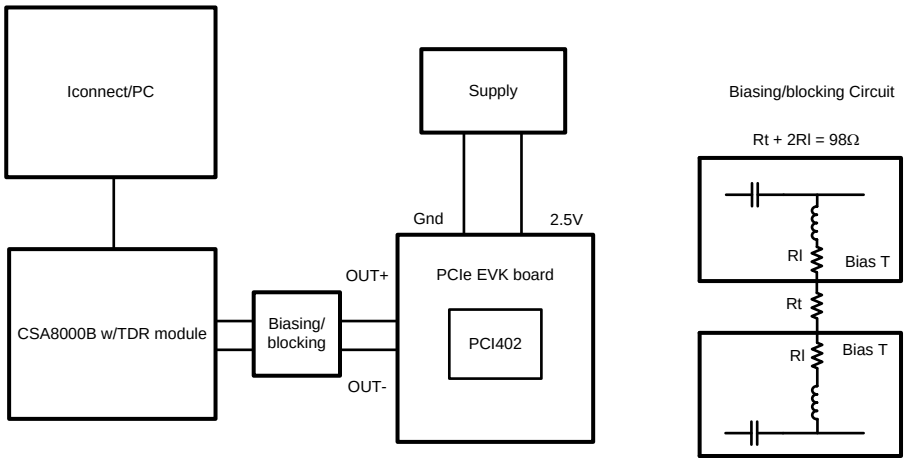


Figure 6. Input and Output Return Loss Setup

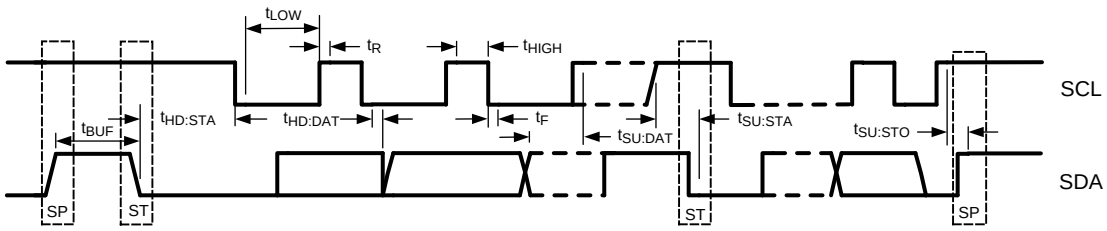


Figure 7. SMBus Timing Parameters

SYSTEM MANAGEMENT BUS (SMBUS) AND CONFIGURATION REGISTERS

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS50PCI402 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBus slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is A0'h. Based on the SMBus 2.0 specification, the DS50PCI402 has a 7-bit slave address of 1010000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 0000'b or A0'h. The device address byte can be set with the use of the AD[3:0] inputs. Below are some examples.

AD[3:0] = 0001'b, the device address byte is A2'h

AD[3:0] = 0010'b, the device address byte is A4'h

AD[3:0] = 0100'b, the device address byte is A8'h

AD[3:0] = 1000'b, the device address byte is B0'h

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

When SMBus is enabled, the DS50PCI402 **must use one of the following De-emphasis settings** (Table 9). The driver de-emphasis value is set on a per channel basis using 8 different registers. Each register (0x11, 0x18, 0x1F, 0x26, 0x2E, 0x35, 0x3C, 0x43) requires one of the following De-emphasis settings when in SMBus mode. See Table 5 for suggested DE settings at 2.5 and 5.0 Gbps operation.

Table 9. De-Emphasis Register Settings (must write one of the following when in SMBus mode)

De-Emphasis Value	Register Setting
0.0 dB	0x01
-3.5 dB	0xE8
-6 dB	0x88
-9 dB	0x90

Table 9. De-Emphasis Register Settings (must write one of the following when in SMBus mode) (continued)

De-Emphasis Value	Register Setting
-12 dB	0xA0

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see SMBus Register Map Table for more information.

SMBus REGISTER WRITES:

The DS50PCI402 outputs will NOT be PCIe compliant with the SMBus registers enabled (ENSMB = 1) until the VOD levels have been set. Below is an example to configure the VOD level to a PCIe compliant amplitude and adjust the DE and EQ signal conditioning to work with a 7m PCIe cable interconnect on the input B-side / output A-side of the device

1. Reset the SMBus registers to default values:
   - **Write 01'h to address 0x00.**
2. Set VOD = 1.0V for all channels (OA[3:0] and OB[3:0]):
   - **Write 0F'h to address 0x10, 0x17, 0x1E, 0x25, 0x2D, 0x34, 0x3B, 0x42.**
3. Set equalization to external pin level EQ[1:0] = 10 (~15.5 dB at 2.5 GHz) for all channels (IB[3:0]):
   - **Write 39'h to address 0x0F, 0x16, 0x1D, 0x24.**
4. Set de-emphasis to DE[1:0] = F1 or -12 dB enhanced for all A channels (OA[3:0]):
   - **Write A0'h to address 0x2E, 0x35, 0x3C, 0x43.**

IDLE AND RATE DETECTION TO EXTERNAL PINS

The functions of IDLE and RATE detection to external pins for monitoring can be supported in SMBus mode. The external GPIO pins of 19, 20, 46 and 47 will be changed and they will serve as outputs for IDLE and RATE detect signals.

The following external pins should be set to auto detection:

RATE = F (FLOAT) – auto RATE detect enabled

TXIDLEA/B = F (FLOAT) – auto IDLE detect enabled

There are 4 GPIO pins that can be configured as outputs with reg_4E[0].

To disable the external SMBus address pins, so pin 46 and 47 can be used as outputs:

Write 01'h to address 0x4E.

Care must be taken to ensure that only the desired status block is enabled and attached to the external pin as the status blocks can be OR'ed together internally. Register bits reg_47[5:4] and bits reg_4C[7:6] are used to enable each of the status block outputs to the external pins. The channel status blocks can be internally OR'ed together to monitor more than one channel at a time. This allows more information to be presented on the status outputs and later if desired, a diagnosis of the channel identity can be made with additional SMBus writes to register bits reg_47[5:4] and bits reg_4C[7:6].

Below are examples to configure the device and bring the internal IDLE and RATE status to pins 19, 20, 46, 47.

To monitor the IDLE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

Write 32'h to address 0x47.

The following IDLE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means IDLE is detected (no signal present).

Pin = LOW (GND) means ACTIVE (data signal present).

To monitor the RATE detect with two channels ORed (CH0 with CH2, CH1 with CH3, CH4 with CH6, CH5 with CH7):

Write C0'h to address 0x4C.

The following RATE status should be observable on the external pins:

pin 19 – CH0 with CH2,

pin 20 – CH1 with CH3,

pin 46 – CH4 with CH6,

pin 47 – CH5 with CH7.

Pin = HIGH (VDD) means high data rate is detected (6 Gbps).

Pin = LOW (GND) means low rate is detected (3 Gbps).

Table 10. SMBus Register Map

Address	Register Name	Bit (s)	Field	Type	Default	Description

Table 10. SMBus Register Map (continued)

0x00	Reset	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Reset			SMBus Reset 1: Reset registers to default value
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CHA_3 [6]: CHA_2 [5]: CHA_1 [4]: CHA_0 [3]: CHB_3 [2]: CHB_2 [1]: CHB_1 [0]: CHB_0 00'h = all channels enabled FF'h = all channels disabled
0x02	PWDN Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override PWDN			0: Allow PWDN pin control 1: Block PWDN pin control
0x08	Pin Control Override	7:5	Reserved	R/W	0x00	Set bits to 0.
		4	Override IDLE			0: Allow IDLE pin control 1: Block IDLE pin control
		3	Reserved			Set bit to 0.
		2	Override RATE			0: Allow RATE pin control 1: Block RATE pin control
		1:0	Reserved			Set bits to 0.
0x0E	CH0 - CHB0 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x0F	CH0 - CHB0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH0 IB0 EQ			IB0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x10	CH0 - CHB0 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH0 OB0 VOD			OB0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x11	CH0 - CHB0 DE Control	7:0	CH0 OB0 DEM	R/W	0x03	OB0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x12	CH0 - CHB0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x15	CH1 - CHB1 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x16	CH1 - CHB1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH1 IB1 EQ			IB1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x17	CH1 - CHB1 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH1 OB1 VOD			OB1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x18	CH1 - CHB1 DE Control	7:0	CH1 OB1 DEM	R/W	0x03	OB1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x19	CH1 - CHB1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x1C	CH2 - CHB2 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x1D	CH2 - CHB2 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH2 IB2 EQ			IB2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x1E	CH2 - CHB2 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH2 OB2 VOD			OB2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x1F	CH2 - CHB2 DE Control	7:0	CH2 OB2 DEM	R/W	0x03	OB2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x20	CH2 - CHB2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x23	CH3 - CHB3 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x24	CH3 - CHB3 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH3 IB3 EQ			IB3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x25	CH3 - CHB3 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH3 OB3 VOD			OB3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x26	CH3 - CHB3 DE Control	7:0	CH3 OB3 DEM	R/W	0x03	OB3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x27	CH3 - CHB3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x2B	CH4 - CHA0 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x2C	CH4 - CHA0 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH4 IA0 EQ			IA0 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x2D	CH4 - CHA0 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH4 OA0 VOD			OA0 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x2E	CH4 - CHA0 DE Control	7:0	CH4 OA0 DEM	R/W	0x03	OA0 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x2F	CH4 - CHA0 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x32	CH5 - CHA1 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x33	CH5 - CHA1 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH5 IA1 EQ			IA1 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x34	CH5 - CHA1 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH5 OA1 VOD			OA1 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x35	CH5 - CHA1 DE Control	7:0	CH5 OA1 DEM	R/W	0x03	OA1 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x36	CH5 - CHA1 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x39	CH6 - CHA2 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x3A	CH6 - CHA2 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH6 IA2 EQ			IA2 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ1 EQ0] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x3B	CH6 - CHA2 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH6 OA2 VOD			OA2 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x3C	CH6 - CHA2 DE Control	7:0	CH6 OA2 DEM	R/W	0x03	OA2 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x3D	CH6 - CHA2 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x40	CH7 - CHA3 IDLE RATE Select	7:6	Reserved	R/W	0x00	Set bits to 0.
		5	IDLE auto			0: Allow IDLE_sel control in Bit 4 1: Automatic IDLE detect
		4	IDLE select			0: Output is ON (SD is disabled) 1: Output is muted (electrical idle)
		3:2	Reserved			Set bits to 0.
		1	RATE auto			0: Allow RATE_sel control in Bit 0 1: Automatic RATE detect
		0	RATE select			0: 2.5 Gbps 1: 5.0 Gbps
0x41	CH7 - CHA3 EQ Control	7:6	Reserved	R/W	0x20	Set bits to 0.
		5:0	CH7 IA3 EQ			IA3 EQ Control - total of 24 levels (3 gain stages with 8 settings) [5]: Enable EQ [4:3]: Gain Stage Control [2:0]: Boost Level Control Pin [EQ0 EQ1] = Register [EN] [GST] [BST] = Hex Value FF = 100000 = 20'h = Bypass (Default) 11 = 101010 = 2A'h 00 = 110000 = 30'h F0 = 110010 = 32'h 10 = 111001 = 39'h F1 = 110101 = 35'h 01 = 110111 = 37'h 0F = 111011 = 3B'h 1F = 111101 = 3D'h
0x42	CH7 - CHA3 VOD Control	7	Reserved	R/W	0x03	Set bit to 0.
		5:0	CH7 OA3 VOD			OA3 VOD Control 03'h = 600 mV (Default) 07'h = 800 mV 0F'h = 1000 mV 1F'h = 1200 mV

Table 10. SMBus Register Map (continued)

0x43	CH7 - CHA3 DE Control	7:0	CH7 OA3 DEM	R/W	0x03	OA3 DEM Control [7]: DEM TYPE (Compatibility = 0 / Enhanced = 1) [6:0]: DEM Level Control Pin [DEM1 DEM0] = Register [TYPE] [Level Control] = Hex Value 00 = 00000001 = 01'h = 0.0 dB 01 = 11101000 = E8'h = −3.5 dB 11 = 10001000 = 88'h = −6.0 dB 0F = 10010000 = 90'h = −9.0 dB 1F = 10100000 = A0'h = −12.0 dB F0 = 10010000 = 90'h = −9.0 dB F1 = 10100000 = A0'h = −12.0 dB FF = 11000000 = C0'h = Reserved
0x44	CH7 - CHA3 IDLE Threshold	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:0	IDLE threshold			De-assert = [3:2], assert = [1:0] 00 = 110 mV, 70 mV (Default) 01 = 150 mV, 110 mV 10 = 170 mV, 130 mV 11 = 190 mV, 150 mV
0x47	Global VOD Adjust	7:2	Reserved	R/W	0x02	Set bits to 0.
		1:0	VOD Adjust			00 = -25.0% 01 = -12.5% 10 = +0.0% (Default) 11 = +12.5%

APPLICATION INFORMATION

GENERAL RECOMMENDATIONS

The DS50PCI402 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and the latest version of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 (SNOA401) for additional information on WQFN packages.

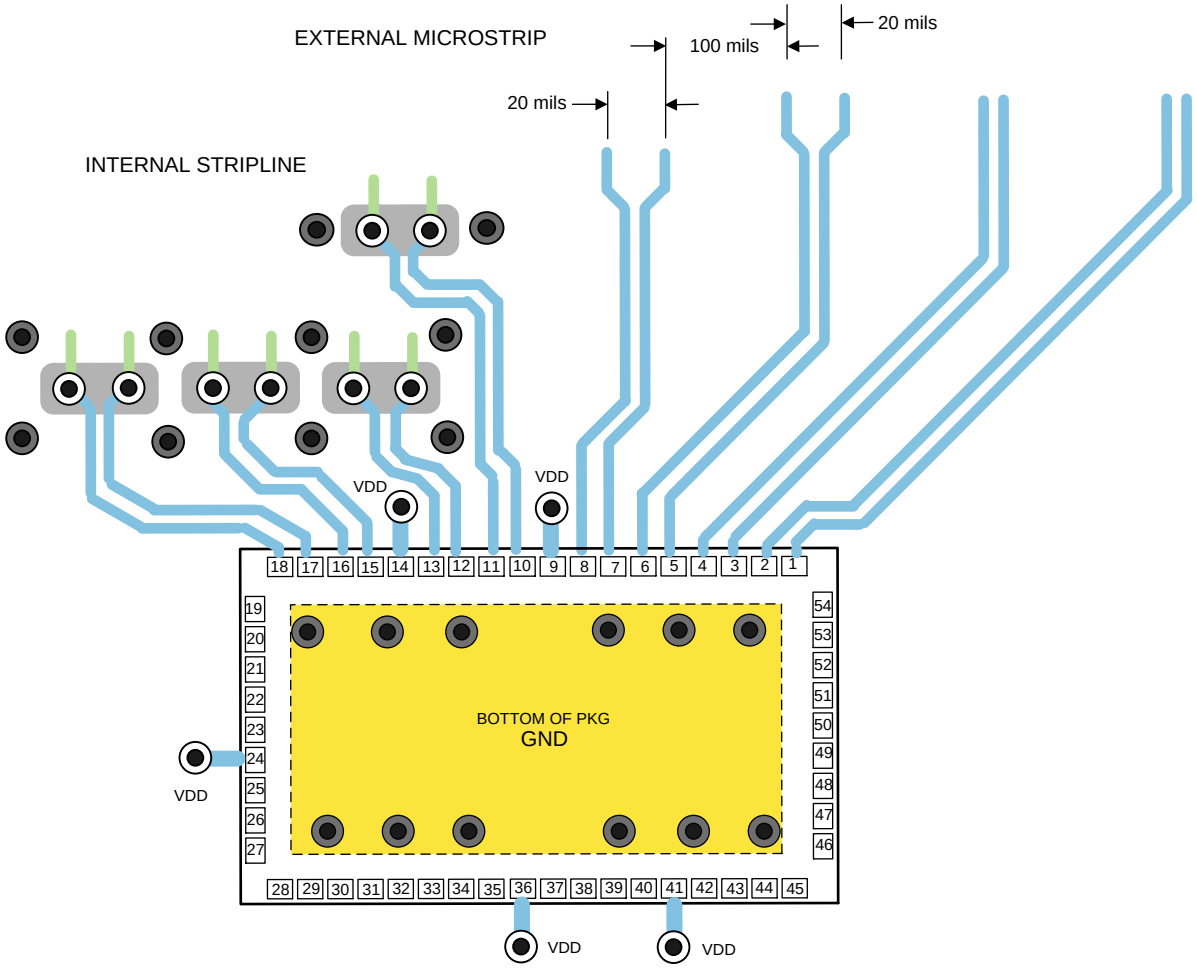


Figure 8. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the deterimential high frequency effects of stubs on the signal path.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS50PCI402 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS50PCI402. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Typical Performance Eye Diagrams and Curves

DS50PCI402 Return Loss

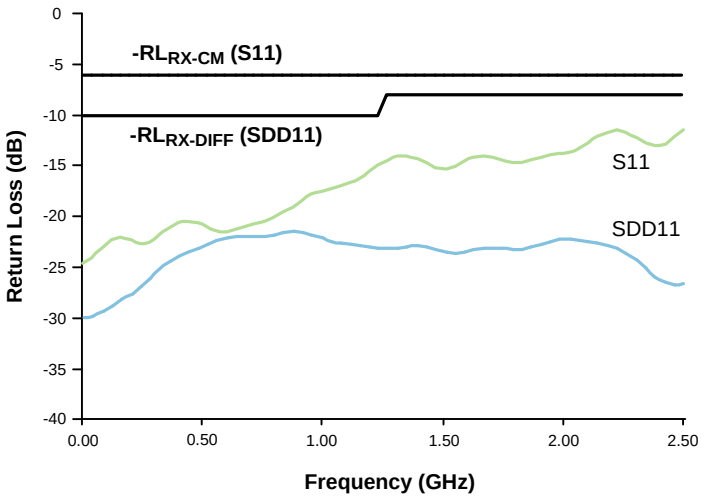


Figure 9. Receiver Return Loss Mask for 5.0 Gbps

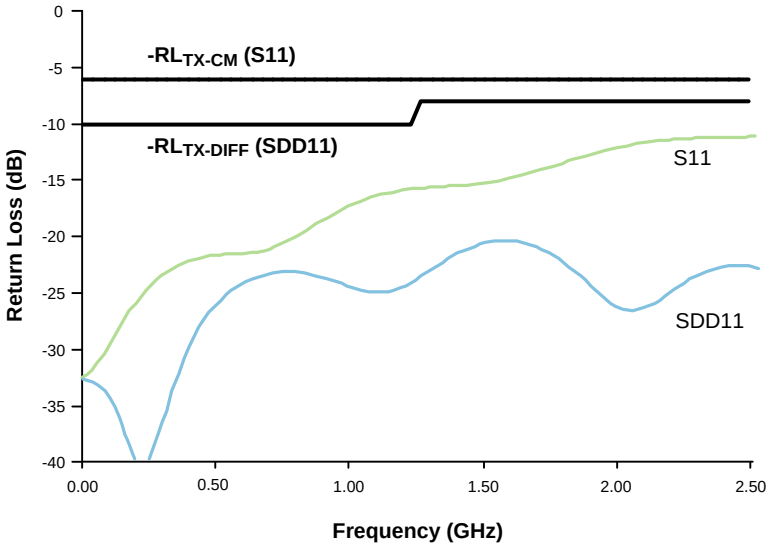


Figure 10. Transmitter Return Loss Mask for 5.0 Gbps

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	30

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS50PCI402SQ/NOPB	ACTIVE	WQFN	NJY	54	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 85	DS50PCI402SQ	Samples
DS50PCI402SQE/NOPB	ACTIVE	WQFN	NJY	54	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 85	DS50PCI402SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

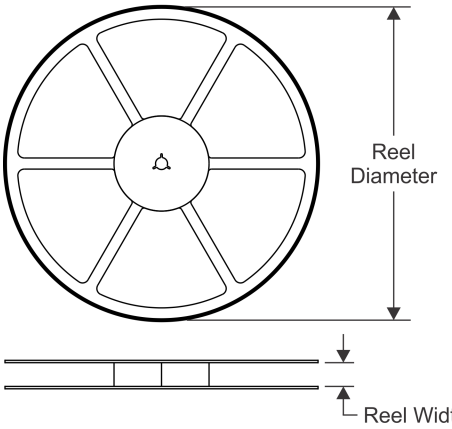
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

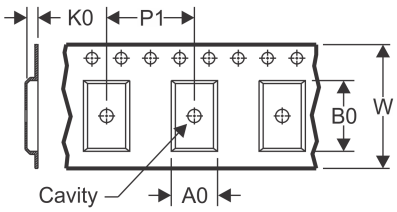
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

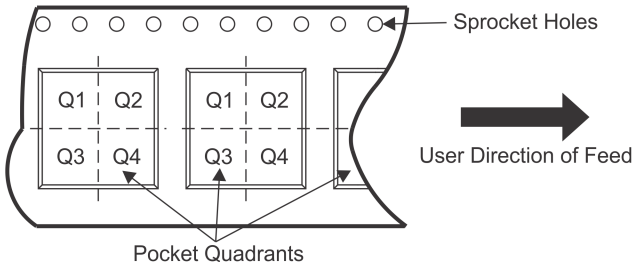


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

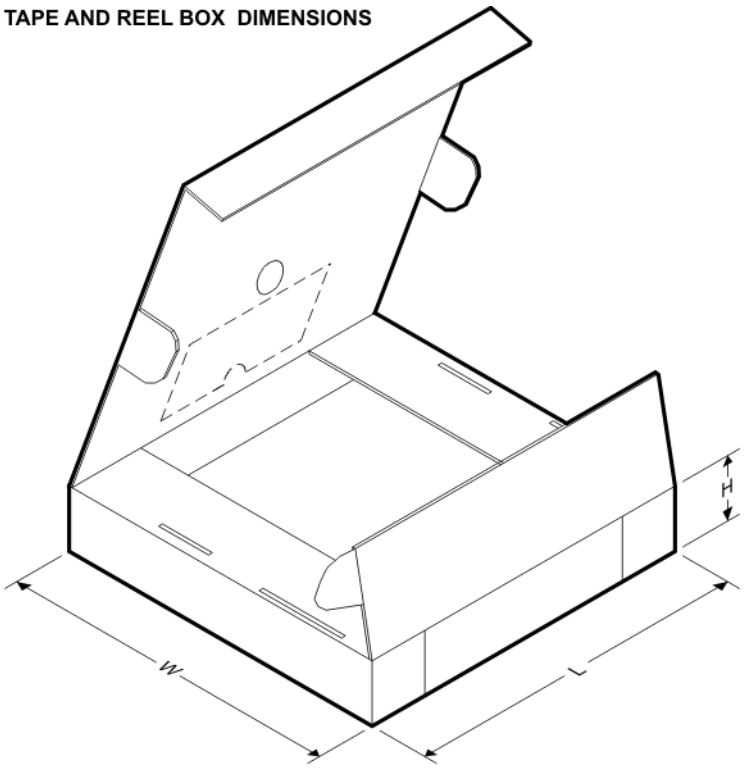
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

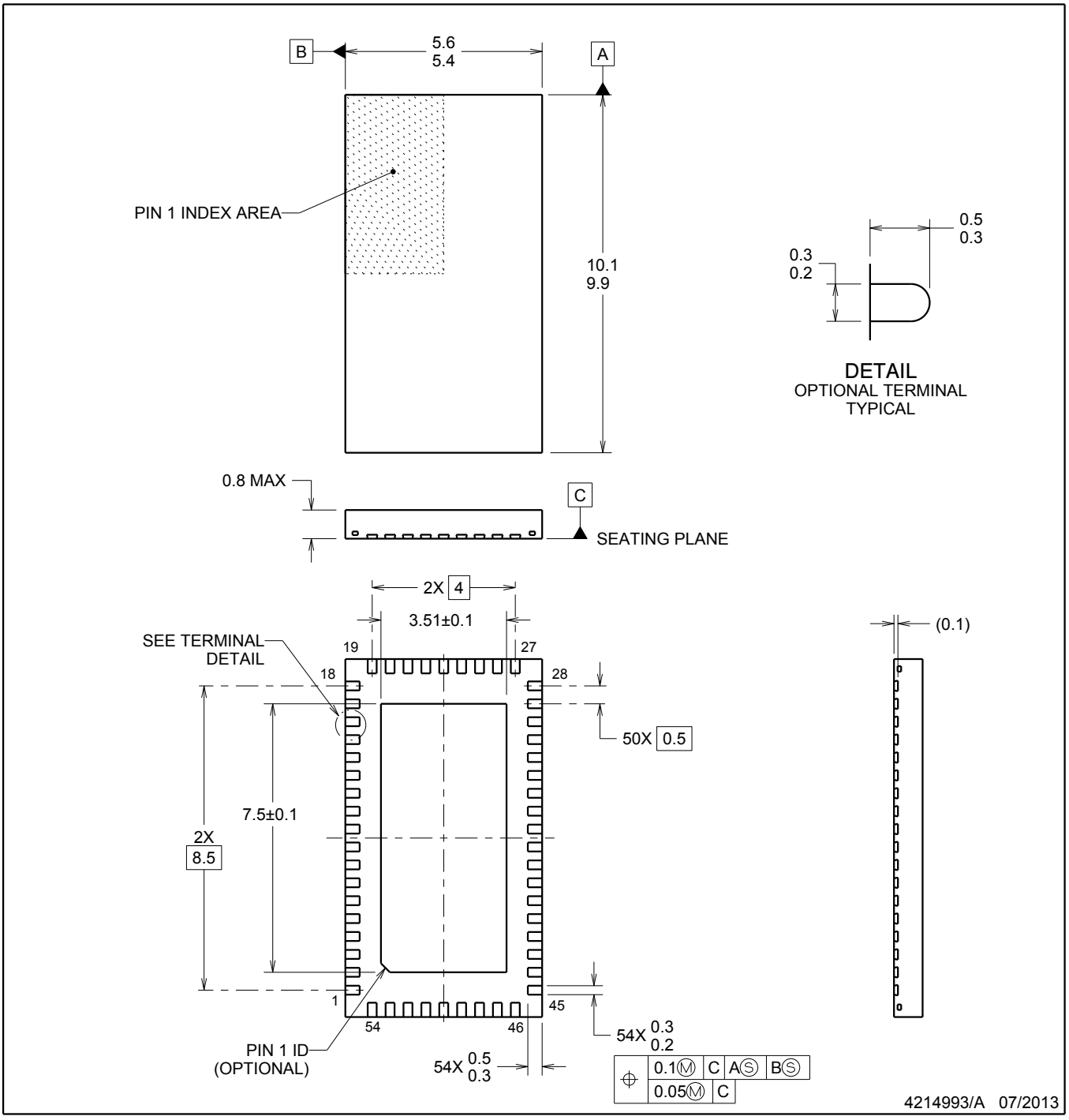
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS50PCI402SQ/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS50PCI402SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



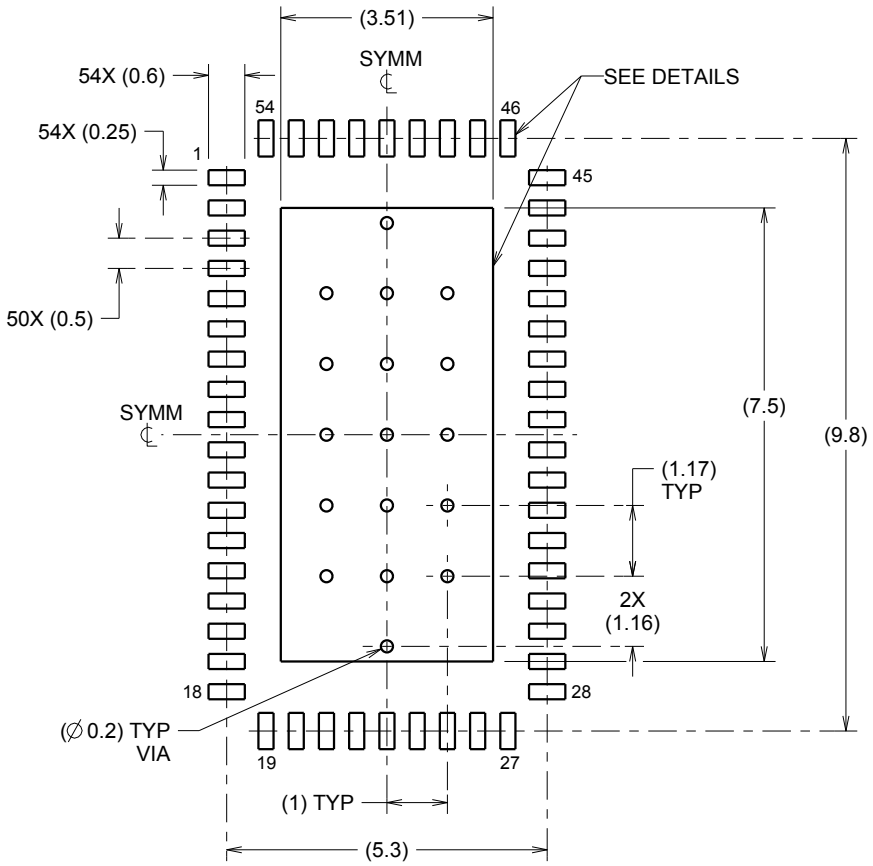
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS50PCI402SQ/NOPB	WQFN	NJY	54	2000	853.0	449.0	35.0
DS50PCI402SQE/NOPB	WQFN	NJY	54	250	208.0	191.0	35.0

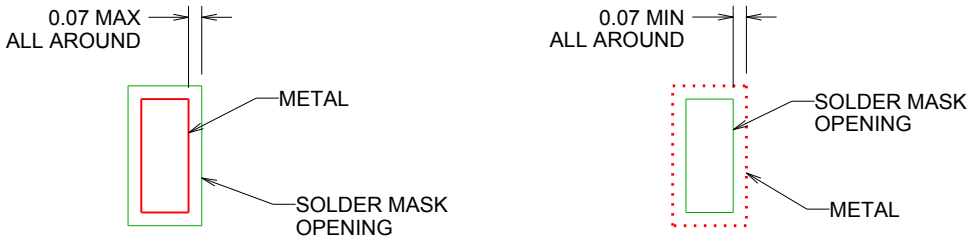


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

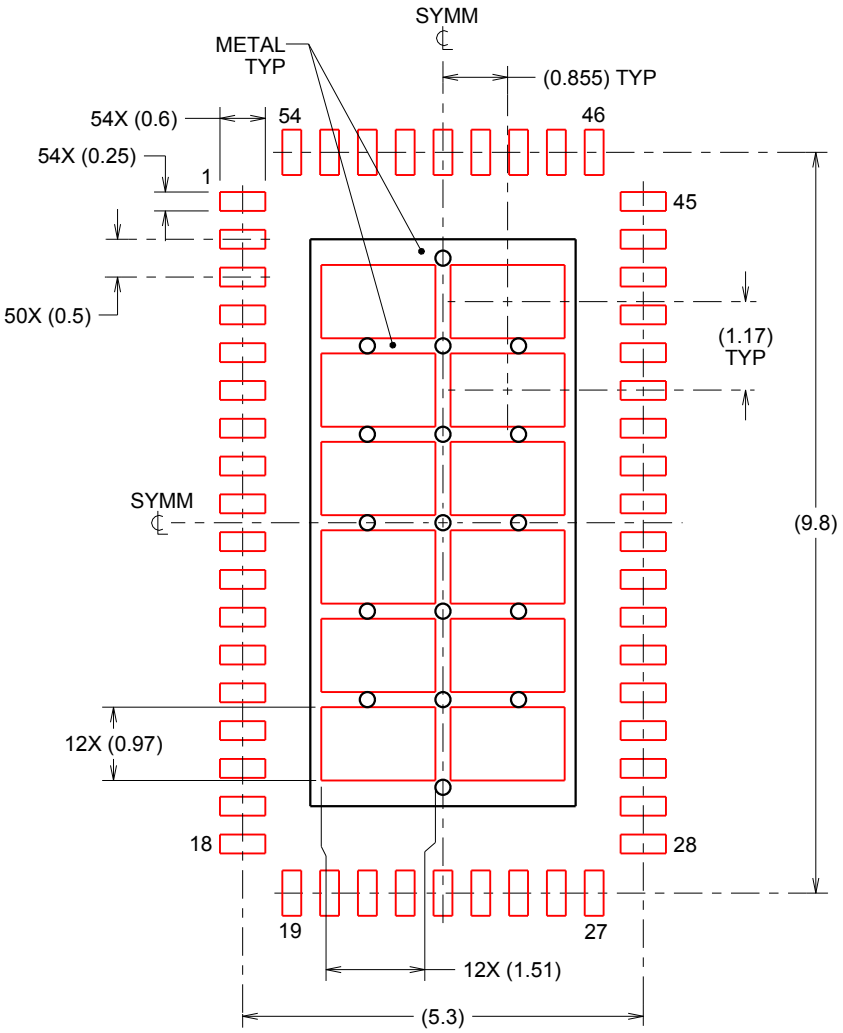
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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