1400 W 12 V phase-shift full-bridge with 600 V CoolMOS™ CFD7 and XMC™

EVAL_1K4W_ZVS_FB_SMD

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Scope and purpose

This document introduces a complete Infineon Technologies AG system solution for a 1400 W DC-DC converter from 400 V to 12 V, which achieves 97 percent peak efficiency. The EVAL_1K4W_ZVS_FB_SMD board is a DC-DC stage for server applications realized by a Phase-Shift Full-Bridge (PSFB) topology block.

This document shows the converter board using the 600 V CoolMOS™ CFD7 and 60 V OptiMOS™ 5 in a full Surface-Mount Device (SMD) solution with an innovative magnetic construction and cooling concept.

The Infineon components used in the 1400 W PSFB SMD are:

- 600 V CoolMOS™ CFD7 Super-Junction (SJ) MOSFET
- 60 V OptiMOS™ 5 Synchronous Rectifier (SR) MOSFET
- 2EDS8265H safety isolated and 1EDN7512G non-isolated gate drivers (EiceDRIVER™)
- XMC4200-F64k256AB microcontroller
- ICE5QSAG CoolSET™ Quasi Resonant (QR) flyback controller
- 950 V CoolMOS™ P7 SJ MOSFET
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC-DC step-down voltage regulator

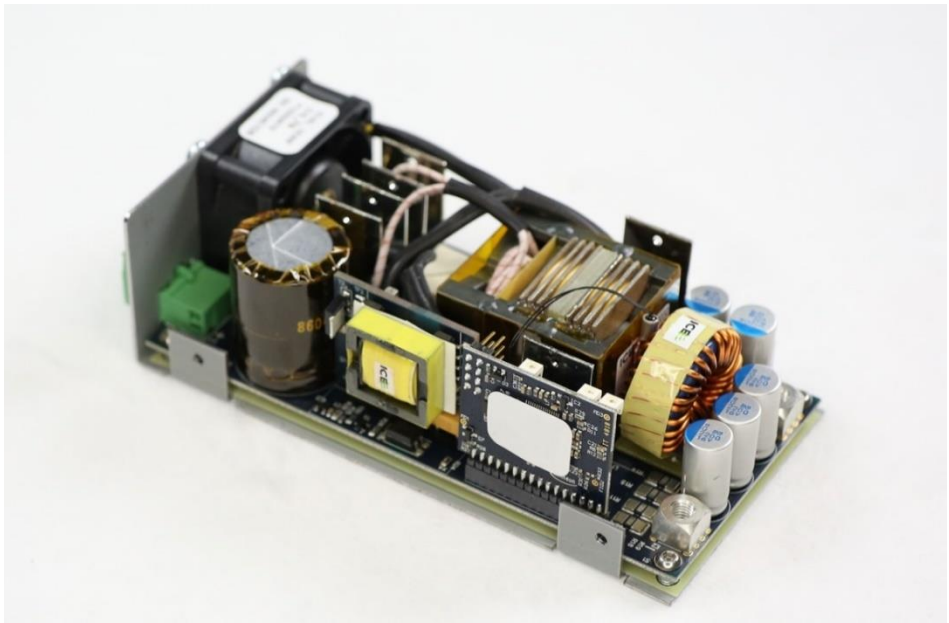

Figure 1 1400 W PSFB SMD

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1 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. In achieving this higher power density, high efficiency is a key parameter, because heat dissipation must be minimized.

Toward this goal, fully resonant topologies such as LLC are often considered to be the best approach in this power range and voltage class [3]. However, the 1400 W PSFB with SMDs is an example of how the improvement in semiconductor technology and control algorithms allows a simple and well-known topology block like PSFB to reach the high efficiency levels traditionally considered out of reach for this topology.

The efficiency shown in Figure 2 can be achieved by using a 600 V CoolMOS™ CFD7 in SMD package together with 60 V OptiMOS™ 5 SRs. The outstanding performance of these semiconductor technologies, the innovative cooling concept for a full SMD solution and the stacked magnetic construction enables a power density in the range of 3.70 W/cm^3 (60.78 W/in^3). Due to production tolerances, efficiency variations in the range of 0.1 percent could be expected in the results shown here.

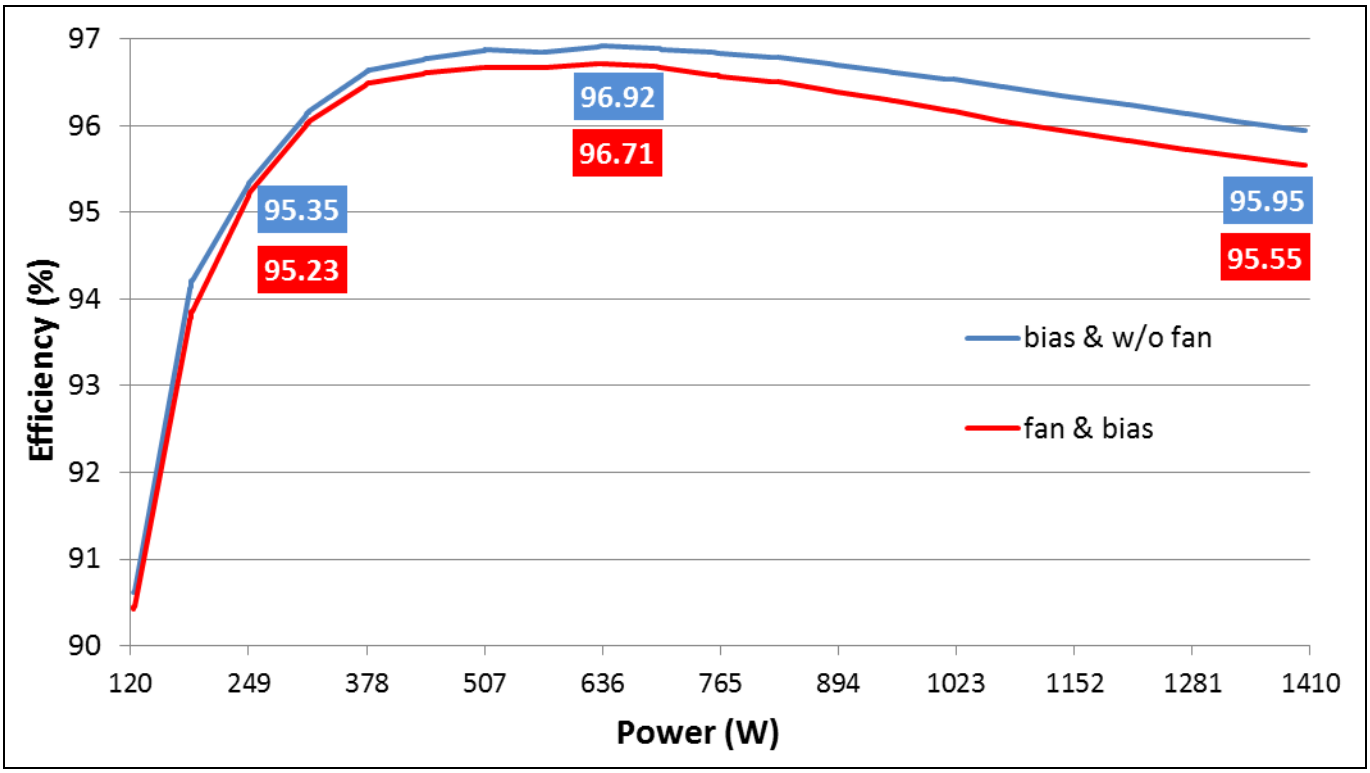

Figure 2 Measured efficiency of 1400 W SMD PSFB at 400 V input and 12 V output

The 1400 W PSFB SMD is a DC-DC converter developed with Infineon power semiconductors as well as Infineon drivers and controllers. The Infineon devices used in the implementation of the 1400 W PSFB SMD are:

- 140 mΩ 600 V CoolMOS™ CFD7 (IPL60R140CFD7) in the HV bridge
- 1.6 mΩ 60 V OptiMOS™ 5 in Super SO-8 package (BSC016N60NS5) in the LV bridge
- 2EDS8265H safety isolated and 1EDN7512G non-isolated gate drivers (EiceDRIVER™)
- ICE5QSAG QR flyback controller with external 4.5 Ω 950 V CoolMOS™ P7 (IPU80R4K5P7) for the auxiliary supply [4]
- XMC4200 microcontroller for control implementation (XMC4200-F64k256AB)
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC/DC step-down voltage regulator

This document will describe the system and board of the 1400 W PSFB SMD, as well as the specifications and main test results. For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search, and the different websites for the different implemented components:

- CoolMOS™ power MOSFETs
- OptiMOS™ power MOSFETs
- Gate driver ICs
- QR CoolSET™
- XMC™ microcontrollers

1.1 System description

The EVAL_1K4W_ZVS_FB_SMD design consists of a PSFB with SR in center-tapped configuration (Figure 3).

The control is implemented in an XMC4200 Infineon microcontroller, which includes voltage regulation functionality with peak current mode control, burst mode operation, output Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Under-Voltage Lockout (UVLO), soft-start, SR control, adaptive timings (bridge and SRs) and serial communication interface. Further details about the digital control implementation and further functionalities of PSFB in the XMC™ 4000 family can be found in [1] and [2].

The converter's nominal output is server level voltage class or 12 V. The stage is operated at a nominal input voltage of 400 V, whereas it can maintain regulation down to 360 V at full load (12 V nominal output voltage), providing enough room for hold-up time whenever the design is part of a full AC-DC converter.

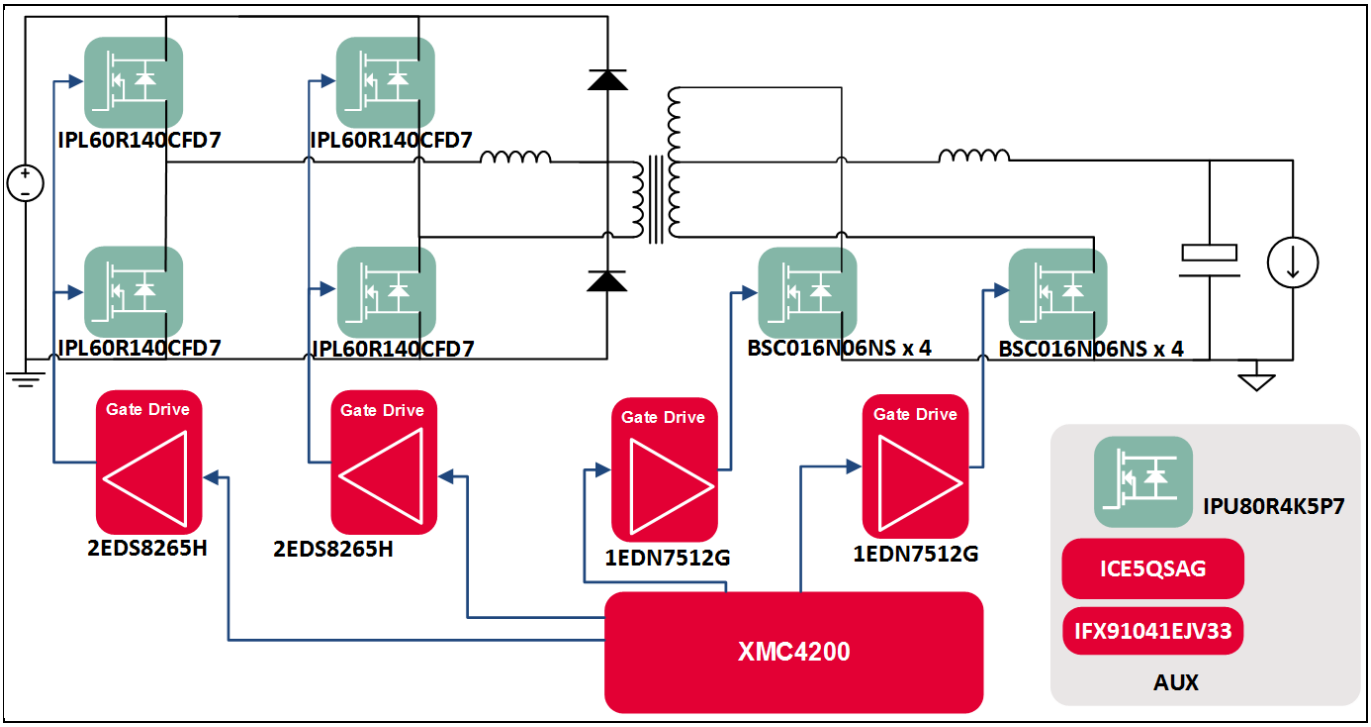

Figure 3 1400 W PSFB SMD (EVAL_1K4W_ZVS_FB_SMD) – simplified diagram showing the Infineon semiconductors used

Switching frequency of the converter is 100 kHz. The design was optimized for frequencies in the range of 90 to 110 kHz, as can be seen in the estimated efficiency versus frequency curves for the 40 percent, 50 percent and 60 percent load points in Figure 4.

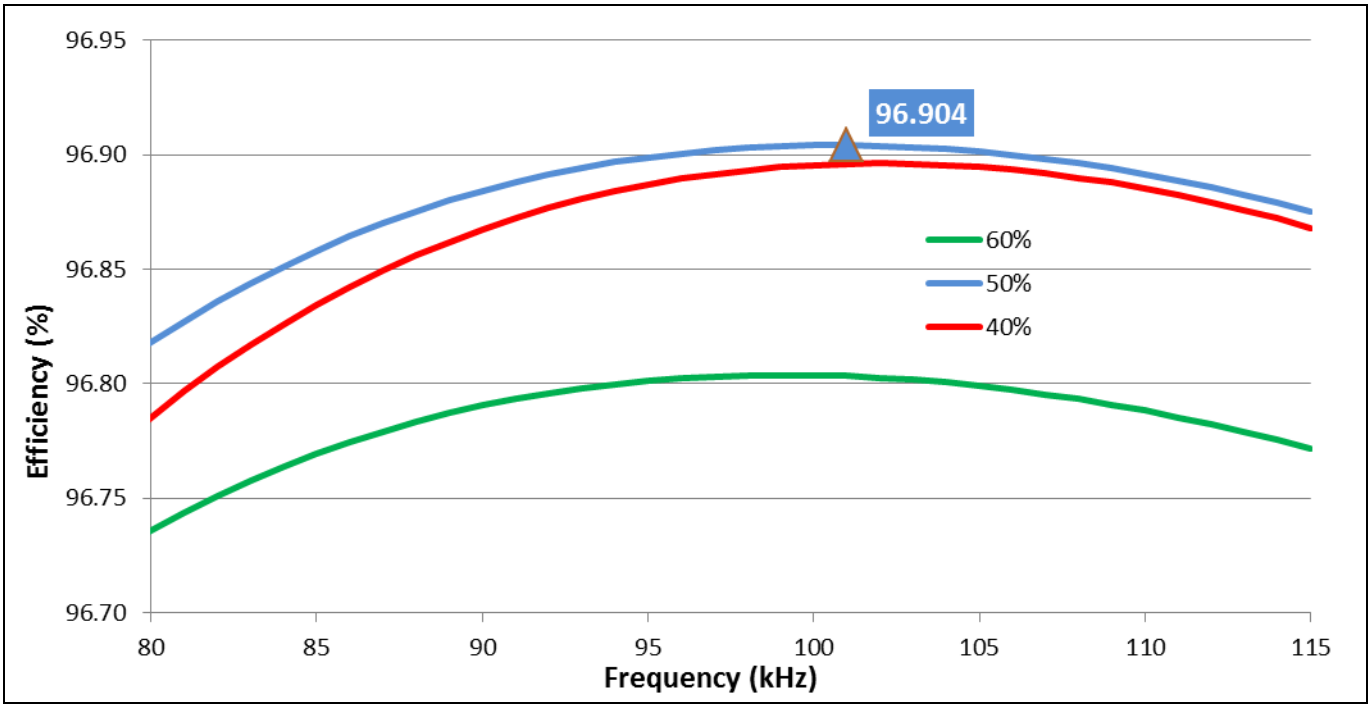

Figure 4 **Estimated efficiency of 1400 W PSFB SMD at different switching frequencies (fan consumption not considered) for the load points of interest. 400 V input and 12 V output.**

1.2 Board description

Figure 6 shows the placement of the different components on the 1400 W bi-directional PSFB. The outer dimensions of the board, enclosed in the case, are 133 mm x 64.5 mm x 44 mm, which results in a power density in the range of 3.70 W/cm^3 (60.78 W/in^3).

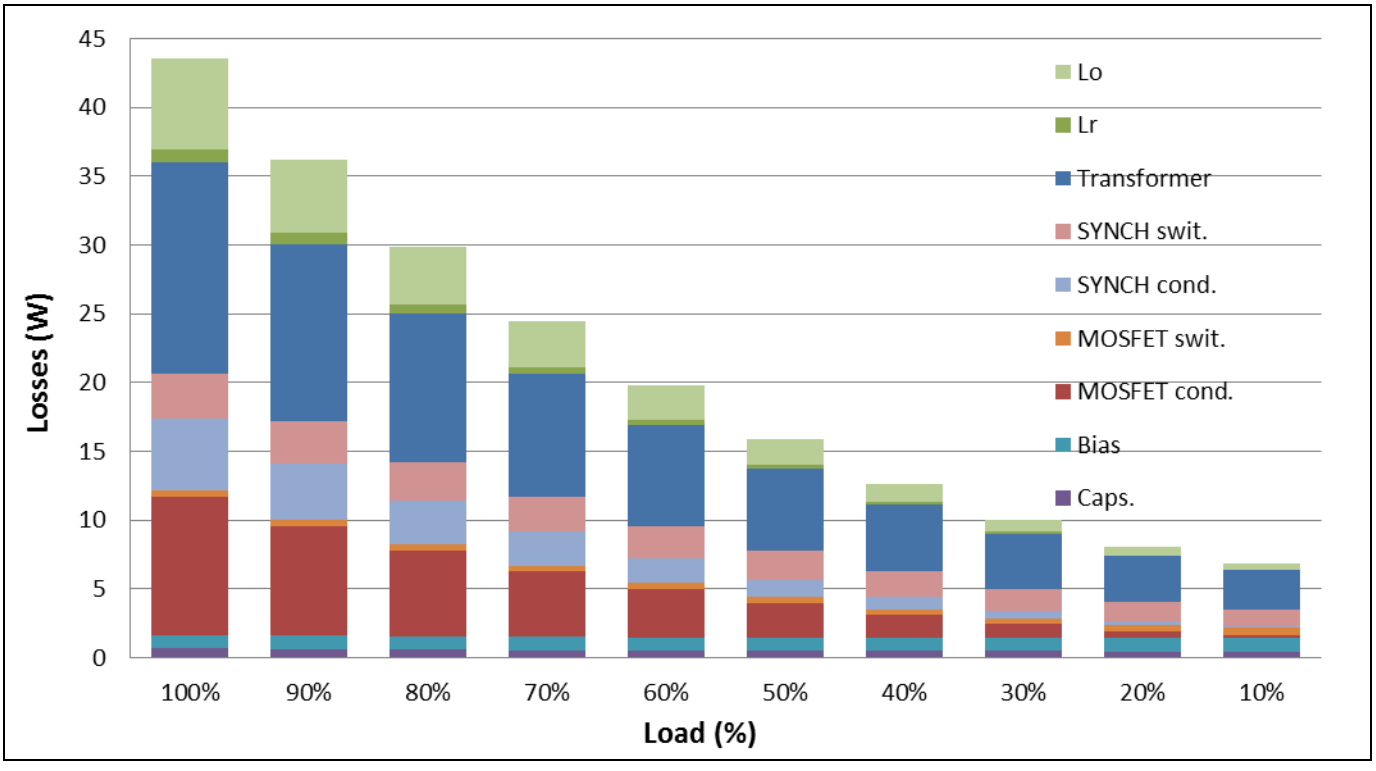

Figure 5 **Overall losses breakdown of 1400 W PSFB SMD along load. 400 V input and 12 V output.**

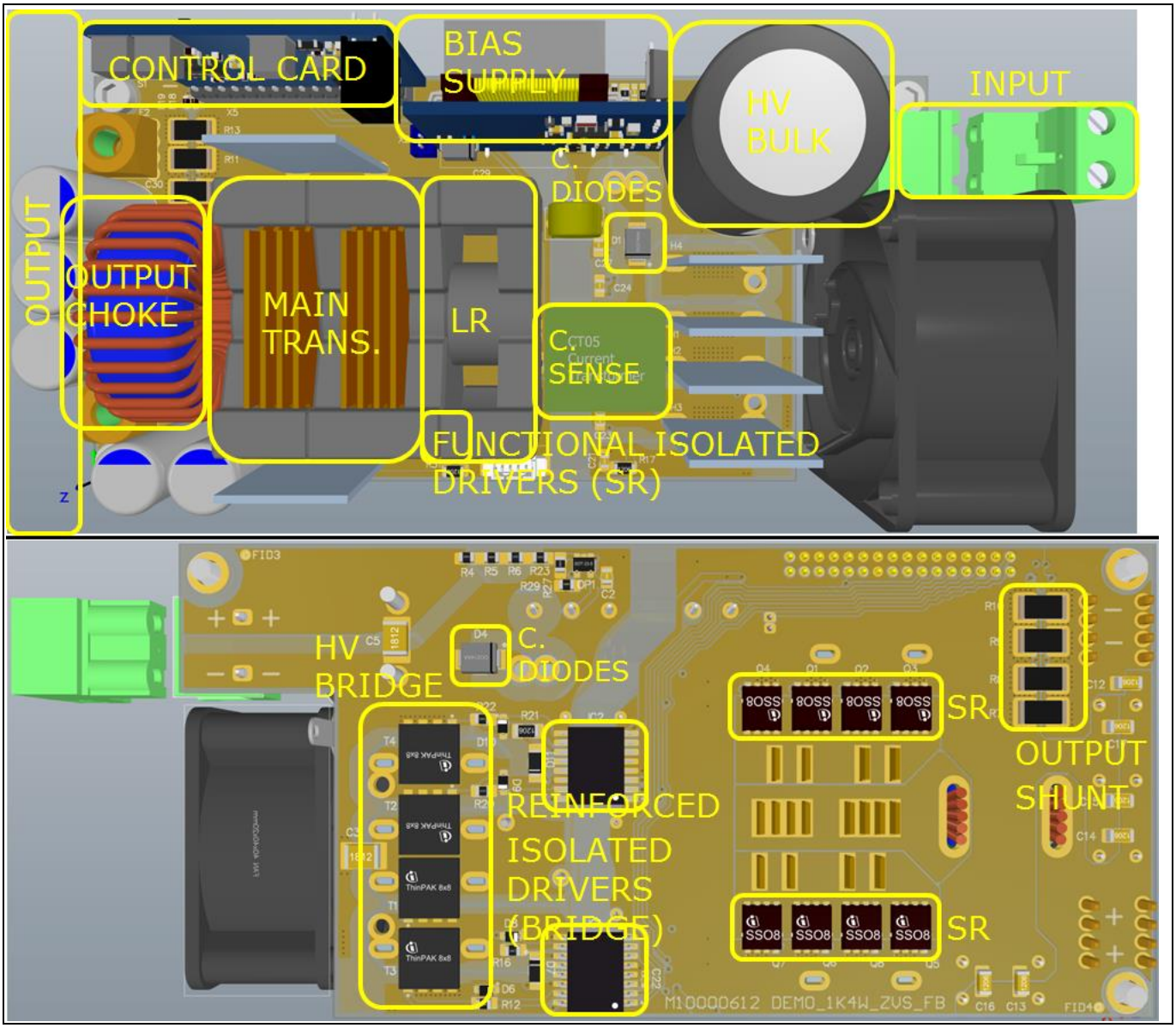

Figure 6 **Placement of the different sections in the 1400 W PSFB SMD with Infineon 600 V CoolMOS™ CFD7 and 60 V OptiMOS™ 5. Current Sense (CS), resonant inductor (Lr), SRs, clamping diodes (c. diodes).**

The estimated overall distribution of losses of the converter along the load proves the main transformer and other magnetics as the main sources of loss (Figure 5). The semiconductors, both the 600 V CoolMOS™ CFD7 and the 60 V OptiMOS™ 5, are best-in-class performance parts and exhibit a good balance of switching to conduction loss.

1.3 600 V CoolMOS™ CFD7

IPL60R140CFD7 stands for the 140 mΩ 600 V CoolMOS™ CFD7 in ThinPAK package, the latest and best-performance fast body diode device from Infineon.

IPL60R140CFD7 brings a low loss contribution along all load ranges and exhibits a good balance of conduction to switching losses at the 50 percent load point, becoming the right device and $R_{DS(on)}$ class when optimizing for high peak efficiency at that point (Figure 7).

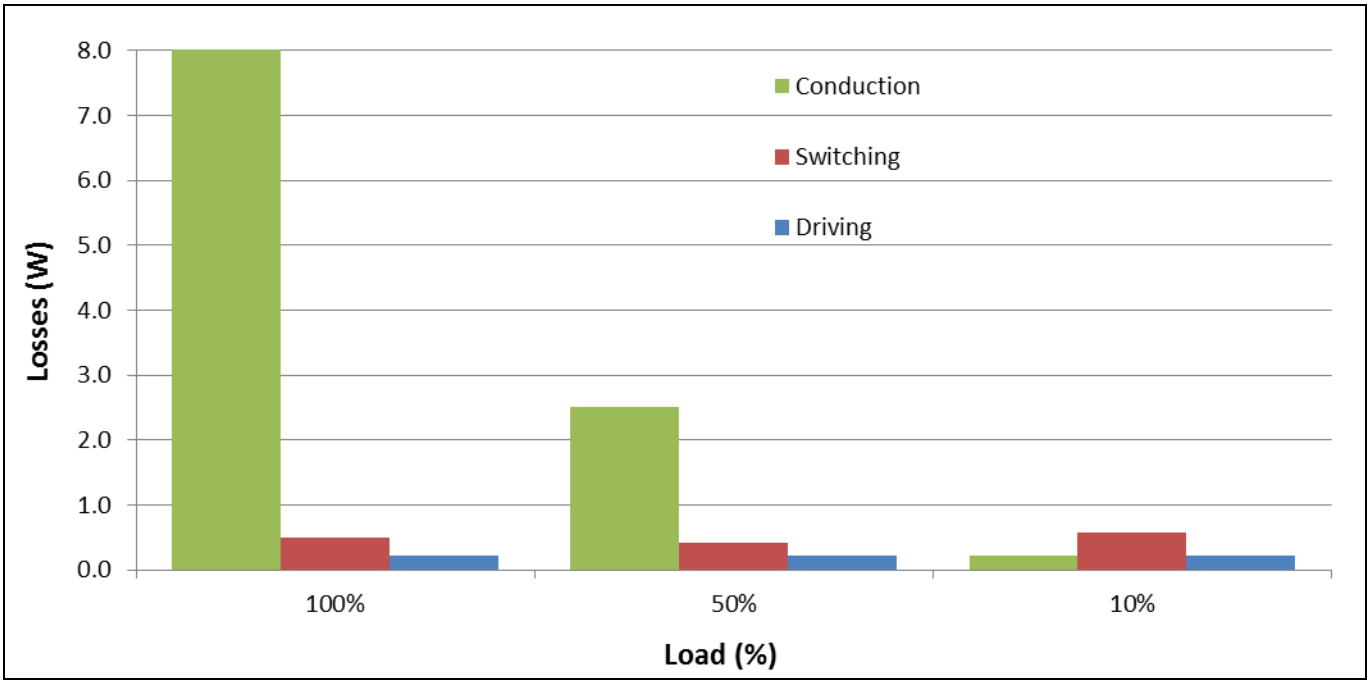

Figure 7 **IPL60R140CFD7 loss distribution (percentage of MOSFET contribution) along load in the 1400 W PSFB SMD. 400 V input and 12 V output.**

The proposed driving circuitry includes a single external resistor (54.9 Ω) in parallel to a medium-power Schottky diode BAT165 (Figure 8): the external turn-on resistor (54.9 Ω) plus the embedded MOSFET gate resistance (R_G) has no impact on turn-on losses under Zero Voltage Switching (ZVS) and keeps dv/dt and di/dt under control in the event of hard-switching turn-on (soft-start or no-load operation); the parallel Schottky diode provides a fast and nearly lossless turning off of the device. In summary the 600 V CoolMOS™ CFD7 achieves incomparable switching performance in all load conditions (Figure 7).

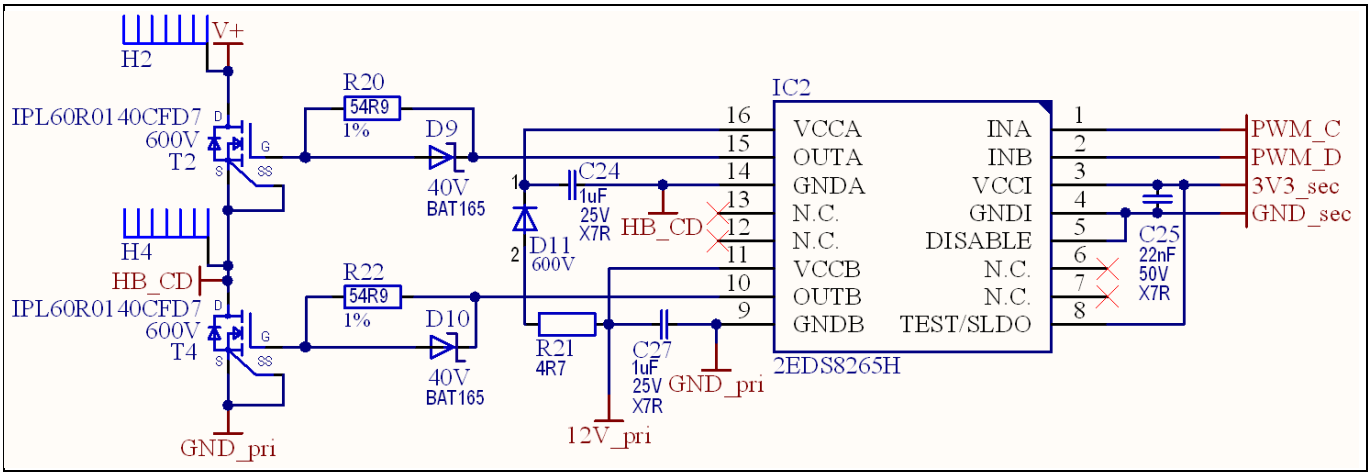

Figure 8 **Proposed driving configuration for IPL60R140CFD7 (half-bridge schematic)**

1.3.1 600 V CoolMOS™ CFD7 $R_{DS(on)}$ comparison

The 600 V CoolMOS™ CFD7 current portfolio in SMD ThinPAK packages (Figure 9) ranges from 225 mΩ (maximum) to 60 mΩ (maximum) (best-in-class device).

600 V CoolMOS™ CFD7 SJ MOSFETs

$R_{DS(on)}$ [Ω]	ThinPAK 8x8	$R_{DS(on)}$ [Ω]	ThinPAK 8x8
225*	IPL60R225CFD7*	115	IPL60R115CFD7
185	IPL60R185CFD7	95	IPL60R095CFD7
160	IPL60R160CFD7	75	IPL60R075CFD7
140	IPL60R140CFD7	60	IPL60R060CFD7

Figure 9 600 V CoolMOS™ CFD7 in ThinPAK $R_{DS(on)}$ portfolio. *Devices coming soon.

For this design IPL60R140CFD7 was chosen as a best compromise between 100 percent, 50 percent and 10 percent load points performance. However, other $R_{DS(on)}$ could be used for a different distribution of losses whenever there is interest in increasing performance in certain working points of the converter.

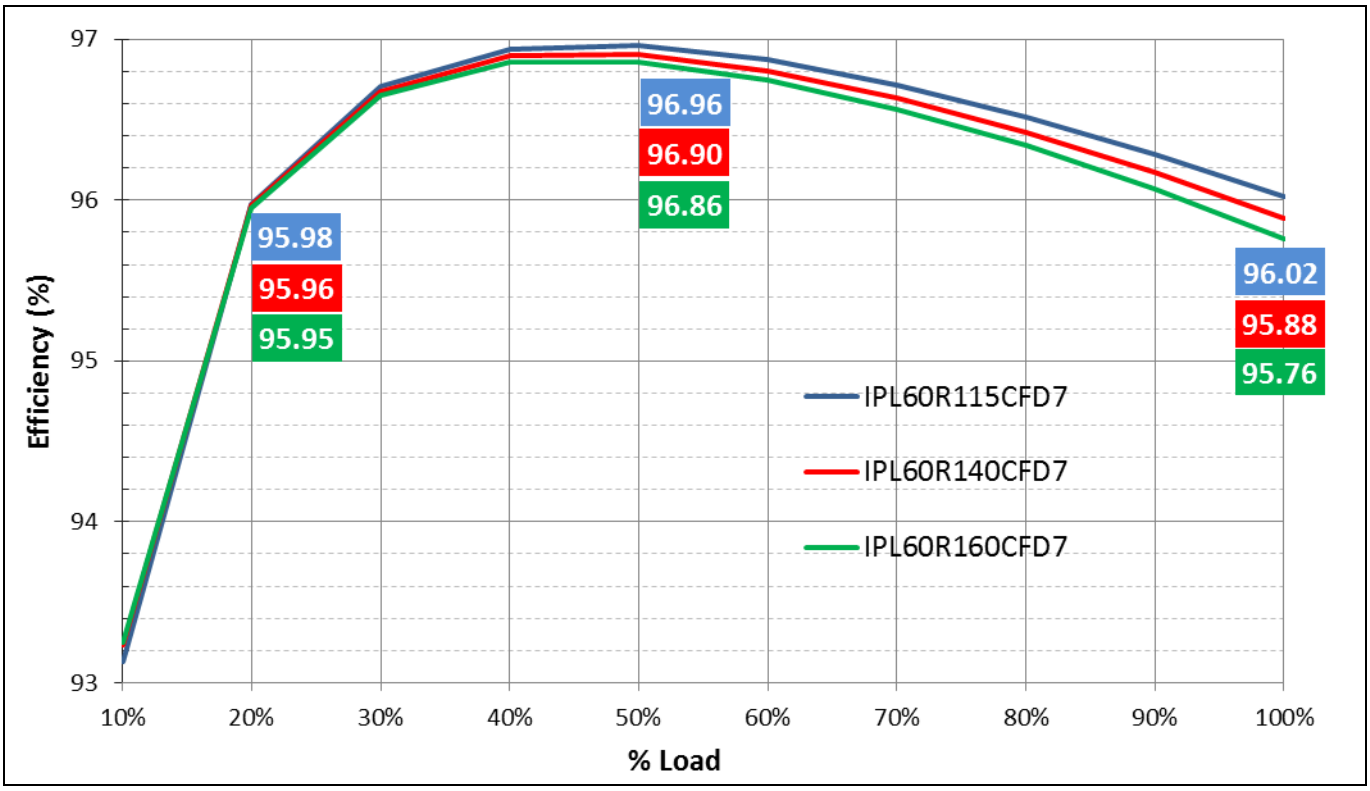

Figure 10 Estimated efficiency of 1400 W PSFB SMD with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK. 400 V input and 12 V output.

For example, here we present an estimated performance comparison of three different $R_{DS(on)}$ devices available in our portfolio: IPL60R140CFD7 (device currently on the design), IPL60R160CFD7 (one step higher $R_{DS(on)}$) and IPL60R115CFD7 (one step lower $R_{DS(on)}$).

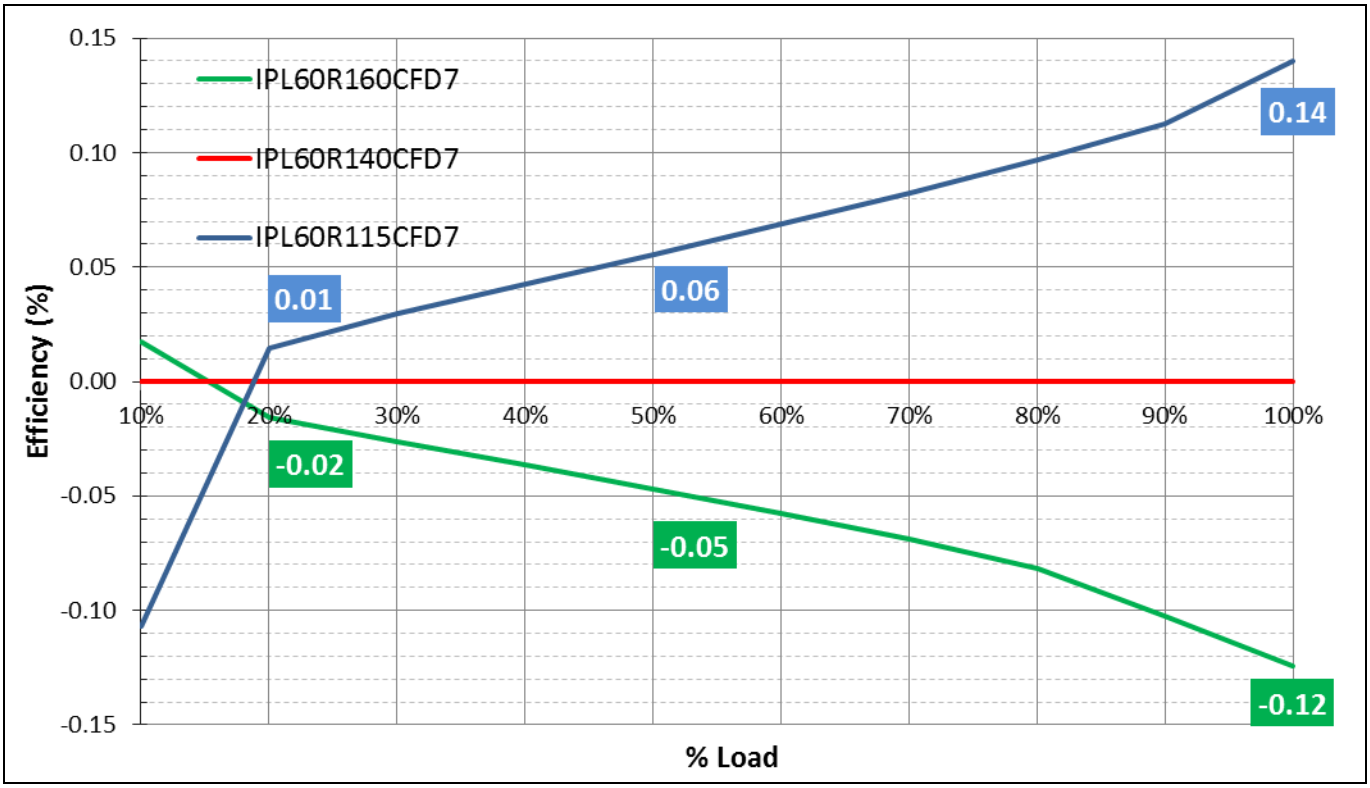

Figure 11 **Differential estimated efficiency of 1400 W PSFB SMD with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK. 400 V input and 12 V output.**

In Figure 12 you can see the estimation of losses at three main working points and how they balance for the three different $R_{DS(on)}$ values. Althought the difference in losses at 50 percent and 10 percent is small in comparison to the difference in losses at 100 percent, the impact in efficiency is still noticeable, as seen in Figure 11. The steep change on differential efficiency comparison between 20 percent and 10 percent is due to the loss of full ZVS at 10 percent and the different E_{oss} values for each $R_{DS(on)}$ values.

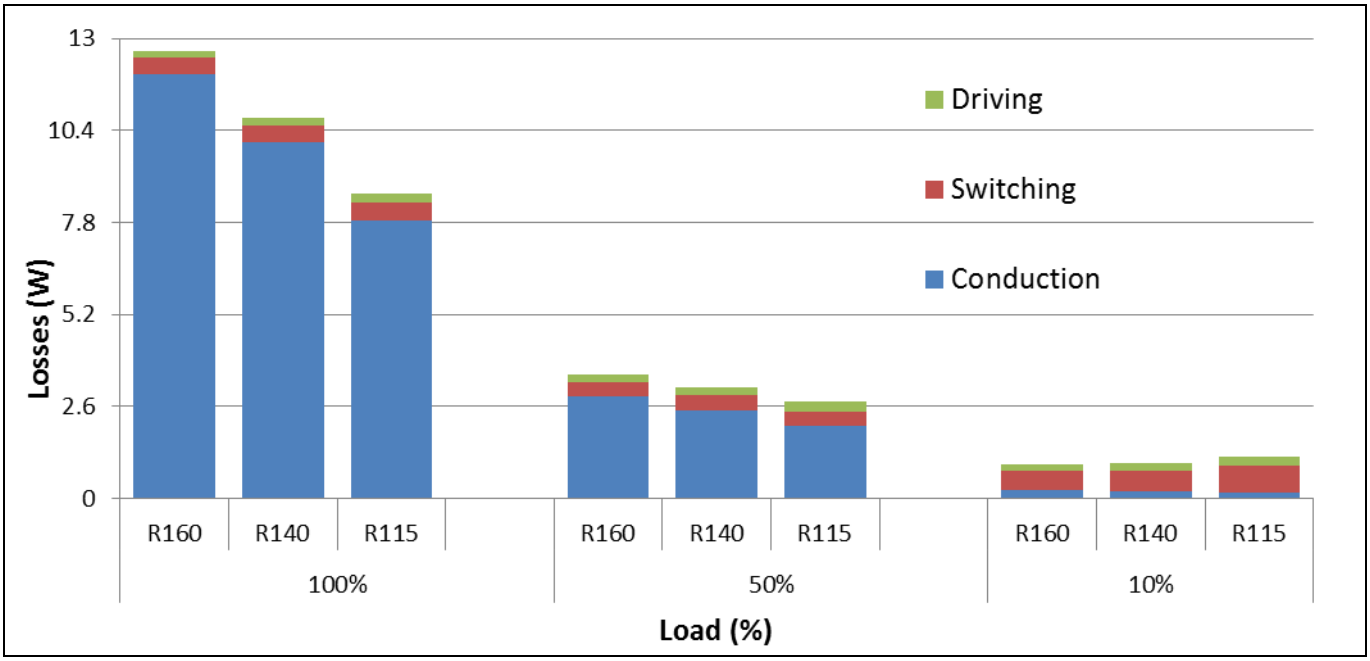

Figure 12 **Estimated distribution of losses of 1400 W PSFB SMD with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in ThinPAK. 400 V input and 12 V output.**

1.3.2 CoolMOS™ CFD2 comparison

CoolMOS™ CFD2 current portfolio in SMD ThinPAK packages ranges from 725 mΩ (maximum) to 165 mΩ (maximum) (best-in-class device).

For a fair comparison between technologies, here we compare IPL65R165CFD with a maximum $R_{DS(on)}$ of 165 mΩ against IPL60R160CFD7 with a maximum $R_{DS(on)}$ of 160 mΩ.

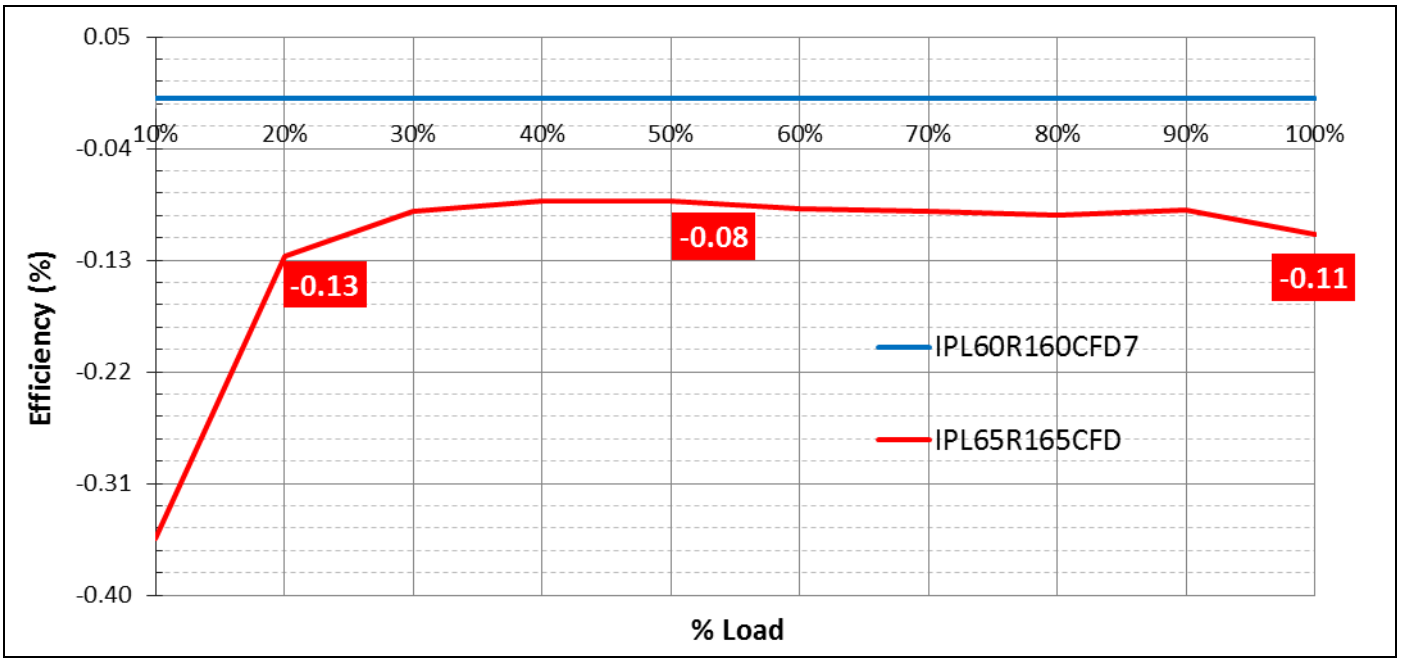

Figure 13 Differential estimated efficiency of 1400 W PSFB SMD with different CoolMOS™ fast body diode technologies. 400 V input and 12 V output.

Thanks to the Figure of Merit (FOM) of CFD7 technology we have the benefit of lower $R_{DS(on)}$ at mid and full load wihout any compromise in switching losses at light or medium loads. Thanks to this, the converter performs better in all load ranges when comparing CFD7 against CFD2 devices (Figure 13 and Figure 14).

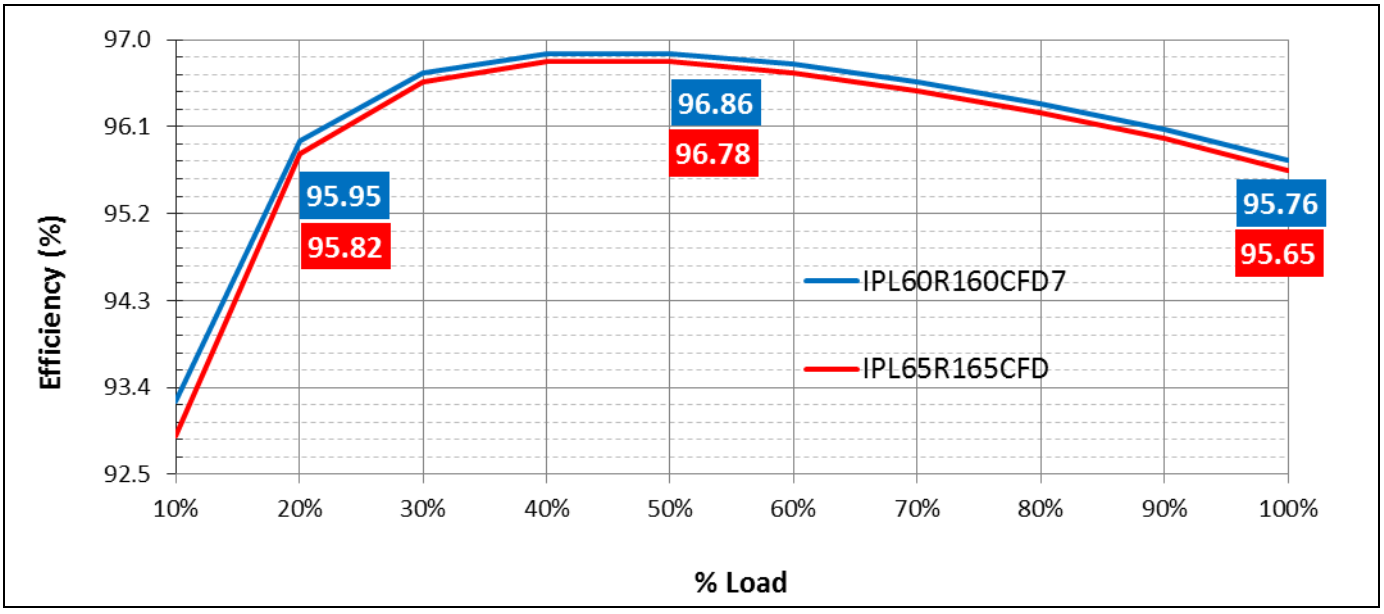

Figure 14 Estimated efficiency of 1400 W PSFB SMD with different CoolMOS™ fast body diode technologies. 400 V input and 12 V output.

Figure 15 shows the distribution of losses for the main working points. The lower input and output charge of CFD7 makes it have lower switching and driving losses even when using a lower equivalent $R_{DS(on)}$.

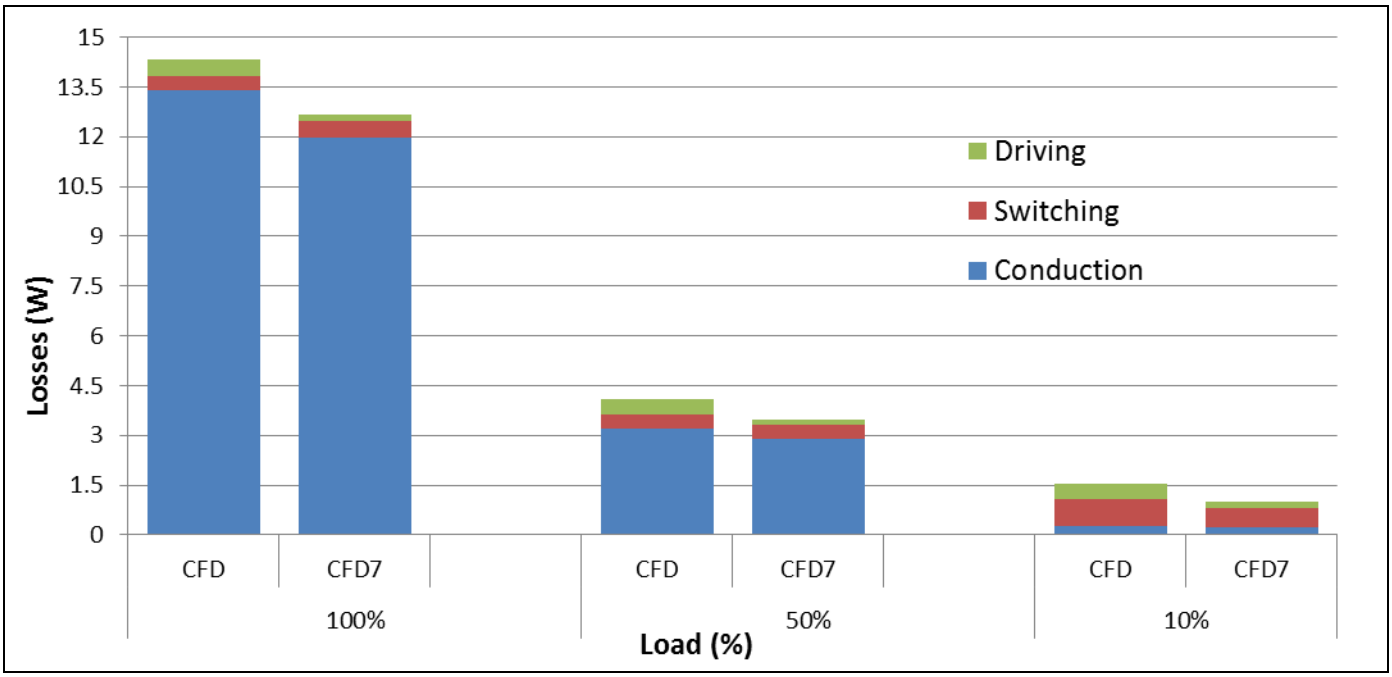

Figure 15 Estimated distribution of losses of 1400 W PSFB SMD with different CoolMOS™ fast body diode technologies. 400 V input and 12 V output.

1.4 Transformer

The main transformer has a turns ratio of 21 primary to 1 secondary, which gives 63 percent effective duty at nominal conditions (400 V input, 12 V output) or 3.15 µs at 100 kHz switching frequency.

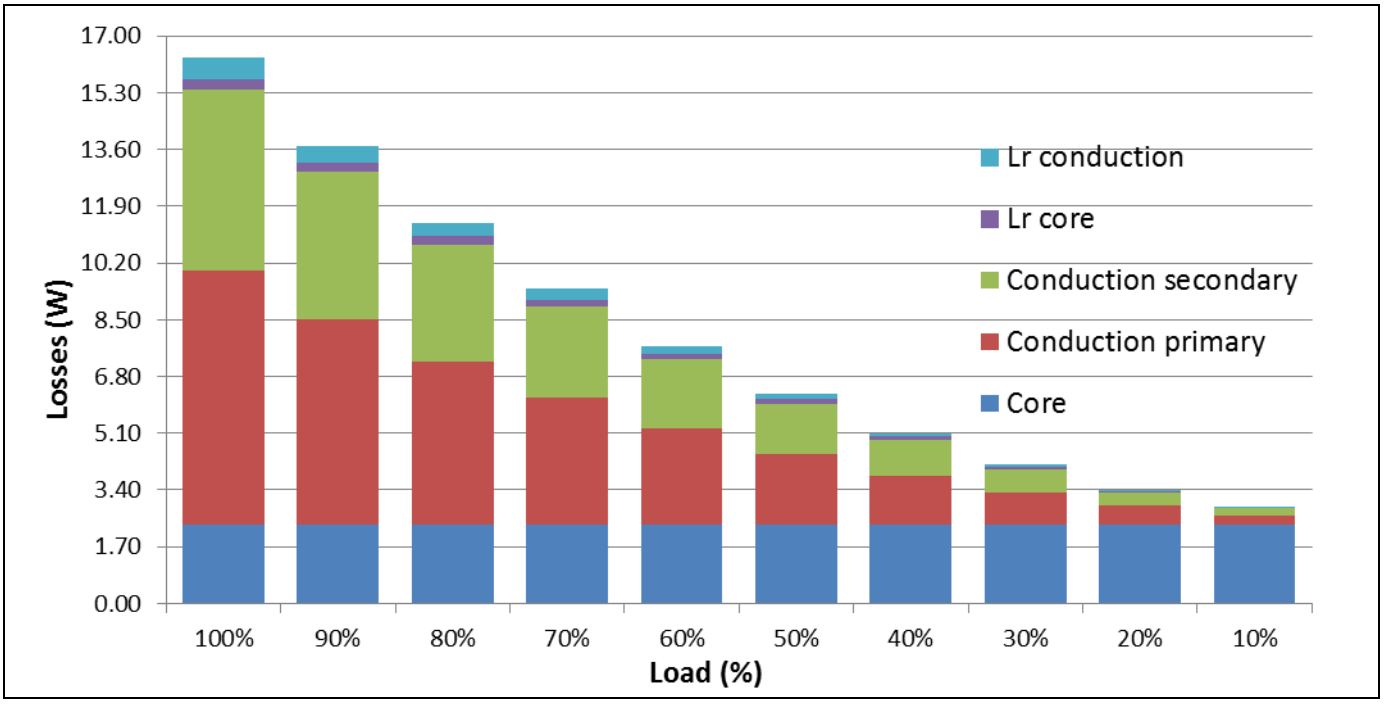

Figure 16 Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance (Lr). 400 V input and 12 V output.

Maximum flux peak (steady-state) is about 0.17 T, well below saturation flux density of the chosen core material: DMR95 from DMEGC.

The transformer has a planar-like construction on PQ35/28 core geometry from DMEGC. Primary winding has been realized with triple-insulated Litz wire made of seven strands of 0.3 mm diameter wire from Furukawa. Secondary winding is made of parallel tinned copper plates of 0.6 mm thickness.

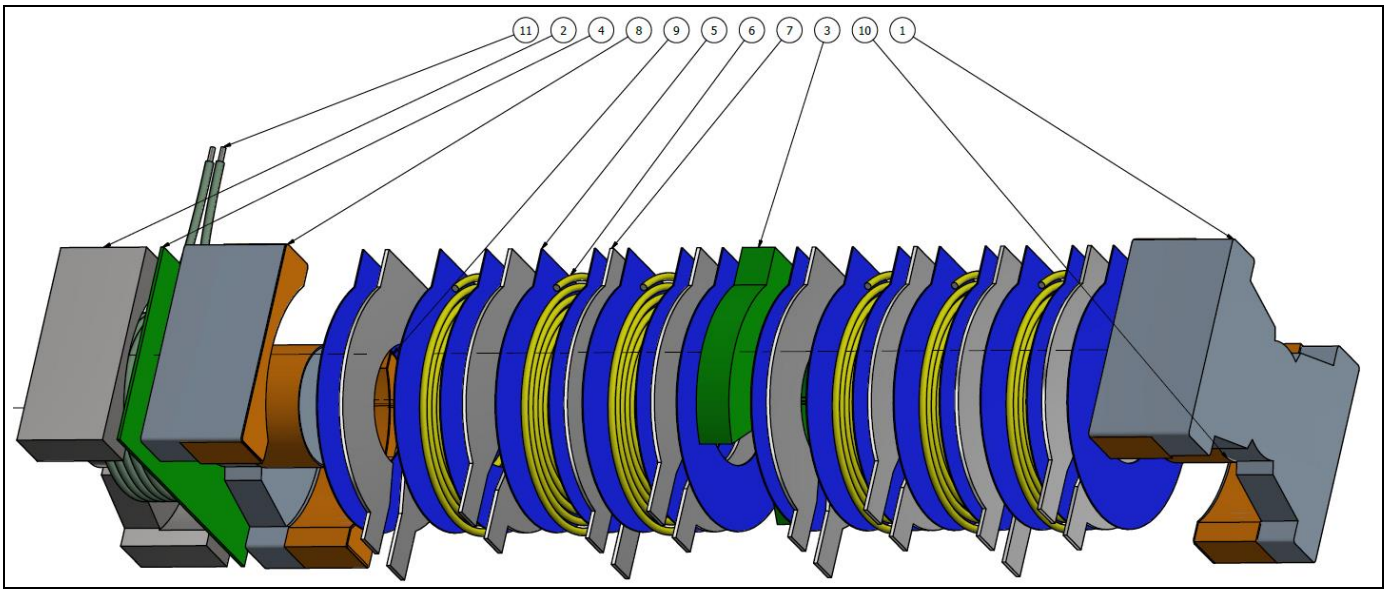

Figure 17 Main transformer and external resonant inductance. Mechanical drawing.

Figure 16 shows an estimated loss distribution of the full stacked magnetic structure. Notice that the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the nature of the converter.

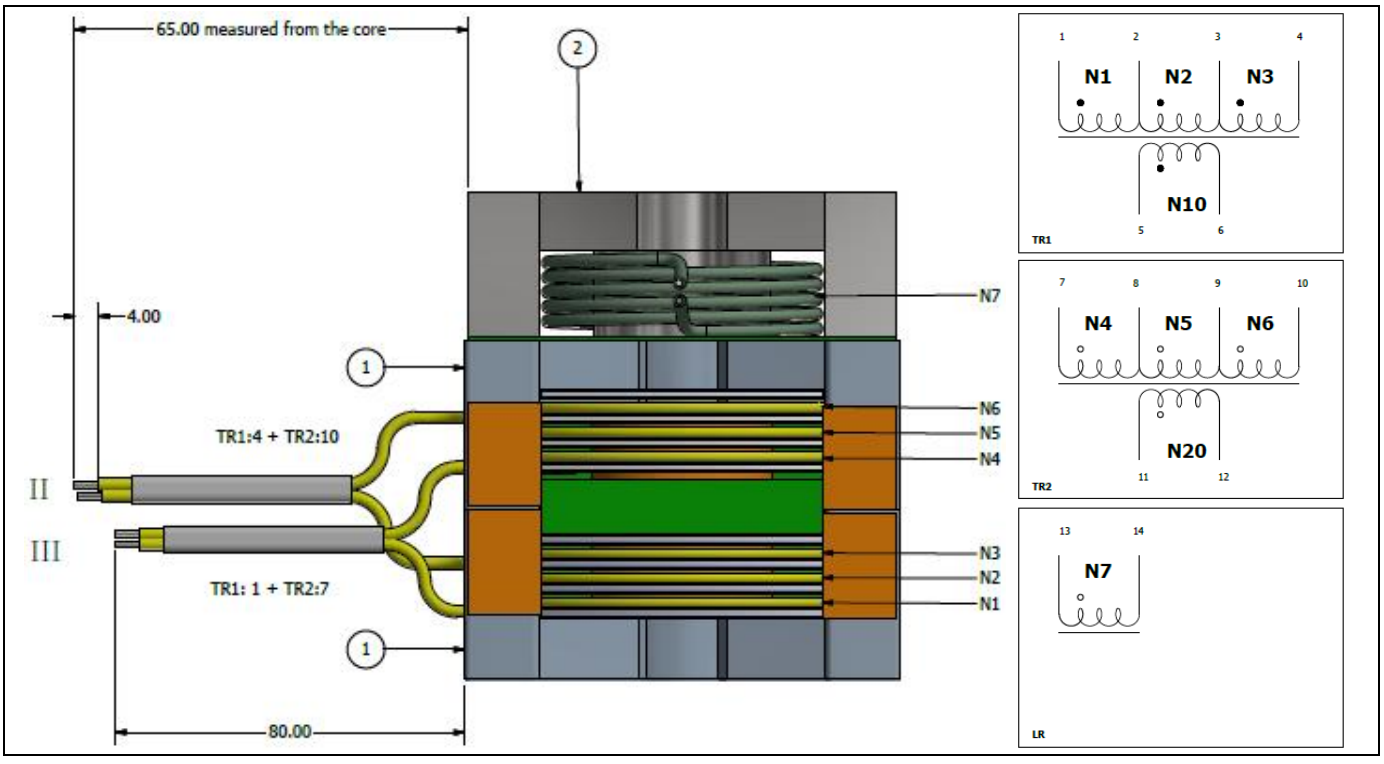

Figure 18 Main transformer and external resonant inductance. Mechanical drawing and schematic.

The winding technique and geometry of the core achieves good coupling (low leakage inductance, in the order of 500 nH) with relatively low intra- and inter-winding capacitances (in comparison to a full planar realization). This enables low drain voltage overshoot on the secondary-side devices and optimum voltage class selection (see 2.2.2).

The interleaving of primary and secondary windings achieves nearly full window utilization and minimizes proximity losses (at switching frequency and higher-order harmonics, on the spectrum of PSFB trapezoidal waveforms). A detailed description of the construction can be seen in Figure 17.

The main transformer structure actually comprises two parallel transformers integrated with the external resonant inductance (Figure 18).

1.5 Cooling solution

The proposed cooling solution for the full SMD design comprises a set of four copper plates for the HV bridge devices and two copper plates for the SR LV devices. The construction of the transformer, where secondary-side winding is made from copper plates, also constitutes part of the secondary-side LV devices' heatsink.

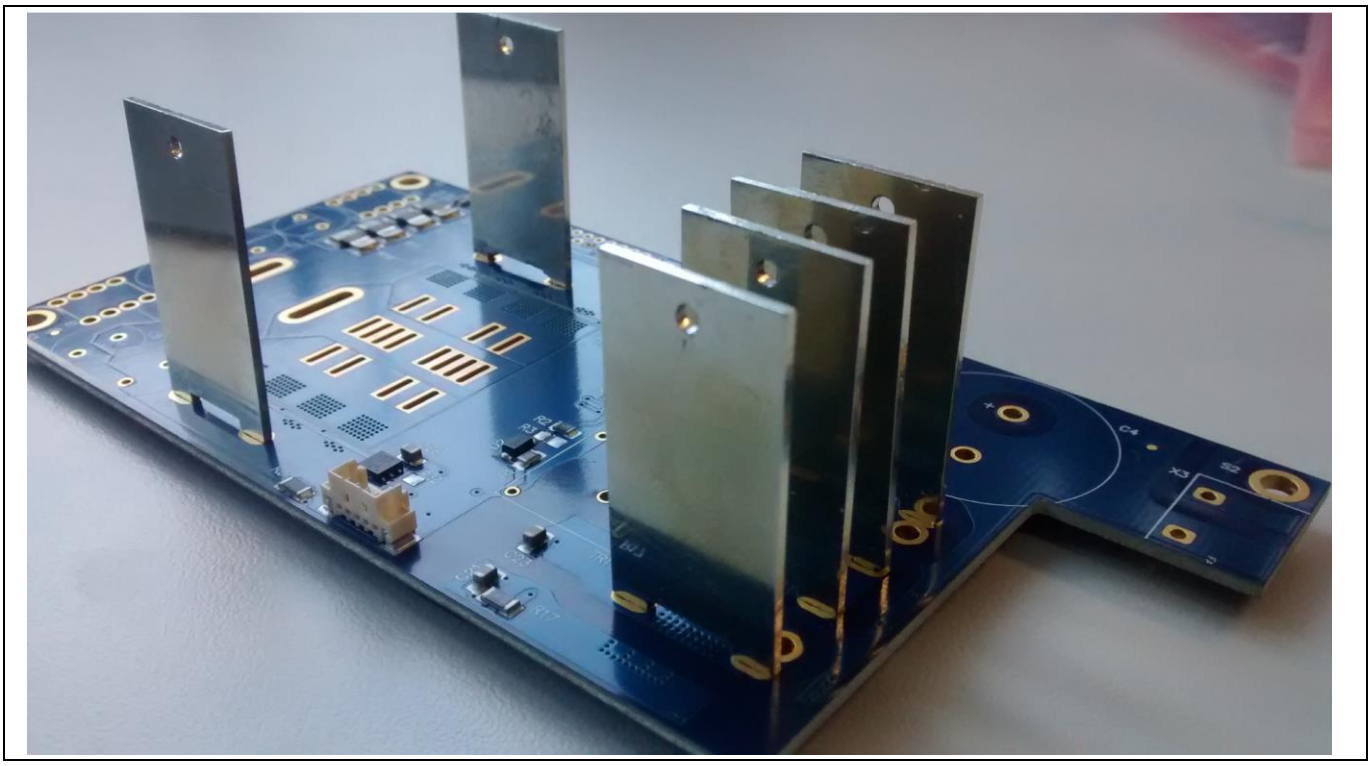

Figure 19 Heatsinks for HV bridge devices and LV secondary devices in a partially assembled 1400 W PSFB SMD converter board

A single fan extracts air from the unit, which flows uninterrupted along the HV bridge heatsinks thanks to their construction. This keeps air pressure low and maximizes the airflow capability of the fan. The fan speed is modulated along the load for best efficiency (see Figure 20), as little cooling effort is required at light and medium loads.

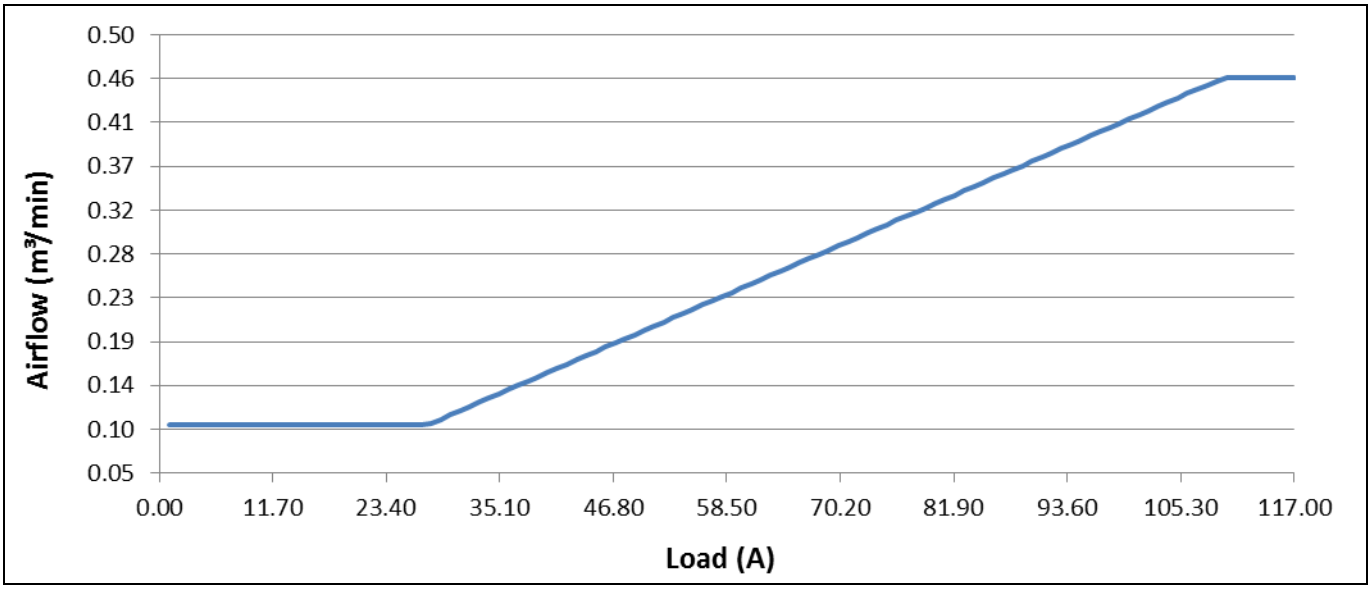

Figure 20 Fan airflow along converter load (assuming fan is working with low pressure)

Based on the estimation of losses for the HV bridge devices (four IPL60R075CFD7s), which at full load is approximately 10.55 W (considering both switching and conduction losses, but not driving, as most of the driving losses are dissipated on the external R_G and driver), some 2.64 W per device; and the measured temperature (see Figure 21) of approximately 75°C on the surface of the device packages, we can estimate thermal impedance of the proposed cooling solution in the range of 10°C/W from junction to air for the HV bridge devices (with the conservative assumption of 50°C airflow, as the air is heated up by the transformer and SRs before reaching the HV bridge heatsinks).

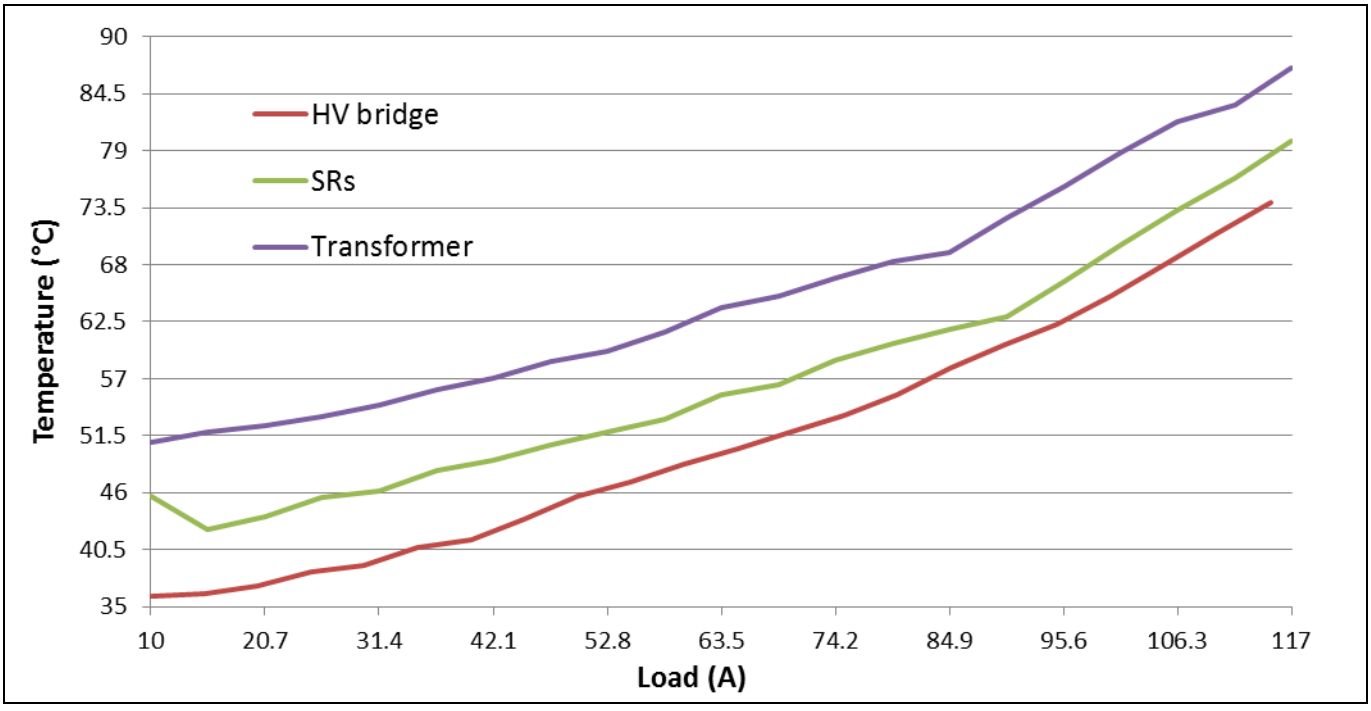

Figure 21 Measured temperatures on 1400 W PSFB SMD converter at 25°C room temperature and within enclosure

As can be seen, the proposed cooling solution is effective, with simple manufacture and assembly, and low cost. This cost saving would enable the use of even lower $R_{DS(on)}$ for an even better performance (see 0).

1.6 EiceDRIVER™ 2EDSx reinforced isolated and 1EDN7512G non-isolated gate driver

The EiceDRIVER™ 2EDi is a family of fast dual-channel isolated MOSFET gate-driver ICs providing functional (2EDFx) or reinforced (2EDSx) input-to-output isolation by means of Coreless Transformer (CT) technology. Due to high driving current, excellent common-mode rejection and fast signal propagation, 2EDi is particularly well suited to driving medium- to high-voltage MOSFETs (CoolMOS™, OptiMOS™) in fast-switching power systems with the following features.

- 4 A/8 A source/sink output current

  The low-ohmic output stage of the EiceDRIVERTM family allows, in this topology, the fast turn-on and turn-off of the HV bridge CoolMOSTM with the best-in-class low source resistance (0.85 Ω for 4 A source current) and sink resistance (0.35 Ω for 8 A sink current) of an isolated gate driver.

- PWM signal propagation delay typ. 37 ns with 3 ns channel-to-channel mis-match and +7/-6 ns propagation delay variance

  The isolated gate driver 2EDS8265H provides typical 37 ns propagation delay with an internal input filter in order to attenuate the noise with pulse width below 18 ns. The best class of +7/-6 ns propagation delay accuracy assures a tight delay window for designers. Meanwhile the designer can benefit from maximum 3 ns channel-to-channel mis-match in a half-bridge design or driving parallel MOSFETs.

- Common Mode Transient Immunity (CMTI) greater than 150 V/ns

  The CMTI indicates the robustness of the IC to fast voltage transients (dv/dt) between its two isolated grounds; the dv/dt causes a current flow through the parasitic input-to-output (CIO) capacitance of the IC, corrupting the transmitted gate signal. The isolated EiceDRIVERTM, thanks to the CT technology, shows a robust CMTI (greater than 150 V/ns) compared to the gate transformer.

- Fast safety turn-off in case of input-side UVLO

  The 8 V UVLO for the 2EDS8265H suits the transfer characteristic of the HV IPL60R140CFD7. In general, an 8 V UVLO works for complete CoolMOSTM and normal-level OptiMOSTM, and 4 V UVLO works for logic-level OptiMOSTM products to maintain safe operation and turn-off in case of gate driver supply drop-off.

Here each 1EDN7512G is used to drive four 1.6 mΩ 60 V OptiMOS™ 5 (BSC016N60NS5) devices:

- 4 A/8 A source/sink output current

  The low-ohmic output stage of the EiceDRIVERTM family allows, in this topology, the fast turn-on and turn-off of the LV OptiMOSTM (four in parallel) with the best-in-class low source resistance (0.85 Ω for 4 A source current) and sink resistance (0.35 Ω for 8 A sink current) of an isolated gate driver.

- PWM signal propagation delay typ. 19 ns with +6/-4 ns propagation delay variance

  The non-isolated gate driver 1EDN7512G provides typical 19 ns propagation delay with an input filter internally in order to attenuate the noise with pulse width below 10 ns. The best class of +6/-4 ns propagation delay accuracy assures a tight delay window for designers.

Driving HV half-bridge device configuration requires the supply of the high-side driving stage, generally done with bootstrapping capacitors and a decoupling HV diode from the low-side driving supply. However, bootstrapping capacitors are initially discharged and can also self-discharge while the converter is in an idle state (e.g. during burst mode operation).

The controller should provide a starting sequence that enables the bootstrapping capacitors charge up before applying pulses to the high-side devices. This could be done in one of several possible ways. Here we apply charging pulses on the low-side devices before starting (Figure 22) or resuming switching (after a configurable idle time) (Figure 23).

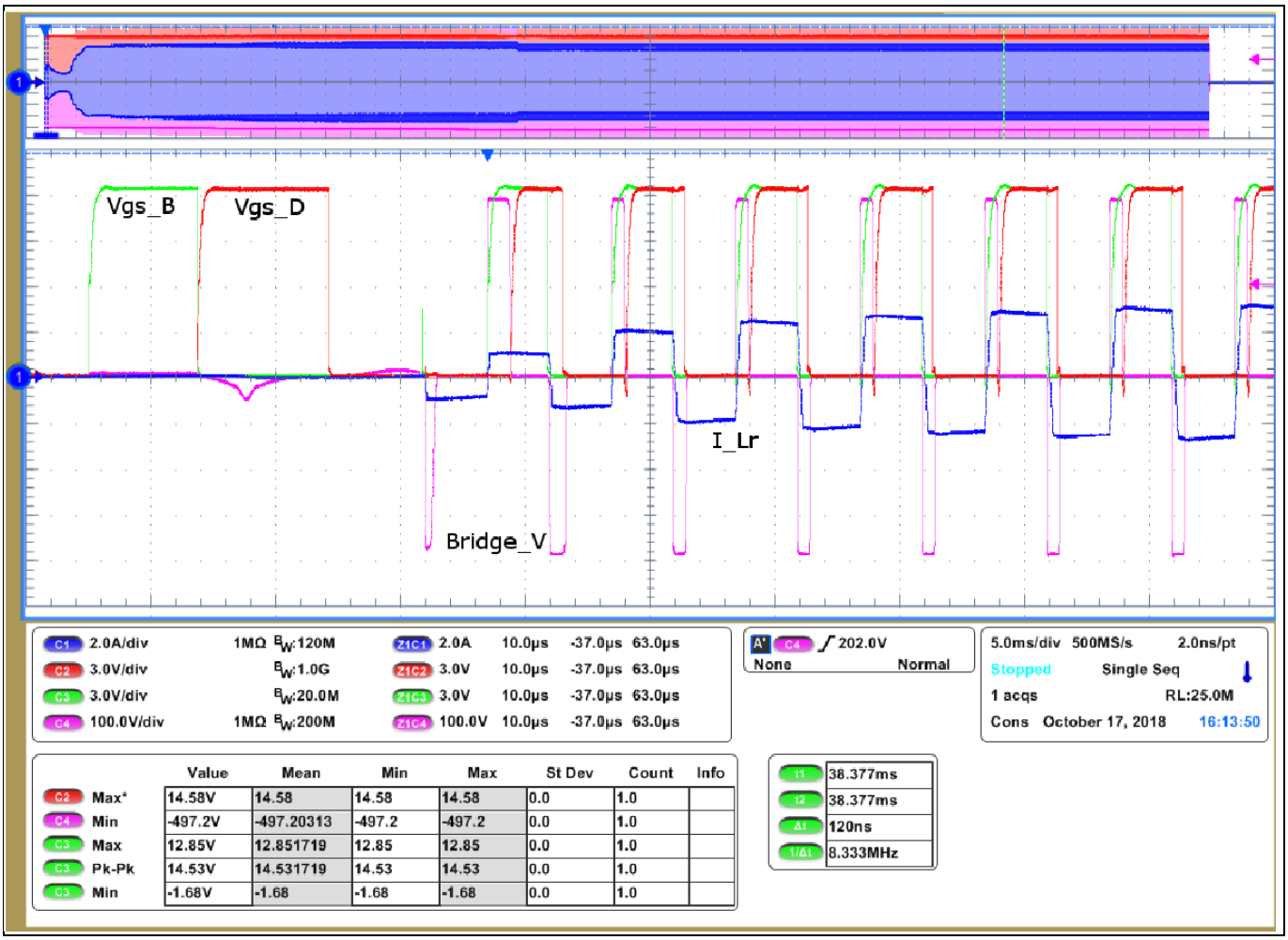

Figure 22 Soft-start with bootstrap capacitors pre-charge

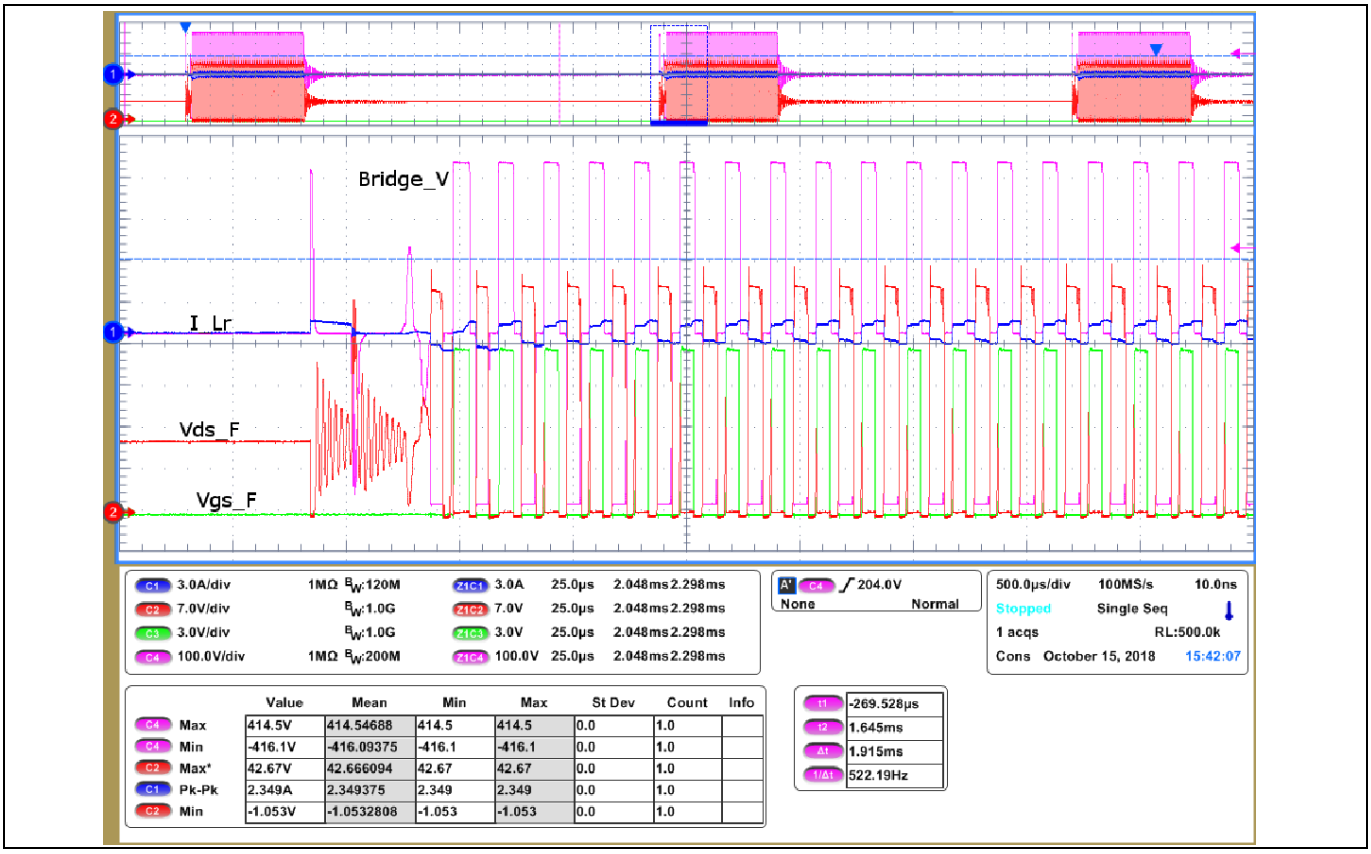

Figure 23 Burst operation with pre-charge of bootstrapping capacitors

1.7 Validation set-up

For validation of the buck mode operation of the 1400 W PSFB SMD, the suggested set-up includes:

- HV supply capable of 400 V and at least 1500 W (when testing up to full load)
- LV electronic load (0 to 12 V), in constant current mode, capable of at least 1400 W (when testing up to full load)

Nominal input voltage of the converter is 400 V. The converter starts to operate at 375 V, turning off with a hysteresis window down to 350 V, as shown in Figure 24.

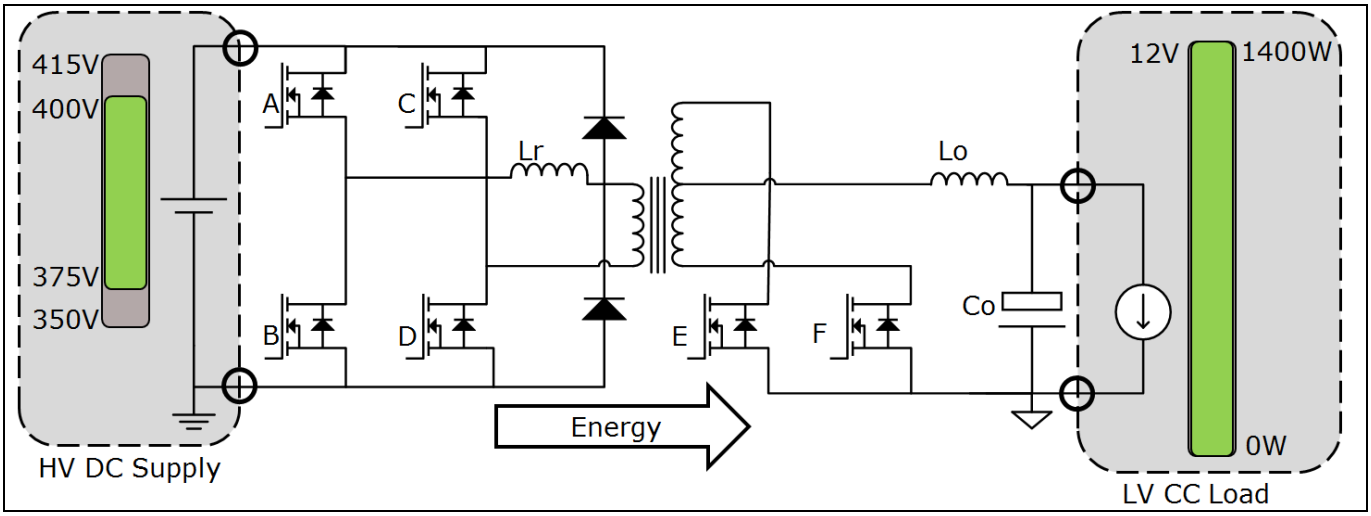

Figure 24 Buck mode recommended validation set-up

2 Buck mode results

2.1 Specification and test results

This chapter shows the specifications, performance and behavior of the 1400 W PSFB SMD with 600 V CoolMOS™ CFD7. Table 1 shows the demonstrator performance and specifications under several steady-state and dynamic conditions.

Table 1 Summary of specifications and test conditions for the 1400 W PSFB SMD

Test	Conditions	Specification
Efficiency test	400 V input, 12 V output	η_{pk} = 96.92 percent at 630 W (45 percent load)
Output voltage		12 V
Steady-state V_{out} ripple	400 V input, 12 V output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
UVLO	375 V on to 350 V off	Analog hysteresis window comparator
Load transient	5 A ↔ 60 A, 1 A/µs	$\lvert\Delta V_{out}\rvert$ less than 600 mV_{pk}
	60 A ↔ 117 A, 1 A/µs	
OCP	118 to 119 A	Shut-down and resume
	120 A	Shut-down and latch
	Output terminals in short-circuit	Detection within switching period Shut-down and latch

2.2 Performance and steady-state waveforms

2.2.1 HV full-bridge

The low E_{oss} energy of IPL60R140CFD7 results in full ZVS of the lagging leg (switches C, D) down to 15 percent load and partial ZVS of the leading leg (switches A, B) in light-load conditions (Figure 25) with full ZVS at 35 percent load and above.

With partial ZVS only a small part of the E_{oss} is lost, and consequently switching losses of CFD7 are low at any load conditions and the overall loss contribution along all load ranges of the converter is also relatively low (Figure 5 and Figure 7).

An additional benefit of the low E_{oss} energy and having near ZVS transition at no load is the lower dv/dt values and lower or no drain voltage overshoot of the HV MOSFETs due to the smooth QR transitions (better EMI).

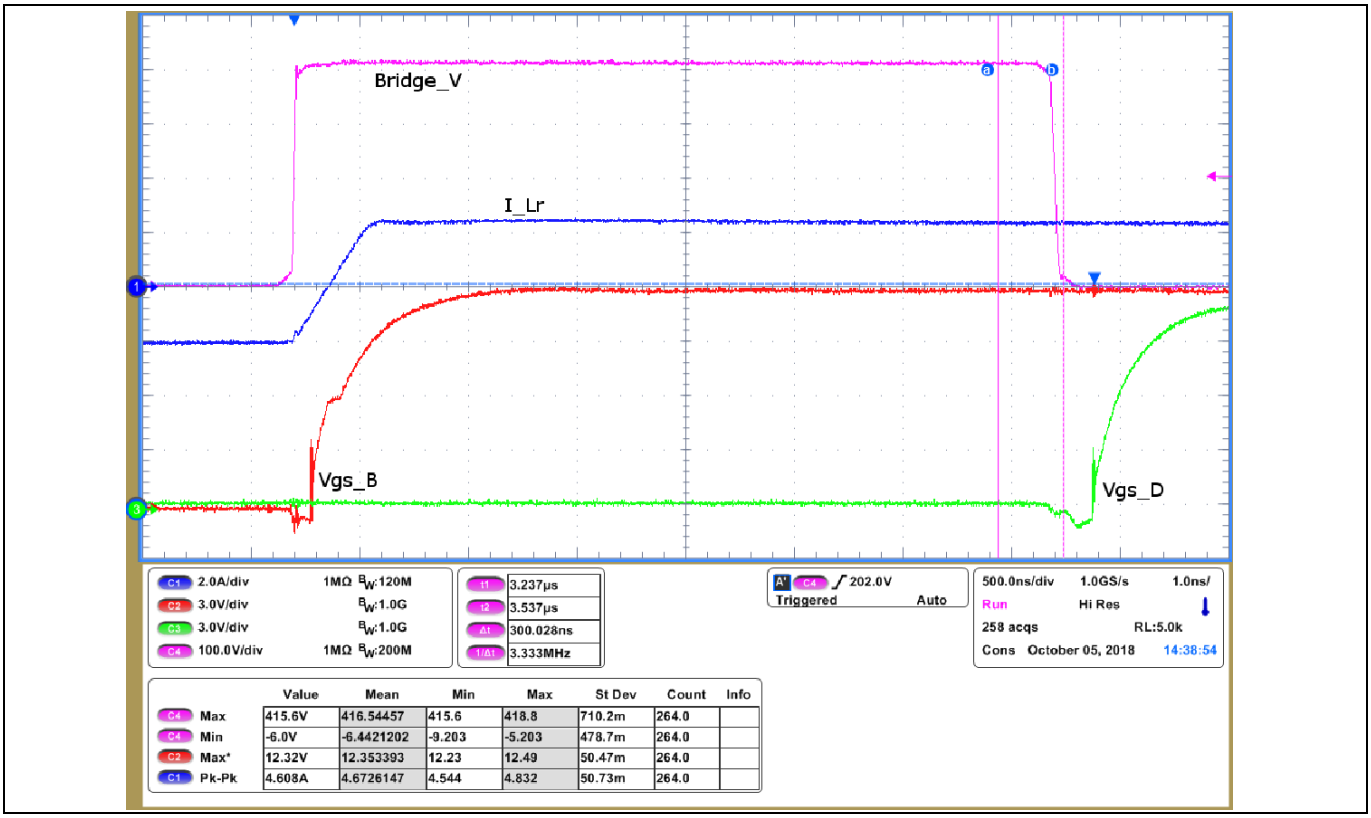

Figure 25 **ZVS turn-on of lagging leg (D switch) and partially hard-switched turn-on of leading leg (B switch) at 15 percent load**

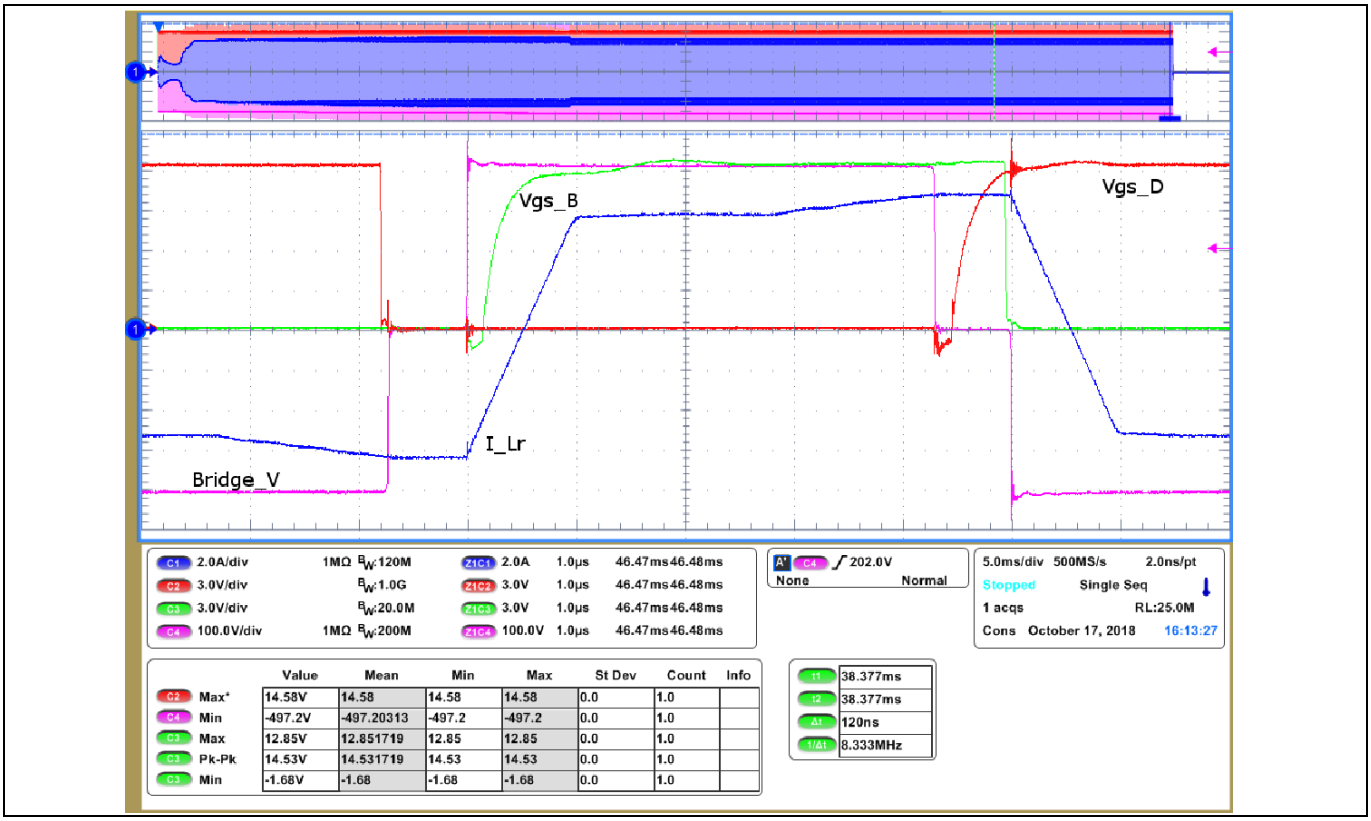

Figure 26 **HV bridge drain voltage overshoot at full load. Note: measured with differential probe Tektronix THDP0200, expected relatively high common mode noise.**

The highest drain voltage overshoot in the HV MOSFETs happens at full load (Figure 26), due to relatively high-current hard-switched turn-off transition; in these transitions the parasitic inductances of the MOSFET package and the layout induce di/dt voltage overshoot.

However, thanks to the low inductances of Infineon's ThinPAK package the overshoot is well under the derated maximum voltage in any operating conditions of the converter (480 V, 80 percent derating of 600 V breakdown voltage of 600 V CoolMOS™ CFD7 at T_j = 25°C).

2.2.2 SRs

The rectifying stage has a full-bridge configuration with eight 1.6 mΩ 60 V OptiMOS™ 5s in a Super SO-8 package. With eight packages the dissipated power can be better spread, bringing higher cooling capability and performance (lower $R_{DS(on)}$ increase due to temperature).

The center-tapped rectifying configuration enables low losses for high output current converters (117 A) but increases the required blocking capability up to two times the reflected transformer secondary voltage (38 V in nominal conditions for this design) plus the additional commutation overshoot.

Nevertheless, thanks to the transformer construction (see 1.4), its low leakage and OptiMOS™ 5 optimized output capacitance it is possible to use 60 V voltage-class devices with more than enough margin for the maximum drain voltage overshoot (e.g. 41.5 V in Figure 27 for an allowed maximum of 48 V, 80 percent derated of 60 V).

The controller provides adaptive turning-on and turning-off points of the SRs along the load for a minimum body diode conduction time in order to reduce conduction losses and reduce generation of reverse recovery charges (Qrr) (meaning there is better efficiency and lower drain voltage overshoot).

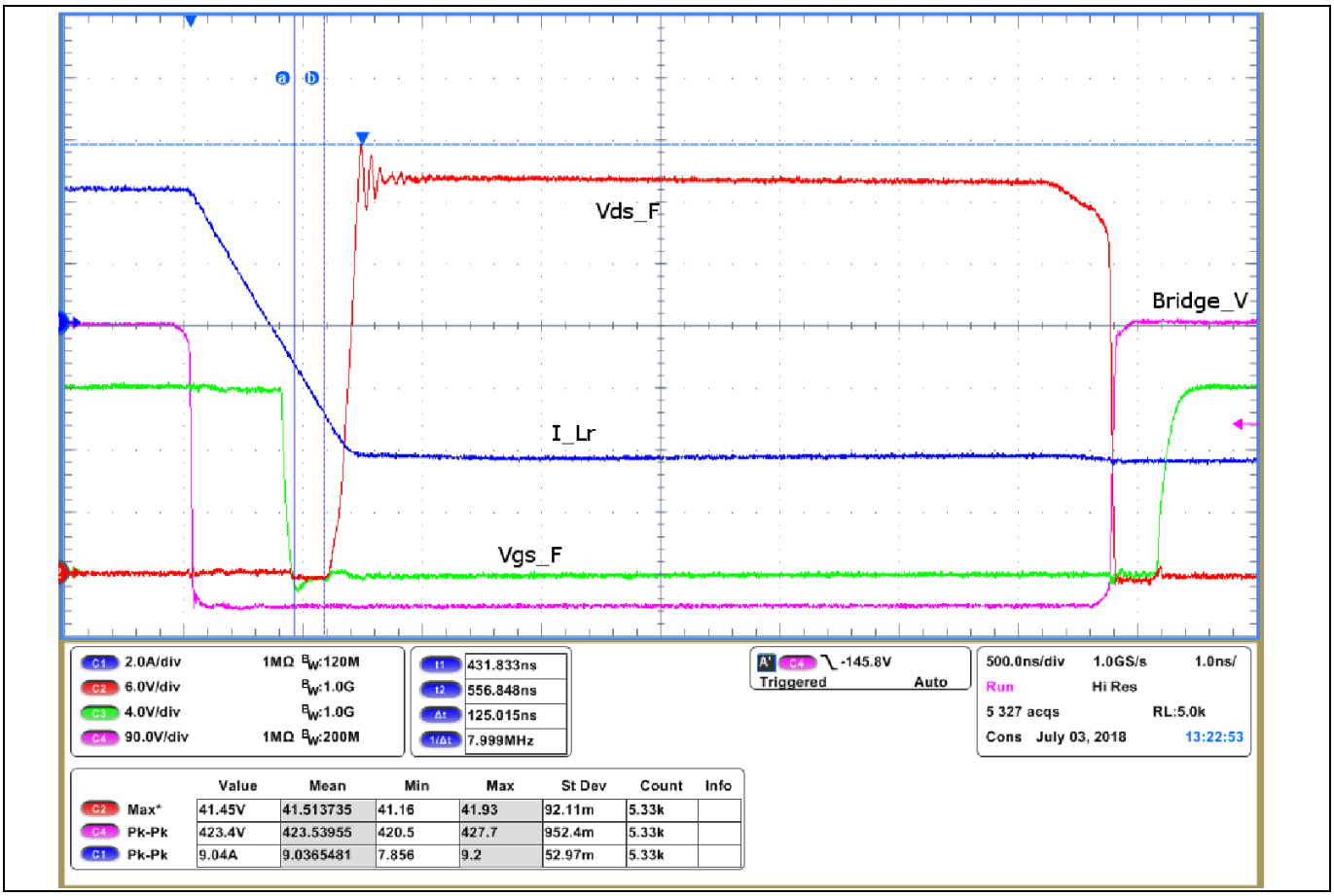

Figure 27 Standard SR driving mode. 80 A load.

2.2.3 Dynamic response

The controller provides hardware-implemented peak current control mode with software-implemented digital compensation designed for a bandwith of 18 kHz with a phase margin of 48 degrees and a gain margin of 12 dB, well within standard stability criteria requirements.

The dynamic response to load jumps (Figure 28) correlates well with the expected response of the designed compensation network, with an overshoot and undershoot within 2.5 percent of the nominal output voltage for a 50 percent load jump.

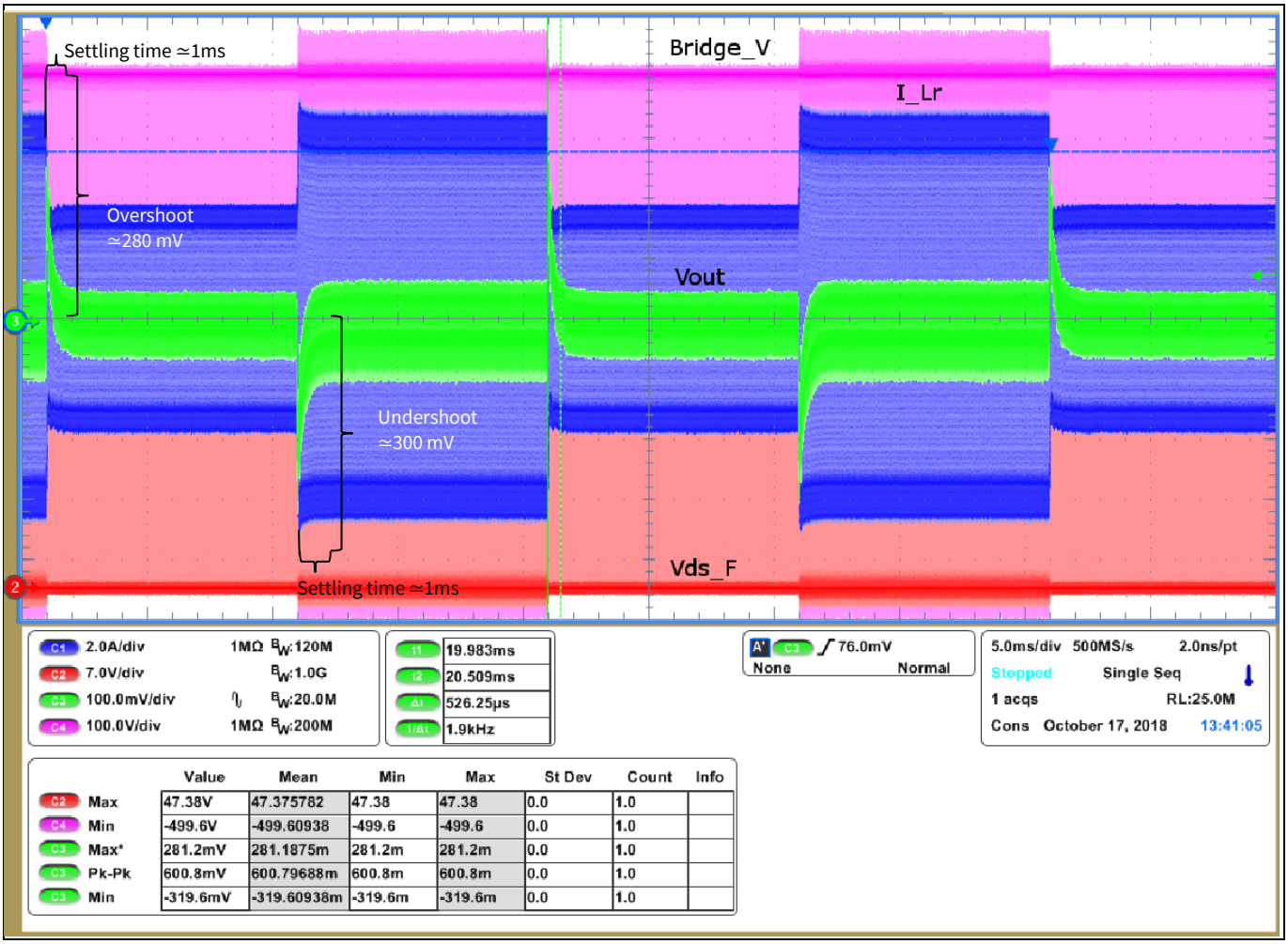

Figure 28 Load-jump, half to full load (60 to 117 A) and full to half load (117 to 60 A). Load jump at 1 A/µs and 10 ms period.

2.2.4 Start-up

The controller implements a soft-start sequence to ensure the converter powers up with minimal stress over any of the components.

In the start-up sequence the output voltage is ramped up in closed-loop operation. The controller increments the output voltage reference within a timed sequence (Figure 29).

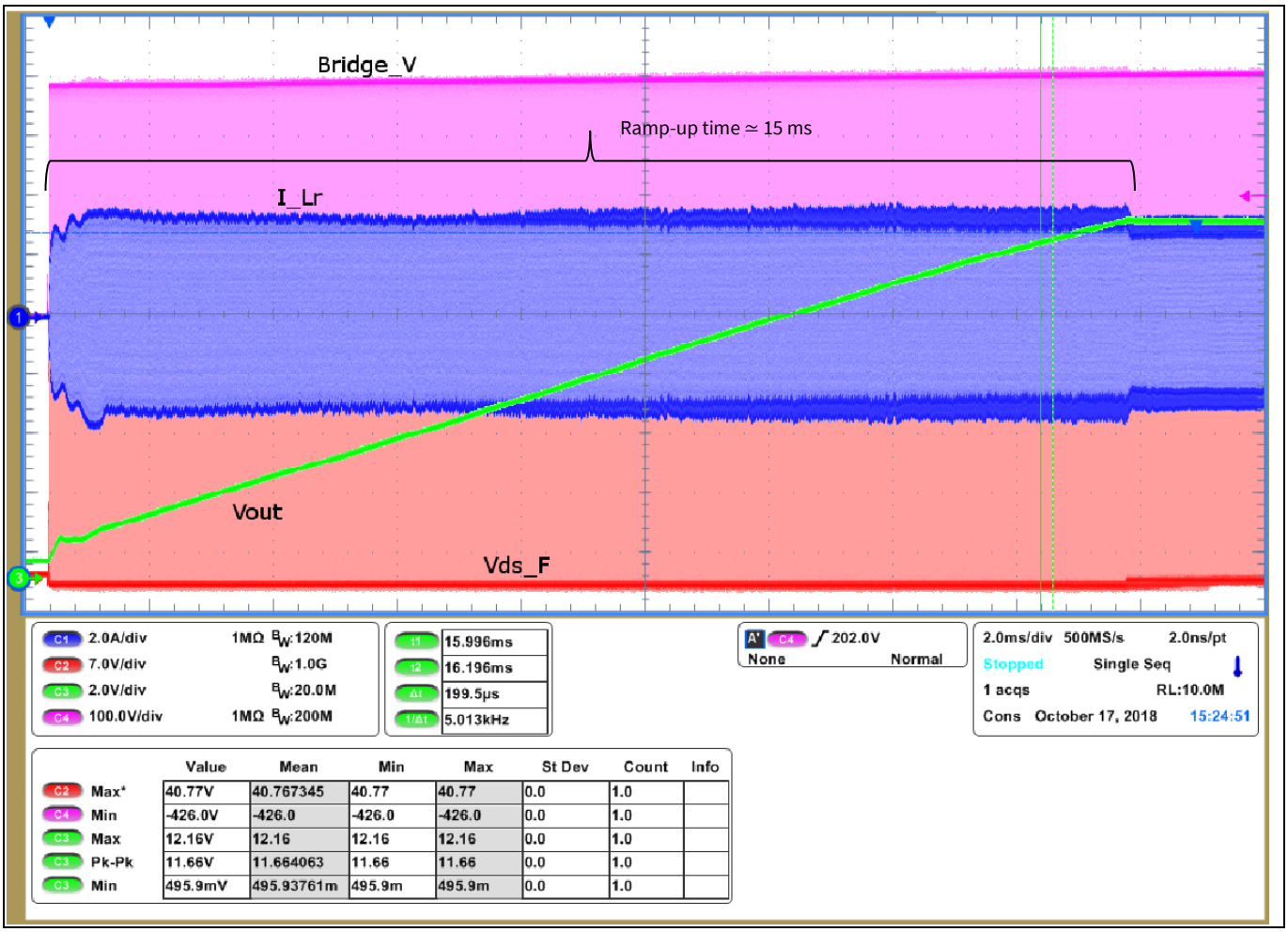

Figure 29 Output voltage soft-start-up

2.2.5 Burst mode operation

For further reduction of power losses under light-load conditions (less than or equal to 3 percent load) the controller implements burst mode operation.

Burst mode ensures that under any condition the HV MOSFETs operate under full or partial ZVS (Figure 30), which reduces the power loss and maintains the smooth QR transitions of the drain voltage (resulting in little or no overshoots and better EMI).

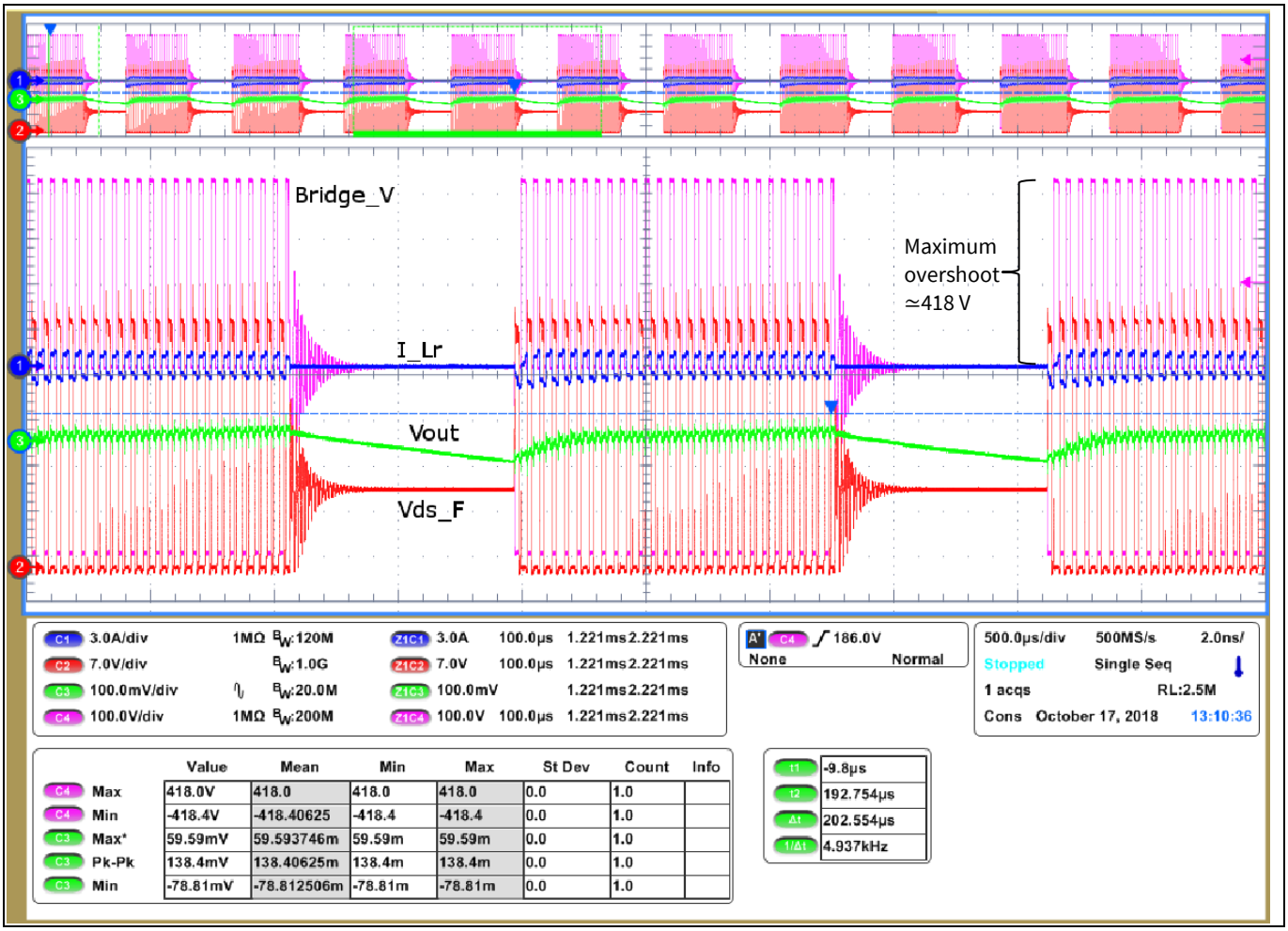

Figure 30 Burst mode operation. Output voltage (green), transformer primary current (blue), bridge voltage (pink), SR drain voltage (red).

2.3 Thermal map

The converter is designed to run enclosed in a cover for the fan to provide enough airflow by the channeling effect. However, the thermal captures in Figure 31 and Figure 32 have been taken with the converter running without enclosure for illustrative purposes (enclosed temperature values would be lower, see 1.5).

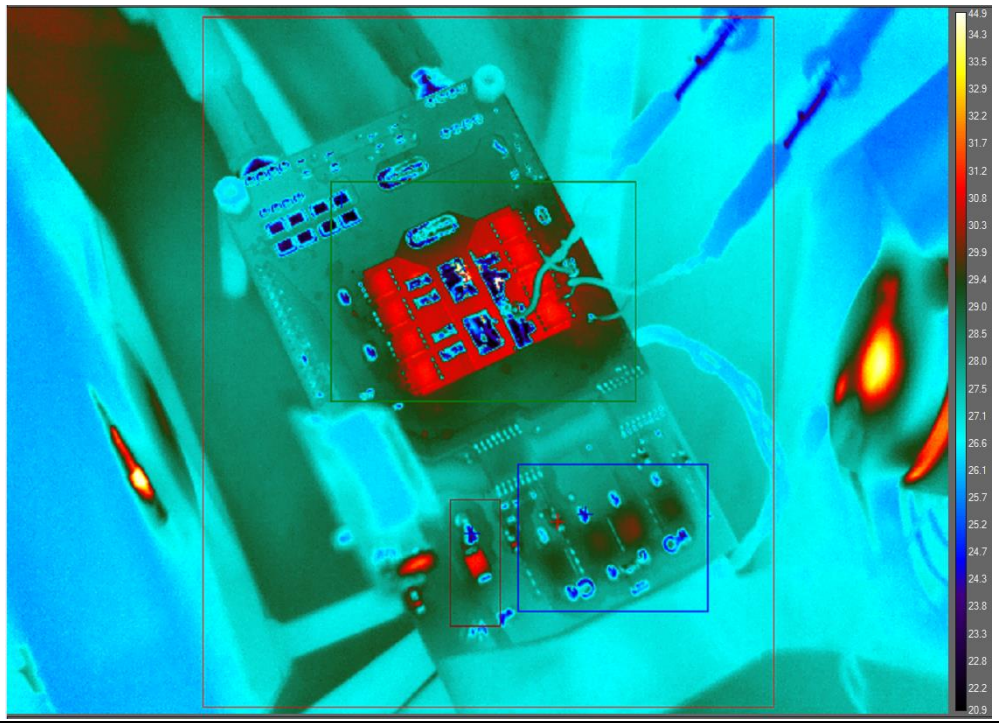

Figure 31 Thermal capture at 15 A load with open case and external supplementary fans. Bottom view.

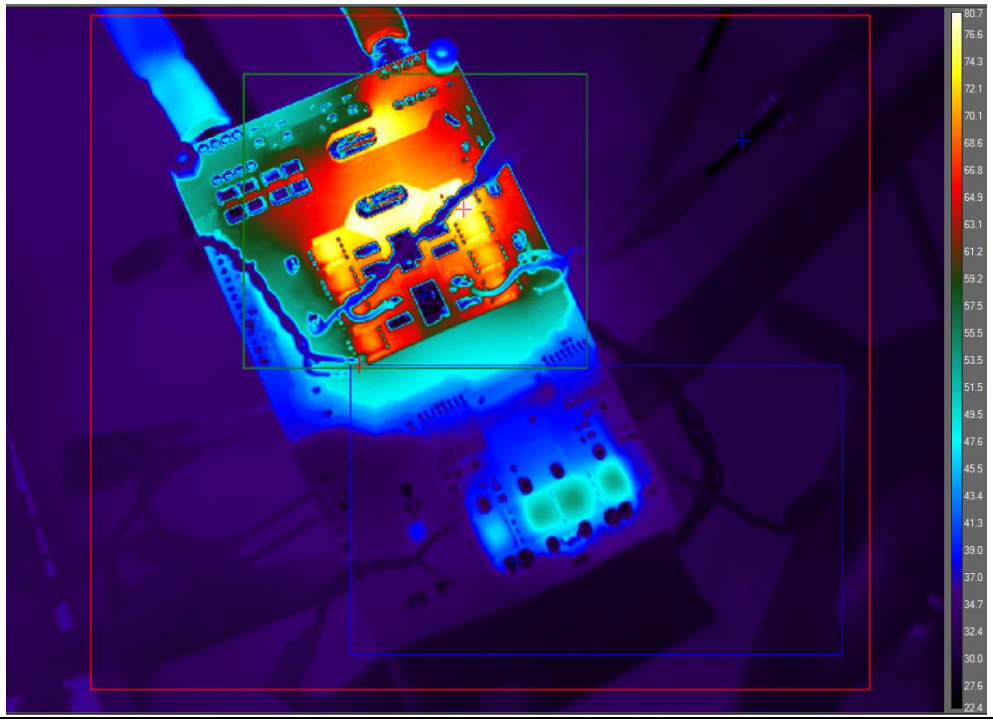

Figure 32 Thermal capture at 117 A load with open case and external supplementary fans. Bottom view.

3 User interface

The controller includes serial communication interface (UART) and a propietary protocol allowing the parametrization of HV and LV MOSFET timings, output voltage settings, protections activation/deactivation and monitoring of status.

The user interface for Windows OS (Figure 33) is an example of the capabilities of the communication library included within the controller. The user interface was specially developed to communicate with the controller through **XMC™ Link** (converts UART to USB), but other serial communication interfaces are also possible.

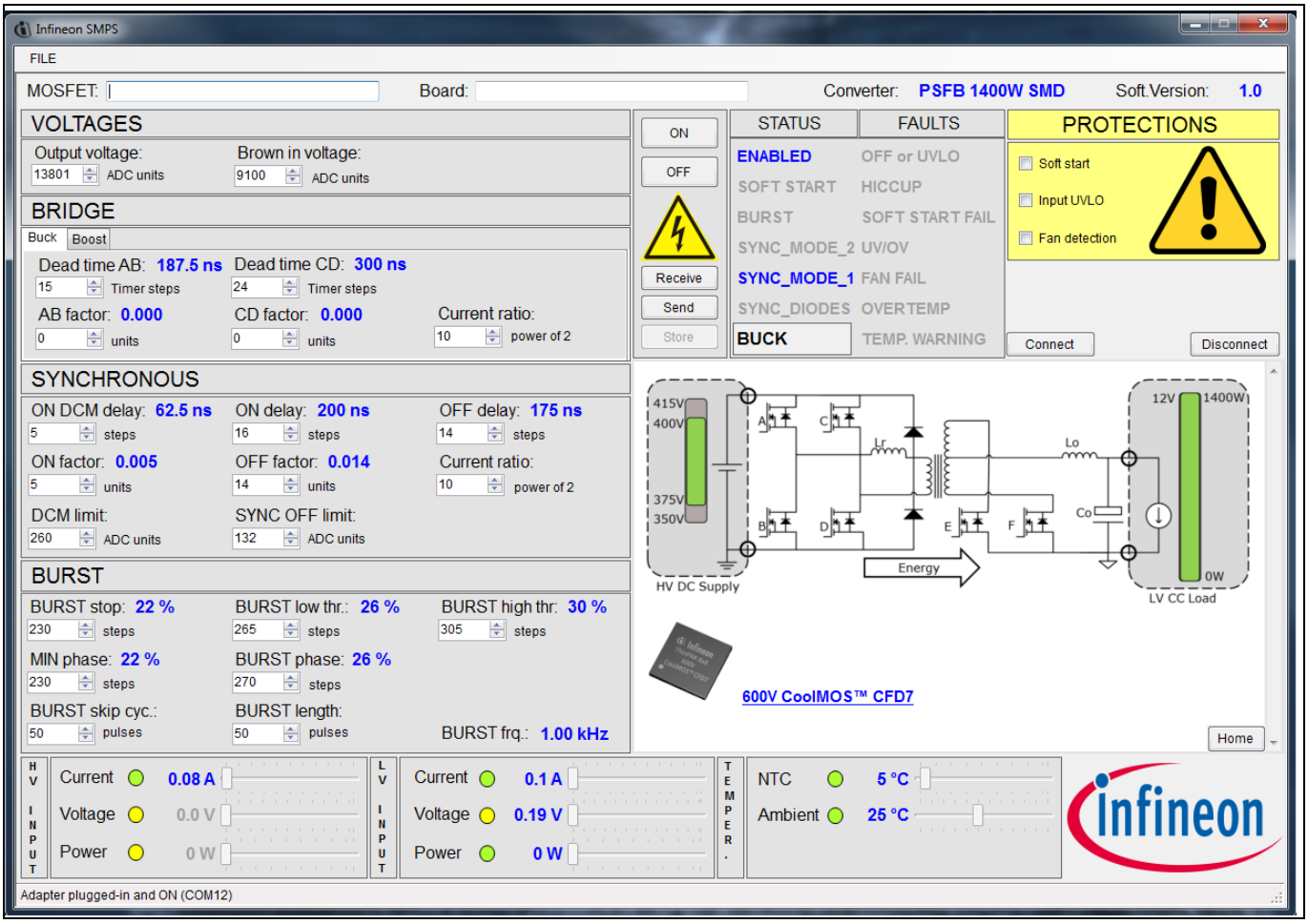

Figure 33 1400 W PSFB SMD advanced user interface

There are two available versions of the GUI:

Advanced user interface with run-time parametrization capabilities of dead-times, voltage and current thresholds, protections and working modes.

Simplified user interface intended for monitoring the converter during run-time (Figure 34).

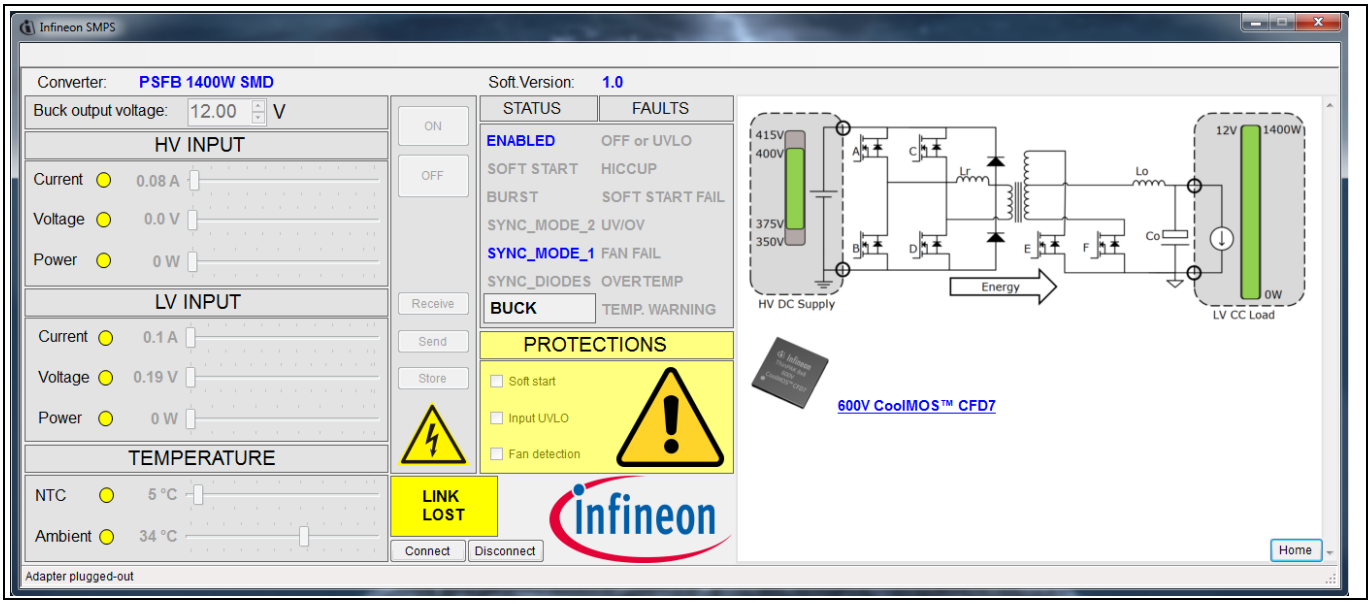

Figure 34 1400 W PSFB SMD simplified user interface

4 Summary

This document introduces a complete Infineon system solution for a 1400 W DC-DC converter from 400 V to 12 V, which achieves 97 percent peak efficiency. The achieved power density is in the range of 3.70 W/cm^3 (60.78 W/in^3), which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution.

Infineon's 600 V CoolMOS™ CFD7 in ThinPAK package, the latest and best-performing fast body diode device from Infineon, combined with a low parasitic package and an optimized layout, achieves incomparable performance with minimum stress on devices, enabled also by the innovative cooling concept presented in this board.

This DC-DC converter proves the feasibility of PSFB topology as a high-efficiency topology at the level of fully resonant topologies when combined with the latest Infineon devices.

This DC-DC converter also proves that digital control, powered by XMC™ Infineon microcontrollers, is not only capable of controlling PSFB topology but can also overcome its drawbacks and enable the use of the latest Infineon devices to achieve the best possible performance.

5 Schematics

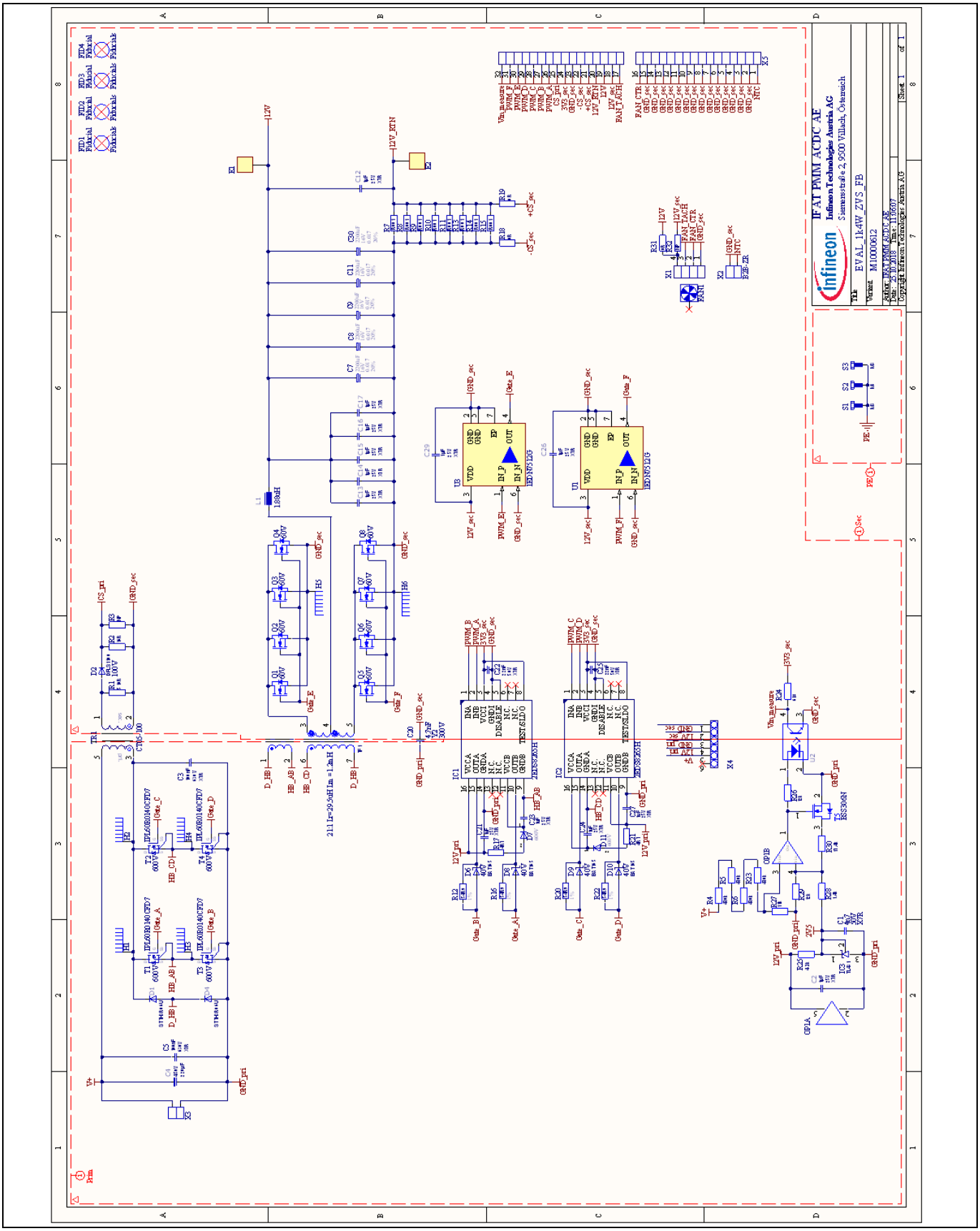

Figure 35 1400 W PSFB SMD main board with IPL60R140CFD7 and BSC016N06NS5

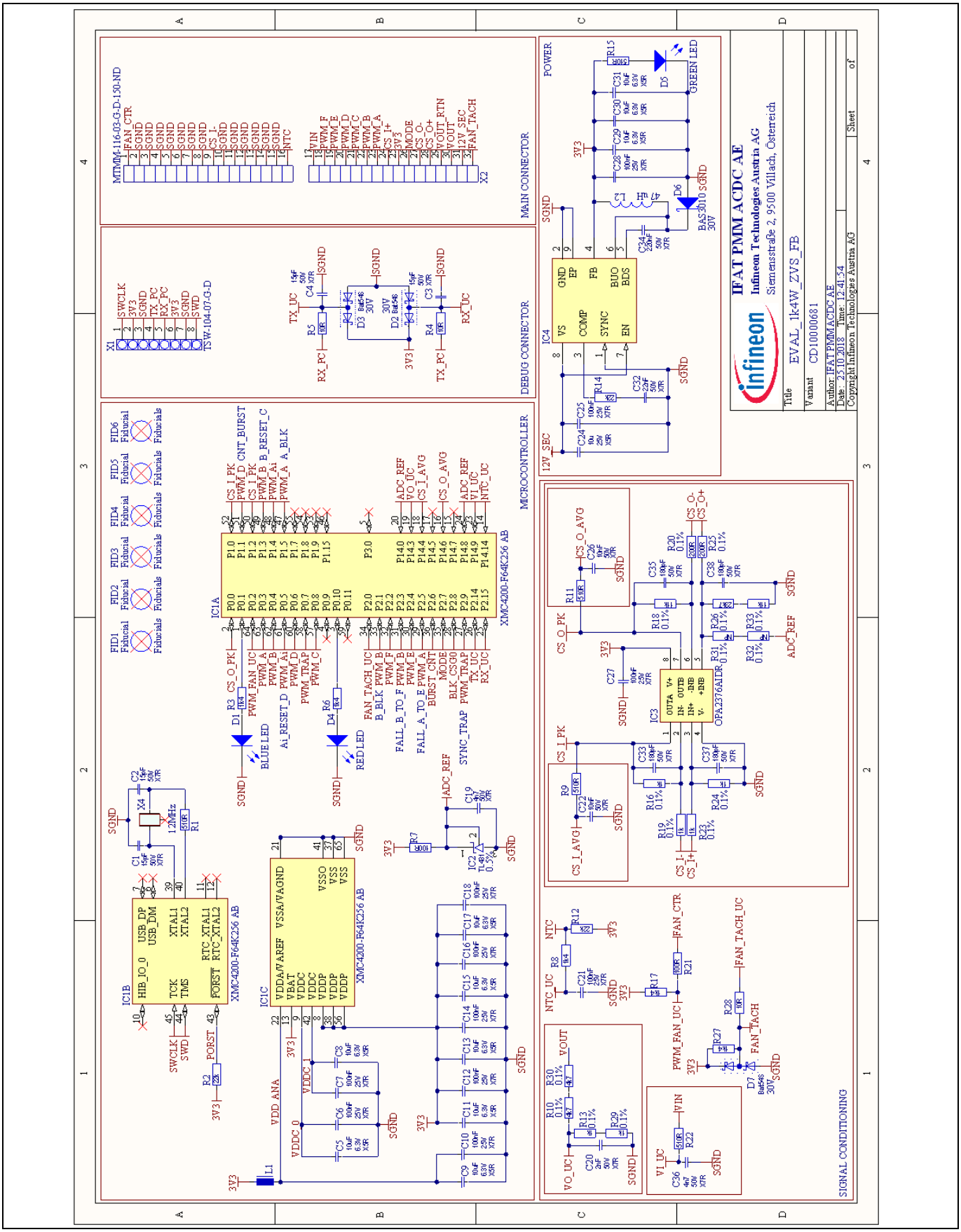

Figure 36 1400 W PSFB SMD controller card with XMC4200-F64K256AB

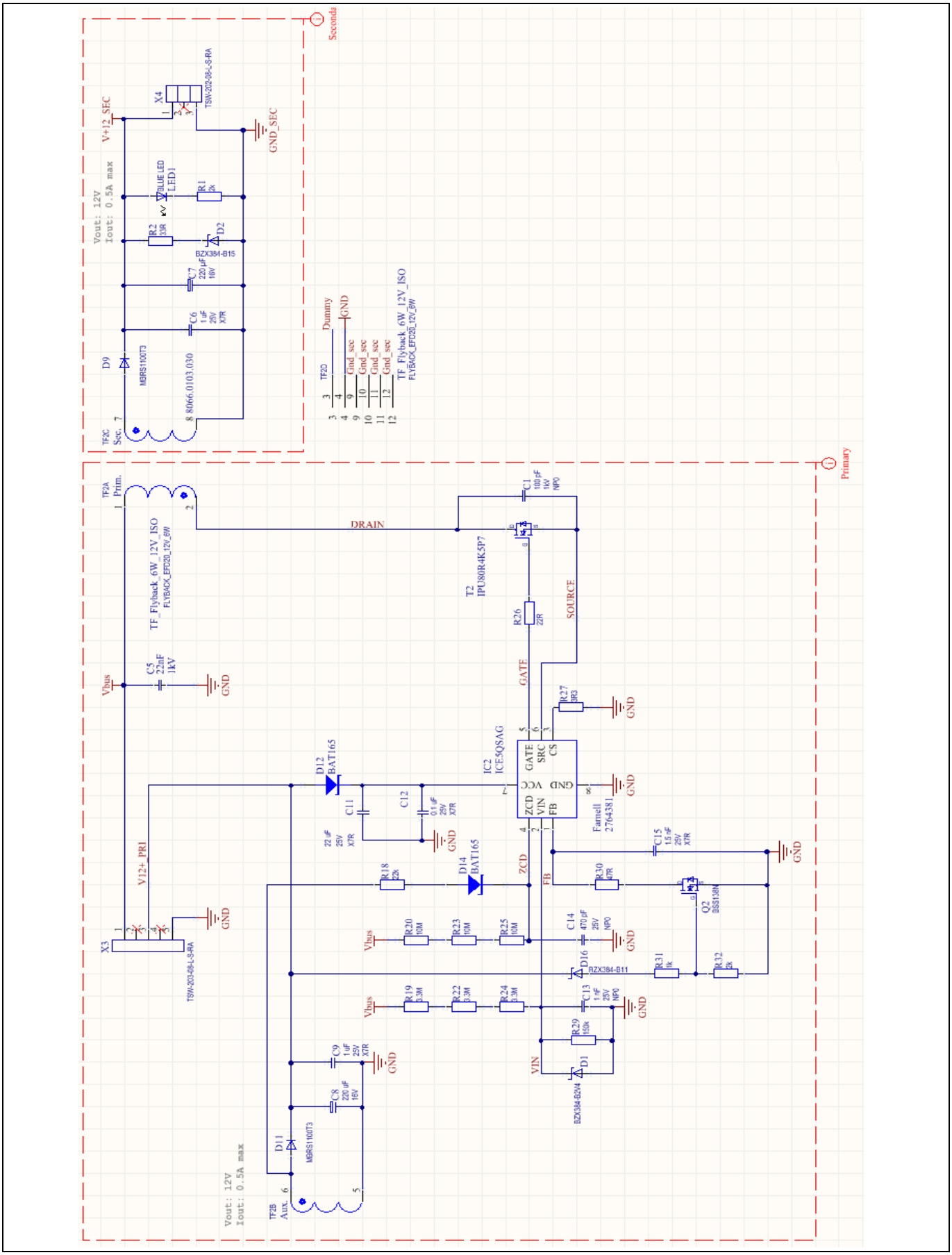

Figure 37 Auxiliary 6 W power supply

6 Bill of Materials (BOM)

Parts designators in bold are produced by Infineon.

Table 2 Main board components

Designator	Value	Tolerance	Voltage	Description	Comment
T1, T2, T3, T4	IPL60R0140CFD7		600 V	CoolMOS™	SMD
U1, U3	1EDN7512G			EiceDRIVER™	SMD
IC1, IC2	2EDS8265H			EiceDRIVER™	SMD
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	BSC016N06NS		60 V	OptiMOS™	SMD
T5	BSS306N		30 V	OptiMOS™	SMD
D6, D8, D9, D10	BAT165		40 V	Schottky diode	SMD
H1, H2, H3, H4, H5, H6	HT10000280			Heatsink	THT
TF1	21:1 Lr = 29.5 µH Lm = 1.2 mH			Transformer	THT
L1	1.88 µH			Inductor	THT
TR1	CT05-100			Transformer	THT
C1	4n7		50 V	Ceramic capacitor	SMD
C2, C26, C29	1 µF		25 V	Ceramic capacitor	SMD
C3, C5	100 nF	X7R	630 V	Ceramic capacitor	SMD
C4	220 µF			Polarized capacitor	THT
C12, C13, C14, C15, C16, C17	1 µF		25 V	Ceramic capacitor	SMD
C20	4.7 nF	Y2	300 V	Ceramic capacitor	THT
C21, C23, C24, C27	1 µF	X7R	25 V	Ceramic capacitor	SMD
C22, C25	22 nF	X7R	50 V	Ceramic capacitor	SMD
D1, D4	STTH3R06U		600 V	Standard diode	SMD
D2	DFLS1100		100 V	Standard diode	SMD
D7, D11	RSFJL		600 V	Diode	SMD
E1, E2	WP-BUCF, M2.5, 6 mm			Redcube press-fit	THT
FAN1	9GA0412P6G001			Fan	
IC3	TL431			TL431	SMD
OP1	TS321			Op-amp	SMD
R1	510R	1 percent		Resistor	SMD
R2	16 R	1 percent		Resistor	SMD
R4, R5, R6, R23	470 k			Resistor	SMD
R7, R8, R9, R10, R11, R13, R14, R15	R001	1 percent		Resistor	SMD
R12, R16, R20, R22	54R9	1 percent		Resistor	SMD
R17, R21	4R7	1 percent		Resistor	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
R18, R19	0 R	1 percent		Resistor	SMD
R24	6k8			Resistor	SMD
R25	4.7 k			Resistor	SMD
R26, R29	12 k			Resistor	SMD
R27	11 k			Resistor	SMD
R28	1.4 k			Resistor	SMD
R30	17.4 k			Resistor	SMD
R31	0 R	1 percent		Resistor	SMD
R32	NP	1 percent		Resistor	SMD
U2	SFH6186-2			Optocoupler	SMD
X1	53398-0471			Connector	SMD
X2	B2B-ZR			Connector	THT
X3	Two-pole connector			Connector	THT
X5	SQW-116-01-L-D			Pin header 2x16 contacts	THT

Table 3 Control board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC1	XMC4200-F64K256 AB			XMC™	SMD
IC4	IFX91041EJ V33			IC buck	SMD
D6	BAS3010		30V	Schottky diode	SMD
D2, D3, D7	Bat54S		30V	Schottky diode	SMD
C1, C2, C3, C4	15 pF	X7R	50V	Ceramic capacitor	SMD
C5, C8, C9, C11, C13, C15, C17, C29, C30, C31	10 µF	X5R	6.3V	Ceramic capacitor	SMD
C6, C7, C10, C12, C14, C16, C18, C21, C25, C27, C28	100 nF	X7R	25V	Ceramic capacitor	SMD
C19, C36	4n7	X7R	50V	Ceramic capacitor	SMD
C20	2 nF	X7R	50V	Ceramic capacitor	SMD
C22, C26	10 nF	X7R	50V	Ceramic capacitor	SMD
C24	10 µF	X5R	25V	Ceramic capacitor	SMD
C32	22 nF	X7R	50V	Ceramic capacitor	SMD
C33, C35, C37, C38	180 pF	X7R	50V	Ceramic capacitor	SMD
C34	220 nF	X7R	50V	Ceramic capacitor	SMD
D1	Blue LED			LED	SMD
D4	Red LED			LED	SMD
D5	Green LED			LED	SMD
IC2	TL431	0.5 percent		Integrated circuit	SMD
IC3	OPA2376AIDR			Integrated circuit	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
L1	Ferrite bead 60 Ω at 100 MHz			Inductor	SMD
L2	47 µH			Inductor	SMD
R1, R9, R11, R15, R22	510 R	1 percent		Resistor	SMD
R2, R12, R14	22 k	1 percent		Resistor	SMD
R3, R6, R8, R17, R27	1k4	1 percent		Resistor	SMD
R4, R5, R28	10 R	1 percent		Resistor	SMD
R7, R21	100 R	1 percent		Resistor	SMD
R10, R30	4k7	0.1 percent		Resistor	SMD
R13, R16, R19, R23, R24, R29	1 k	0.1 percent		Resistor	SMD
R18, R33	11 k	0.1 percent		Resistor	SMD
R20, R25	200 R	0.1 percent		Resistor	SMD
R26	23k7	0.1 percent		Resistor	SMD
R31, R32	NP	0.1 percent		Resistor	SMD
X1	TSW-104-07-G-D			Female header 2 x 4	THT
X2	MTMM-116-03-G-D-150-ND			Pin header 2 x 16	SMD
X4	12 MHz			Crystal oscillator	SMD

7 References

[1] F. Di Domenico, B. Schmoelzer, M. Escudero Rodriguez, S. Raghunath, “800 W ZVS phase shift full bridge evaluation board. Using 600 V CoolMOS™ CFD7 and digital control by XMC4200”, AN_201709_PL52_027, Infineon Technologies, November 2017

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