Final Product Change Notification | 201902005F01

Issue Date: 13-Feb-2019
Effective Date: 14-May-2019

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Management Summary
Applications using the LVDS Display Bridge (LDB) interface Pixel Clock frequencies above 72MHz have experienced display issues.

Change Category

[ ] Wafer Fab Process	[ ] Assembly Process	[ ] Product Marking	[ ] Test Location	[ ] Design
[ ] Wafer Fab Materials	[ ] Assembly Materials	[ ] Mechanical Specification	[ ]Test Process	[ ] Errata
[ ] Wafer Fab Location	[ ] Assembly Location	[ ] Packing/Shipping/Labeling	[ ] Test Equipment	[X] Electrical spec./Test coverage
[ ] Firmware	[ ] Other			

iMX6 DualPlus / QuadPlus Data Sheet Revision Update

Description of Change

The Commercial, Industrial, and Automotive version of the iMX6 DualPlus / QuadPlus data sheets will be updated to revision Rev. 4, 02/2019 with the below specification changes:

Section: 1.2 Features
- LVDS serial ports - Two ports with a maximum Pixel Clock up to 72 Mpixels/sec for both.

Table 67. LVDS Display Bridge (LDB) Electrical Specification
Added Row: Max Pixel Clock - 72 MHz

Please use the below link once Rev. 4, 02/2019 has been approved. Rev 4, 02/2019 documents are attached to this PCN.
https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors:IMX6X_SERIES

Corresponding ZVEI Delta Qualification Matrix ID SEM-DS-01

Reason for Change

- Applications using the LVDS Display Bridge (LDB) interface Pixel Clock at frequencies above 72HMz may experience display issues.
- Initial failures are either Black Display (no Pixel Clock Output) or Distorted Display (Unstable Pixel Clock Frequency). Worst case operation occurs at high temperature.
- Current data sheets (Rev. 3, 2018) do not show an FMAX specification for the Pixel Clock.

Identification of Affected Products

Product identification does not change

Product Availability

Sample Information

Not applicable

Production

Planned first shipment 13-Feb-2019

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Data Sheet Revision

A new datasheet will be issued

Disposition of Old Products

If the application is using an LDB frequency >72MHz, contact your NXP Representative.

Timing and Logistics

In compliance with JEDEC J-STD-046, your acknowledgement of this change is expected by 15-Mar-2019.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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Customer Focus, Passion to Win.

NXP Quality Management Team.

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NXP Semiconductors
High Tech Campus, 5656 AG Eindhoven, The Netherlands

Changed Orderable Part#	Changed Part 12NC
MCIMX6QP4AVT8AA	935312724557
MCIMX6DP6AVT8AB	935357862557
MCIMX6QP7CVT8AA	935312744557
MCIMX6DP6AVT8AA	935312751557
MCIMX6DP7CVT8AA	935315902557
MCIMX6QP5EYM1AA	935316001557
MCIMX6DP5EYM1AA	935316005557
MCIMX6DP6AVT1AA	935316031557
MCIMX6QP6AVT1AA	935318871557
MCIMX6DP4AVT8AA	935322521557
MCIMX6QP4AVT1AA	935324954557
MCIMX6DP4AVT1AA	935325982557
MCIMX6QP6AVT8AA	935325995557
MCIMX6QP6AVT1AB	935352721557
MCIMX6DP7CVT8AB	935356639557
MCIMX6QP7CVT8AB	935356641557
MCIMX6DP5EYM1AB	935357835557
MCIMX6QP5EYM1AB	935357836557
MCIMX6DP4AVT1AB	935357856557
MCIMX6DP4AVT8AB	935357858557
MCIMX6DP6AVT1AB	935357861557