CDB43L21

Evaluation Board for the CS43L21

Features

- MUX'd Analog Output
  - Stereo RCA Output (w/Optional Load or LPF)
  - Stereo Headphone Jack
  - Mono Speaker Driver w/Banana Posts
- 8 kHz to 96 kHz S/PDIF Interface
  - CS8415 Digital Audio Receiver
- I/O Stake Headers
  - External Control Port Accessibility
  - External DSP Serial Audio I/O Accessibility
- Independent, Regulated Supplies
- 1.8 V to 3.3 V Logic Interface
- Hardware Control
  - 11 Pre-Defined Switch Settings
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User-Configurable Scripts
- Layout and Grounding Recommendations

Description

The CDB43L21 evaluation board is an excellent means for evaluating the CS43L21 DAC. Evaluation requires a digital signal source, analog analyzer, and power supplies. Optionally, a Windows PC-compatible computer may be used to evaluate the CS43L21 in Software Mode.

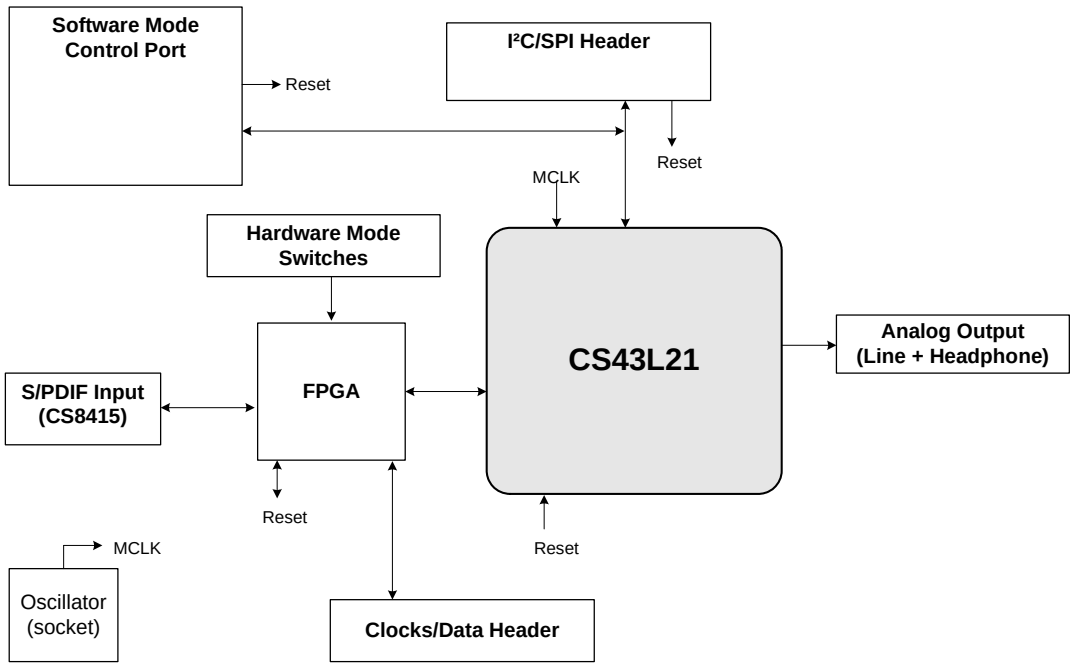
System timing can be provided by the CS8415, by the CS43L21 with supplied master clock, or by an I/O stake header with a DSP connected.

RCA phono jacks are provided for the CS43L21 analog outputs. 1/8th inch jacks are also available for headphone output. Digital data input is available via RCA phono or optical connectors to the CS8415.

The Windows software provides a Graphical User Interface (GUI) to make configuration of the CDB43L21 easy. The software communicates through the PC's serial port/USB to configure the control port registers so that all the features of the CS43L21 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB43L21	Evaluation Board



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1. SYSTEM OVERVIEW

The CDB43L21 evaluation board is an excellent means for evaluating the CS43L21. Digital audio signal interfaces are provided, and an FPGA is used for easily configuring the board. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

The CDB43L21 schematic set has been partitioned into six pages and is shown in Figures 10 through 15. “System Connections” on page 14 provides a description of all stake headers and connectors, including the default factory settings for all jumpers.

1.1 Power

Power is supplied to the evaluation board through the +5.0 V binding posts. Jumpers connect the CS43L21’s power supplies to a regulated voltage of +1.8 V, 2.5 V or +3.3 V for VL and +1.8 V or 2.5 V for VD, VA and VA_HP. All voltage inputs must be referenced to the black binding post ground connector.

For current measurement purposes only, a series resistor is connected to each supply. The current is easily calculated by measuring the voltage drop across this resistor.

NOTE: The stake headers connected in parallel with these resistors must be shunted with the supplied jumper during normal operation.

WARNING: Please refer to the CS43L21 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS43L21 requires careful attention to power supply and grounding arrangements to optimize performance. The CDB43L21 demonstrates these optimal arrangements. Figure 9 on page 15 provides an overview of the connections to the CS43L21. Figure 16 on page 22 shows the component placement, Figure 17 on page 23 shows the top layout, and Figure 18 on page 24 shows the bottom layout. The decoupling capacitors are located as close to the CS43L21 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 FPGA

The FPGA provides digital signal routing between the CS43L21, CS8415 and the I/O stake header. It also configures the Hardware Mode options of the CS8415 and provides routing control of the system master clock from an on-board oscillator, the CS8415 and the I/O stake header. The Cirrus FlexGUI software and “FPGA H/W Control” switches provide full control of the FPGA’s routing and configuration options. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

1.4 CS43L21

A complete description of the CS43L21 is included in the CS43L21 product data sheet, and a schematic is provided in Figure 10 on page 16.

The CS43L21 may be configured using either the Cirrus FlexGUI or the on-board “CS43L21 H/W Control” switches. The Software Mode control port registers are accessible through the “Register Maps” tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. The Hardware Mode, stand-alone controls for the CS43L21 are accessible through the on-board, stand-alone switches, “CS43L21 H/W Control.”

Clock and data source selections are made in the control port of the FPGA, accessible through the “General Configurations” tab of the Cirrus FlexGUI software or through the on-board “FPGA H/W Control” switches.

Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

1.5 CS8415 Digital Audio Receiver

A complete description of the CS8415 receiver (Figure 12 on page 18) and a discussion of the digital audio interface are included in the CS8415 data sheet.

The CS8415 converts the input S/PDIF data stream from either the optical or the RCA connector into PCM data for the CS43L21. The CS8415 operates in master or slave mode, generates a 256xFs master clock, and can operate in either the Left-Justified or I²S interface format.

Selections are made in the control port of the FPGA, accessible through the “General Configurations” tab of the Cirrus FlexGUI software or through the on-board “FPGA H/W Control” switches. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

1.6 Oscillator

The on-board oscillator provides one of the system master clocks. Selections are made in the control port of the FPGA, accessible through the “General Configurations” tab of the Cirrus FlexGUI software or through the on-board switches, “FPGA H/W Control.” Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. Additional sockets are also installed, allowing the optional use of a half-can- or full-can-sized oscillator.

1.7 I/O Stake Headers

The evaluation board has been designed to allow interfacing with external systems via a serial port header (reference designation J5) and a control port header, “CS43L21 S/W Control.” The serial port header provides access to the serial audio signals required to interface with a DSP (Figure 13 on page 19). Selections are made in the control port of the FPGA, accessible through the “General Configurations” tab of the Cirrus FlexGUI software or through the on-board “FPGA H/W Control” switches. Section 2. “Software Mode Control” on page 7 and Section 3. “Hardware Mode Control” on page 11 provide configuration details.

The control port header provides bidirectional access to the SPI™/I²C® control port signals by simply removing all the shunt jumpers from the “PC” position. The user may then choose to connect a ribbon cable to the “CONTROL” position, allowing operation of the CS43L21 in a user-application for system development. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I²C power rail.

1.8 Analog Outputs

RCA connectors are connected directly to the output of the CS43L21 to allow evaluation of the ground-centered analog outputs. The Right Channel and Left Channel stake headers optionally connect a passive-filtered output to the RCA connectors. For evaluation of the CS43L21’s drive strength into a load, the 16 W HP Load stake headers connect the analog outputs to 16 W. Headphones may also be connected to the 1/8th inch jack. When connecting headphones, the 16 Ω load resistors should be disconnected by removing the jumpers on each stake header.

One of the analog outputs may be connected to a speaker driver through the “Speaker” stake header. A mono speaker may then be driven via the red and black banana jack. The red banana jack designates the positive terminal and the black designates the negative.

1.9 Stand-Alone Switches

The “FPGA H/W Control” and “CS43L21 H/W Control” switches control all Hardware Mode options. Section 3. “Hardware Mode Control” on page 11 provides a description of each topology.

1.10 Control Port Connectors

A graphical user interface is available for the CDB43L21, allowing easy manipulation of each register. This GUI interfaces with the CDB via the RS-232 connector and controls all Software Mode options. Section 2. “Software Mode Control” on page 7 provides a description of the GUI.

1.10.1 USB Connector

Connecting a USB port cable from a PC to the USB connector and launching the Cirrus FlexGUI software enables one to use the CDB43L21.

1.10.2 RS-232 Connector

Connecting a cable to the RS-232 connector and launching the Cirrus FlexGUI software enables the CDB43L21 in Software Mode.

2. SOFTWARE MODE CONTROL

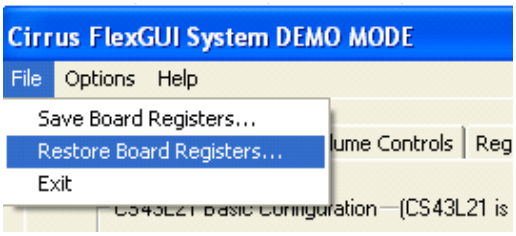
The CDB43L21 may be used with the Microsoft® Windows-based FlexGUI graphical user interface, allowing software control of the CS43L21 and FPGA registers. The latest control software may be downloaded from **www.cirrus.com/msasoftware**. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software according to the instructions provided on the Website.
2. Connect and apply power to the +5.0 V binding post.
3. Connect the CDB to the host PC using either a 9-pin serial or USB cable.
4. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
5. Enable the CS43L21 by engaging the “Enable CS43L21” push-button.
6. Refresh the GUI by clicking on the “Update” button. *The default state of all registers are now visible.*
7. Engage and then disengage the “Power Down” push-button in the “General Configurations” group. *This performs the necessary write sequence to the* CS43L21 *for Software Mode operation.*

For standard setup:

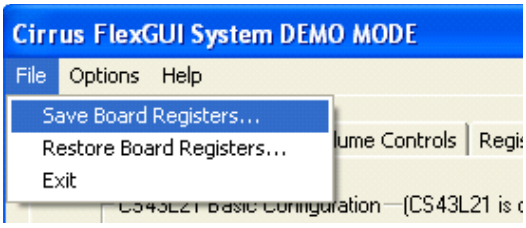
8. Set up the signal routing in the “General Configurations” tab as desired.
9. Set up the CS43L21 in the “General Configurations” and “DAC Volume Controls” tab as desired.
10. Begin evaluating the CS43L21.

For quick setup, the CDB43L21 may be configured by loading a predefined sample script file:



11. On the File menu, click "Restore Board Registers..."
12. Browse to Boards\CDB43L21\Scripts\.
13. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:



14. On the File menu, click "Save Board Registers..."
15. Enter any name that sufficiently describes the created setup.
16. Choose the desired location and save the script.
17. To load this script, follow the instructions from step 11 above.

2.1 General Configuration Tab

The “General Configuration” tab provides high-level control of signal routing on the CDB43L21. This tab also includes basic controls for the CS43L21 for quickly setting up the CDB43L21 in simple configurations. Status text detailing the CS43L21’s specific configuration is shown in parenthesis or appears directly below the associated control. This text may change depending on the setting of the associated control. A description of each control group is outlined below:

CS43L21 Basic Configuration - Includes basic register controls in the CS43L21 used for setting up power status, interface format and clocking functions. See Section 2.2 and Section 2.3 for more controls in the CS43L21.

S/PDIF Receiver Control - Includes all available Hardware Mode controls for setting up the CS8415.

Clock/Data Routing and CS43L21 Reset - Includes controls used for routing clocks and data between the CS43L21, CS8415, oscillator and the I/O stake header. Also includes a reset control for the CS43L21.

Update - Reads all registers in the FPGA and CS43L21 and reflects the current values in the GUI.

Reset - Resets FPGA to default routing configuration.

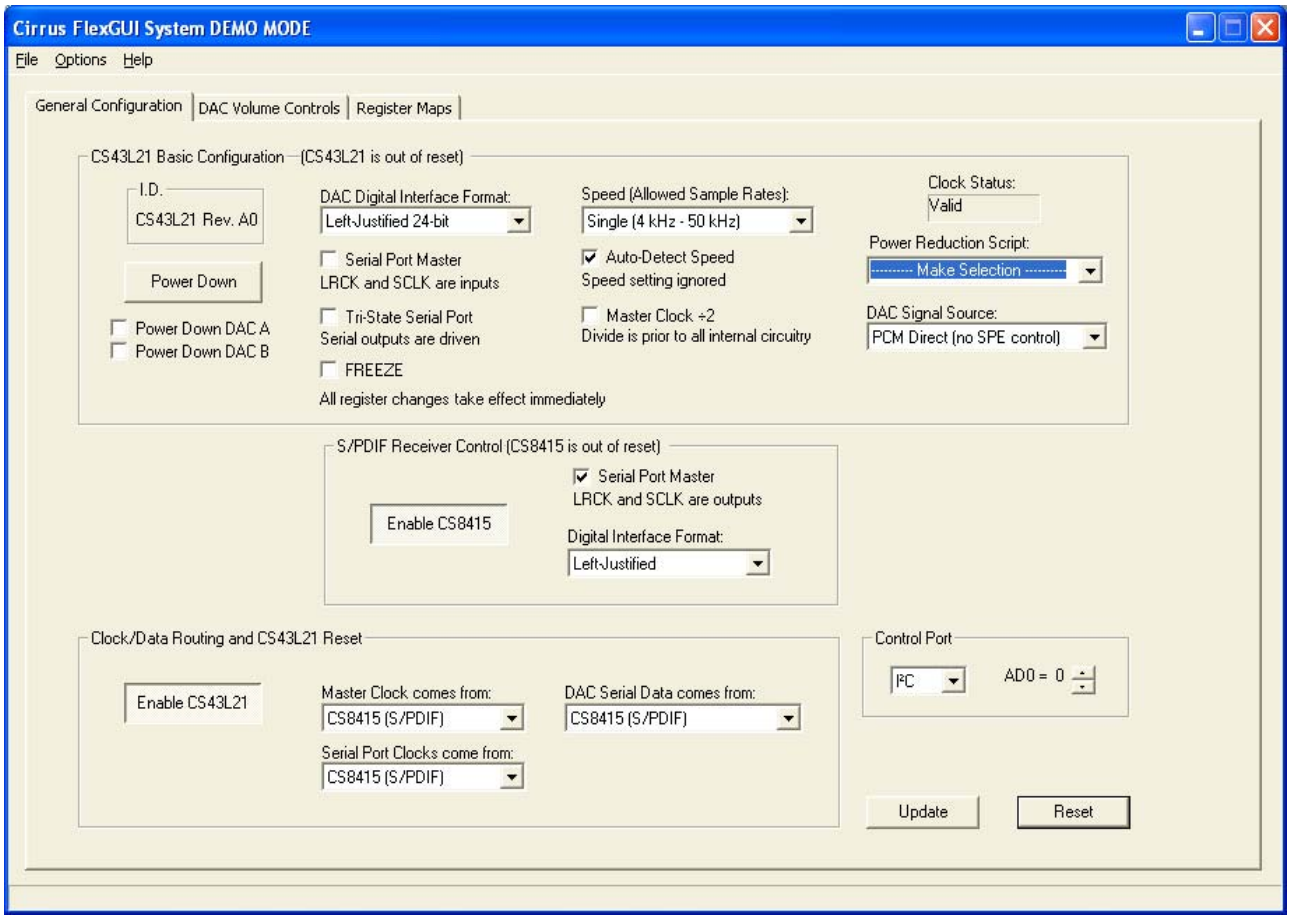


Figure 1. General Configuration Tab

2.2 DAC Volume Controls Tab

The “DAC Volume Controls” tab provides high-level control of all volume settings in the CS43L21. Status text detailing the CS43L21’s specific configuration is shown in read-only edit boxes, in parenthesis, or it appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS43L21 data sheet):

Digital Volume Control - Includes all digital volume controls and adjustments for the DAC.

Analog Multipliers - Includes the control for the analog gain of the output amplifier and displays the full-scale output factors.

Limiter Configuration - Includes all configuration settings for the Limiter.

Tone Control - Includes all bass and treble boosting controls and adjustments.

BEEP Generator - Includes all configuration settings for the BEEP generator.

Update - Reads all registers in the CS43L21 and reflects the current values in the GUI.

Reset - Resets the CS43L21.

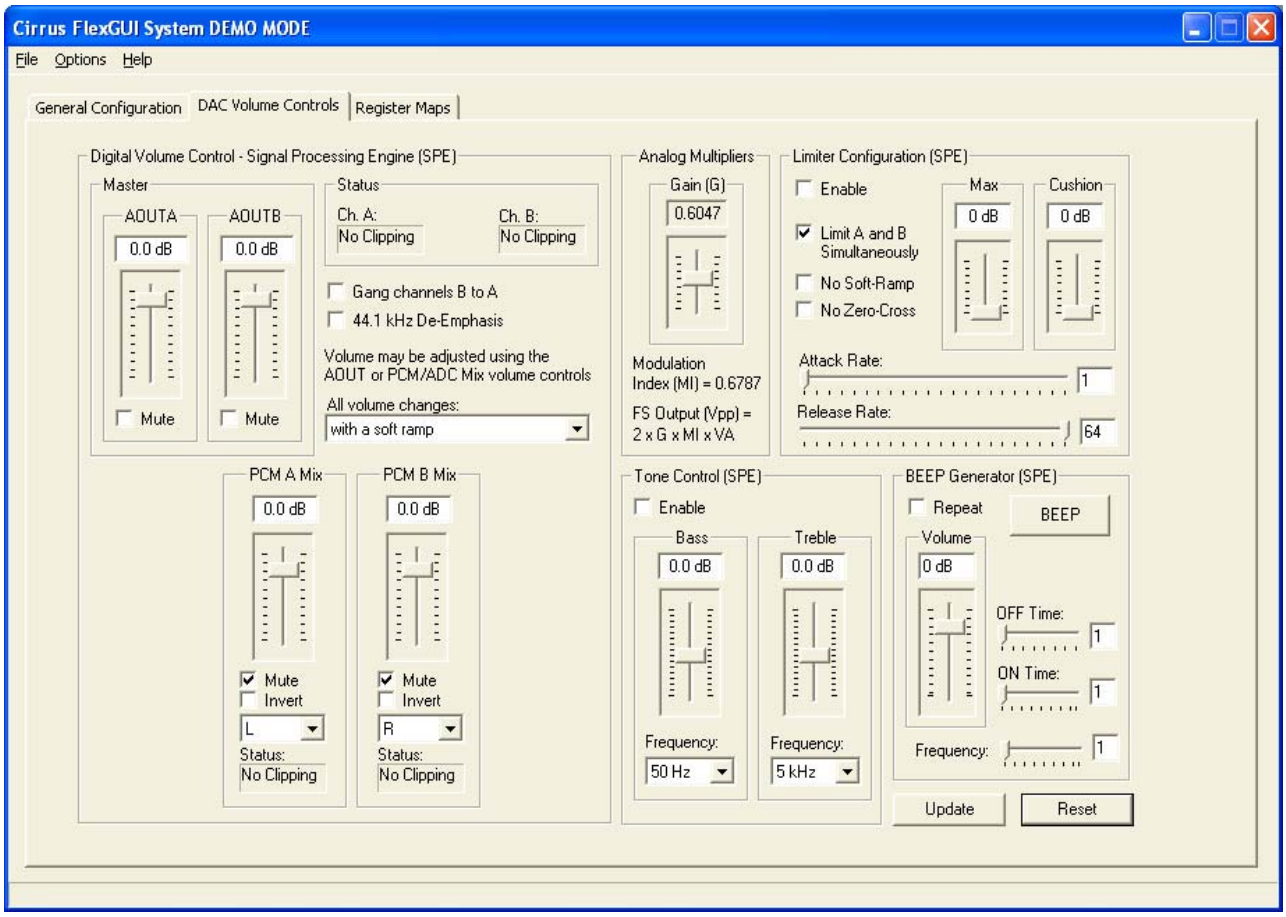


Figure 2. DAC Volume Controls Tab

2.3 Register Maps Tab

The Advanced Register Debug tab provides low-level control of the CS43L21 individual register settings. Register values can be modified bit-wise or byte-wise. For bit-wise, click the appropriate push-button for the desired bit. For byte-wise, the desired hex value can be typed directly into the register address box in the register map. The “FPGA” and “GPIO” tabs may be ignored.

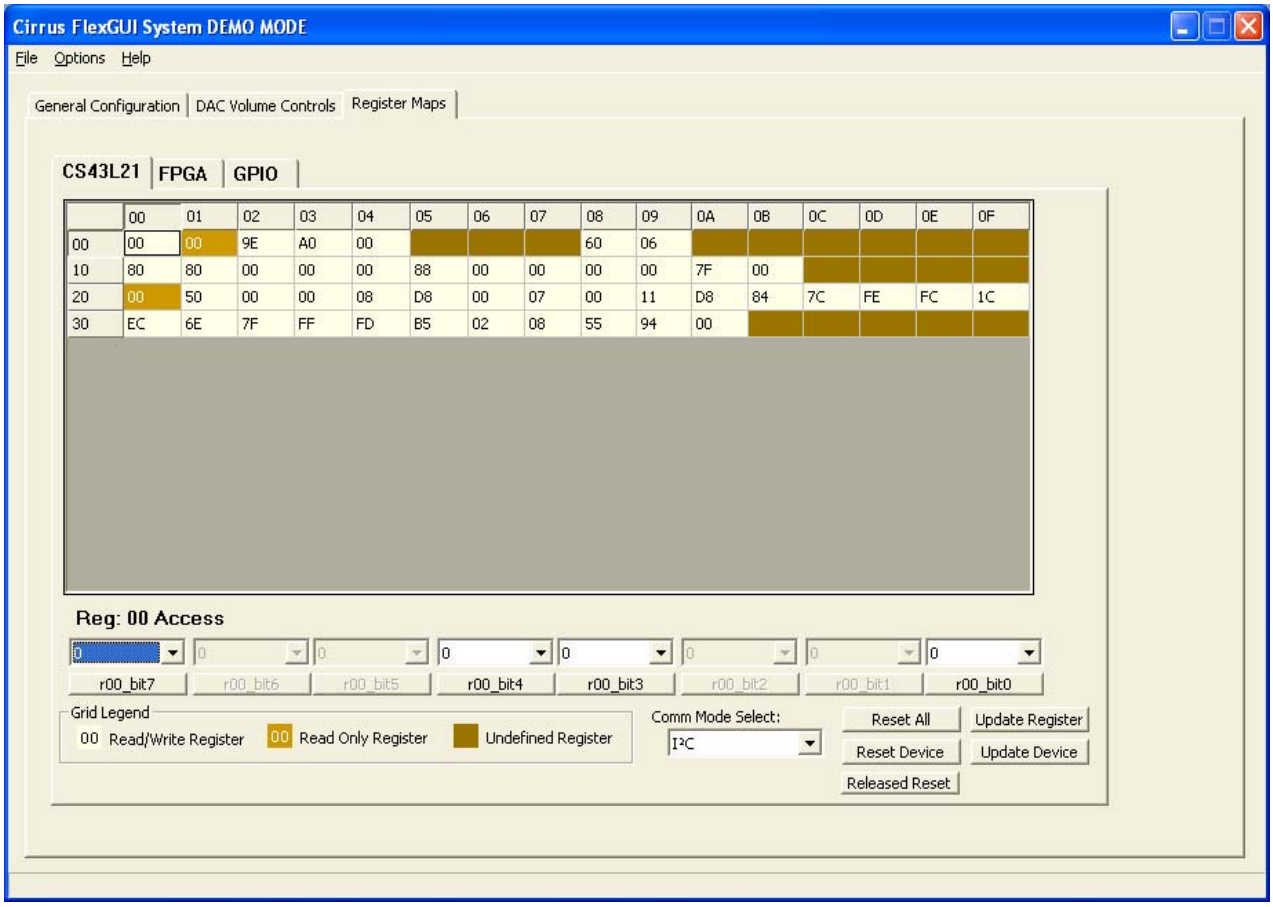


Figure 3. Register Maps Tab - CS43L21

3. HARDWARE MODE CONTROL

The CDB may be configured without the use of a software control port through the use of two switches, “FPGA H/W Control” and “CS43L21 H/W Control.” These switches are enabled in Hardware Mode only and ignored in Software Mode. The CDB43L21 automatically enters Hardware Mode upon initial power up, when exiting Software Mode, upon termination of the Cirrus FlexGUI software, or by disconnecting the RS-232 serial cable.

3.1 FPGA H/W Control

The “FPGA H/W Control” switch sets up the CDB in 11 pre-defined routing topologies in Hardware Mode. The tables and figures below describe each switch setting. The At-A-Glance Controls table provides a quick reference for all presets.

At-A-Glance Controls		
S[3:2]	**S[1]**	**S[0]**
00 - CS8415 MCLK / CS8415 clocks/data route through FPGA **01** - I/O Header MCLK / I/O Header clocks/data route through FPGA **10** - Oscillator MCLK / I/O Header clocks/data route through FPGA **11** - Reserved	**0** - CS43L21 Slave Routing **1** - CS43L21 Master Routing	**0** - Normal Operation **1** - Reserved

Signal Routing	S[3:0]	General Description	Detailed Description
CS8415 MCLK			
1 Figure 4	0000	CS8415 Clocks/Data	1) CS8415 masters MCLK. 2) CS8415 masters PCM clocks. 3) CS8415 data into SDIN.
I/O MCLK			
2 Figure 5	0100	I/O Clocks/Data	1) I/O masters MCLK. 2) I/O masters PCM clocks. 3) I/O data into SDIN.
3 Figure 6	0110	CS43L21 Clocks, I/O Data	1) I/O masters MCLK. 2) CS43L21 masters PCM clocks. 3) I/O data into SDIN.
Oscillator MCLK			
4 Figure 7	1000	I/O Clocks/Data	1) Oscillator masters MCLK. 2) I/O masters PCM clocks. 3) I/O data into SDIN.
5 Figure 8	1010	CS43L21 Clocks, I/O Data	1) Oscillator masters MCLK. 2) CS43L21 masters PCM clocks. 3) I/O data into SDIN.

Table 1. MCLK and Clock/Data Routing Options

3.2 CS43L21 H/W Control

The stand-alone “CS43L21 H/W Control” switch controls the Hardware Mode options of the CS43L21. A description of each switch is outlined in the following table:

Switch	Position	Function
M/$\overline{S}$	LO	LRCK and SCLK are inputs to CS43L21
	HI	LRCK and SCLK are outputs to CS43L21
MCLKDIV2	LO	Internal MCLK to CS43L21 not divided
	HI	Internal MCLK to CS43L21 divided by 2
I2S/$\overline{LJ}$	LO	CS43L21 Interface Format: Left-Justified
	HI	CS43L21 Interface Format: I²S
DE-EMPHASIS	LO	No internal De-emphasis applied to CS43L21
	HI	44.1 kHz internal De-emphasis applied to CS43L21

Table 2. CS43L21 H/W Mode Control

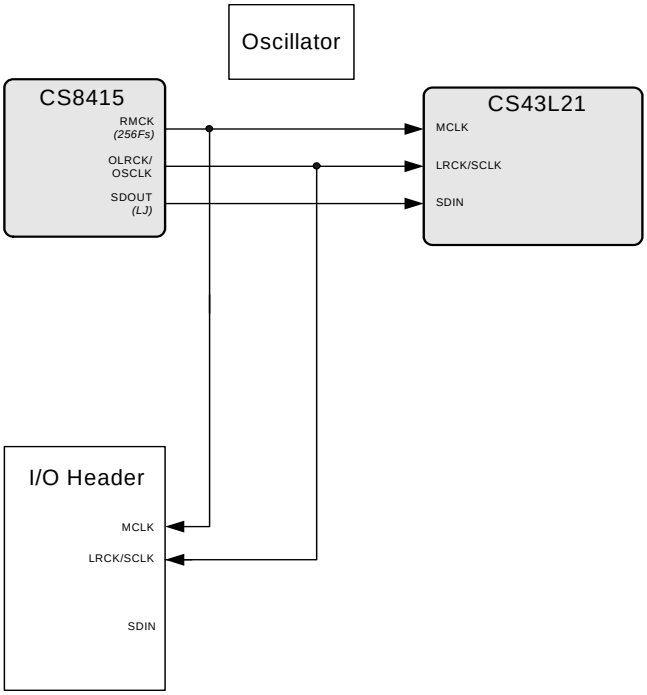


Figure 4. Routing 1

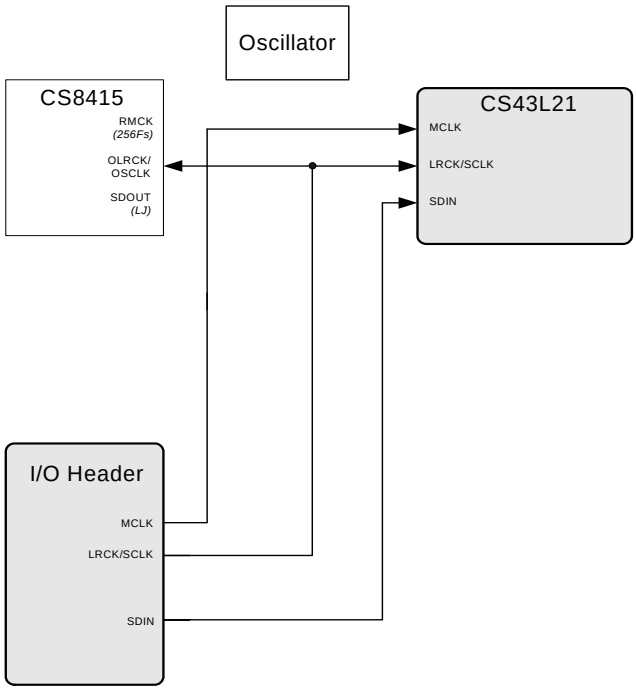


Figure 5. Routing 2

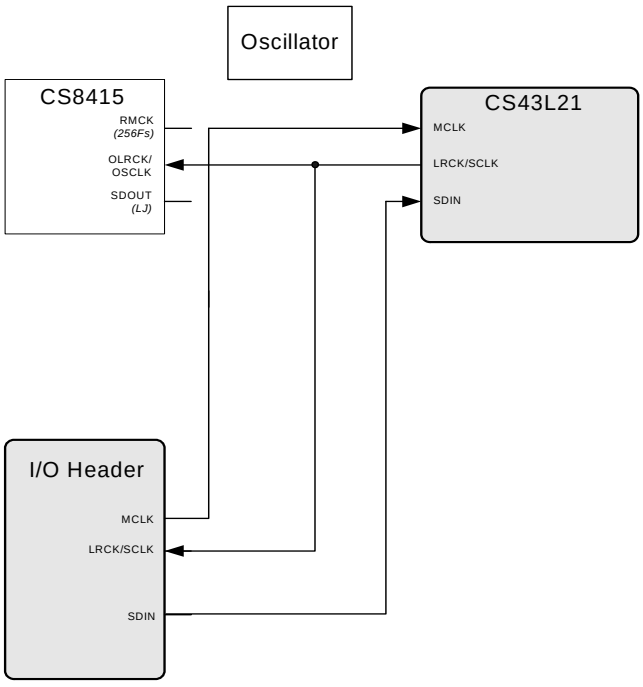


Figure 6. Routing 3

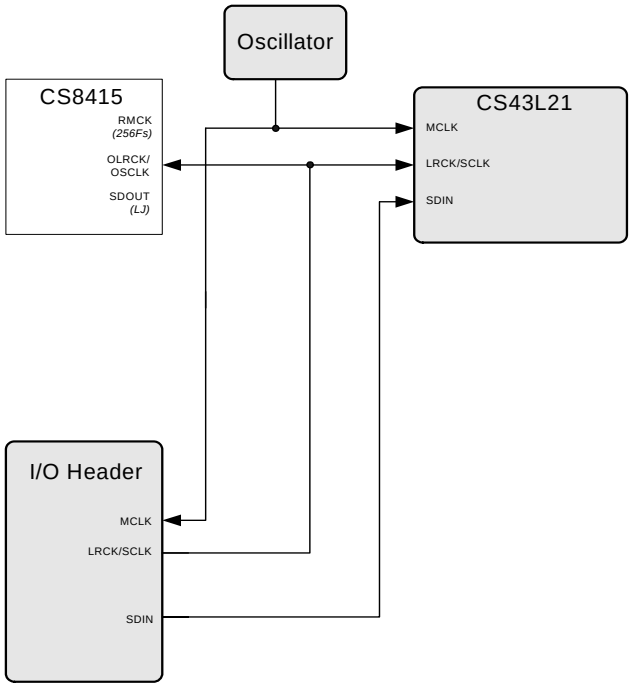


Figure 7. Routing 4

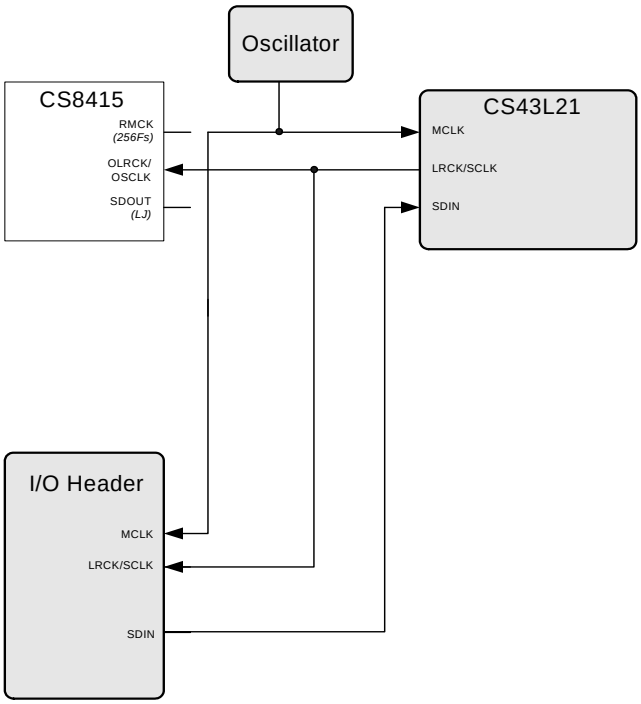


Figure 8. Routing 5

4. SYSTEM CONNECTIONS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J26	Input	+5.0 V Power Supply
GND	J27	Input	Ground Reference
RS232	J95	Input/Output	Serial connection to PC for SPI / I²C control port signals
USB	J94	Input/Output	USB connection to PC for SPI / I²C control port signals
S/PDIF OPTICAL IN	OPT1	Input	CS8415 digital audio input via optical cable
S/PDIF COAX IN	J61	Input	CS8415 digital audio input via coaxial cable
I/O Header	J5	Input/Output	I/O for Clocks & Data
S/W CONTROL	J109	Input/Output	I/O for external SPI / I²C control port signals
MICRO JTAG	J110	Input/Output	I/O for programming the micro controller (U84)
FPGA JTAG	J78	Input/Output	I/O for programming the FPGA (U14)
MICRO RESET	S4	Input	Reset for the micro controller (U84)
FPGA PROGRAM	S2	Input	Reload Xilinx Flash program into the FPGA (U14)
H/W BOARD RESET	S1	Input	Reset for the CS43L21 (U1)
LEFT RIGHT	J19 J20	Output	RCA phono jacks for analog outputs
SPEAKER + SPEAKER -	J72 J73	Output	Binding Post connected to LM4889 speaker driver for analog outputs
Headphone Jack	J11	Output	Headphone jack for analog outputs

Table 3. System Connections

5. JUMPER SETTINGS

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
J31	VL	Selects source of voltage for the VL supply * (Note 1)	*+1.8 V	Voltage source is +1.8 V regulator
			+2.5 V	Voltage source is +2.5 V regulator
			+3.3 V	Voltage source is +3.3 V regulator
J36	VA_HP	Selects source of voltage for the VA_HP supply	*+1.8 V	Voltage source is +1.8 V regulator
			+2.5 V	Voltage source is +2.5 V regulator
J25	VA	Selects source of voltage for the VA supply	*+1.8 V	Voltage source is +1.8 V regulator
			+2.5 V	Voltage source is +2.5 V regulator
J28	VD	Selects source of voltage for the VD supply	*+1.8 V	Voltage source is +1.8 V regulator
			+2.5 V	Voltage source is +2.5 V regulator
J52 J48 J47 J53	VL +VA_HP VA VD	Current Measurement	*SHUNTED	1 Ω series resistor is shorted
			OPEN	1 Ω series resistor in power supply path
J6	Left Channel	Selects between filtered and non-filtered output	*AOUTA	Connects AOUTA of part directly to LEFT RCA jack
			AOUTA (LPF)	Connects low-pass filtered AOUTA to LEFT RCA jack
J4	Right Channel	Selects between filtered and non-filtered output	*AOUTB	Connects AOUTB of part directly to RIGHT RCA jack
			AOUTB (LPF)	Connects lowpass filtered AOUTA to RIGHT RCA jack
J10	16 ohm HP LOAD	Load Simulation	SHUNTED	16 Ω resistor shunted from AOUTA to GND
			*Not connected	Jumper placed on pin 1
J13	16 ohm HP LOAD	Load Simulation	SHUNTED	16 Ω resistor shunted from AOUTB to GND
			*Not connected	Jumper placed on pin 1
*Default factory settings				

Notes: 1. Refer to Section 9 on page 25 regarding jumper settings for J31.

Table 4. Jumper Settings

6. CDB43L21 BLOCK DIAGRAM

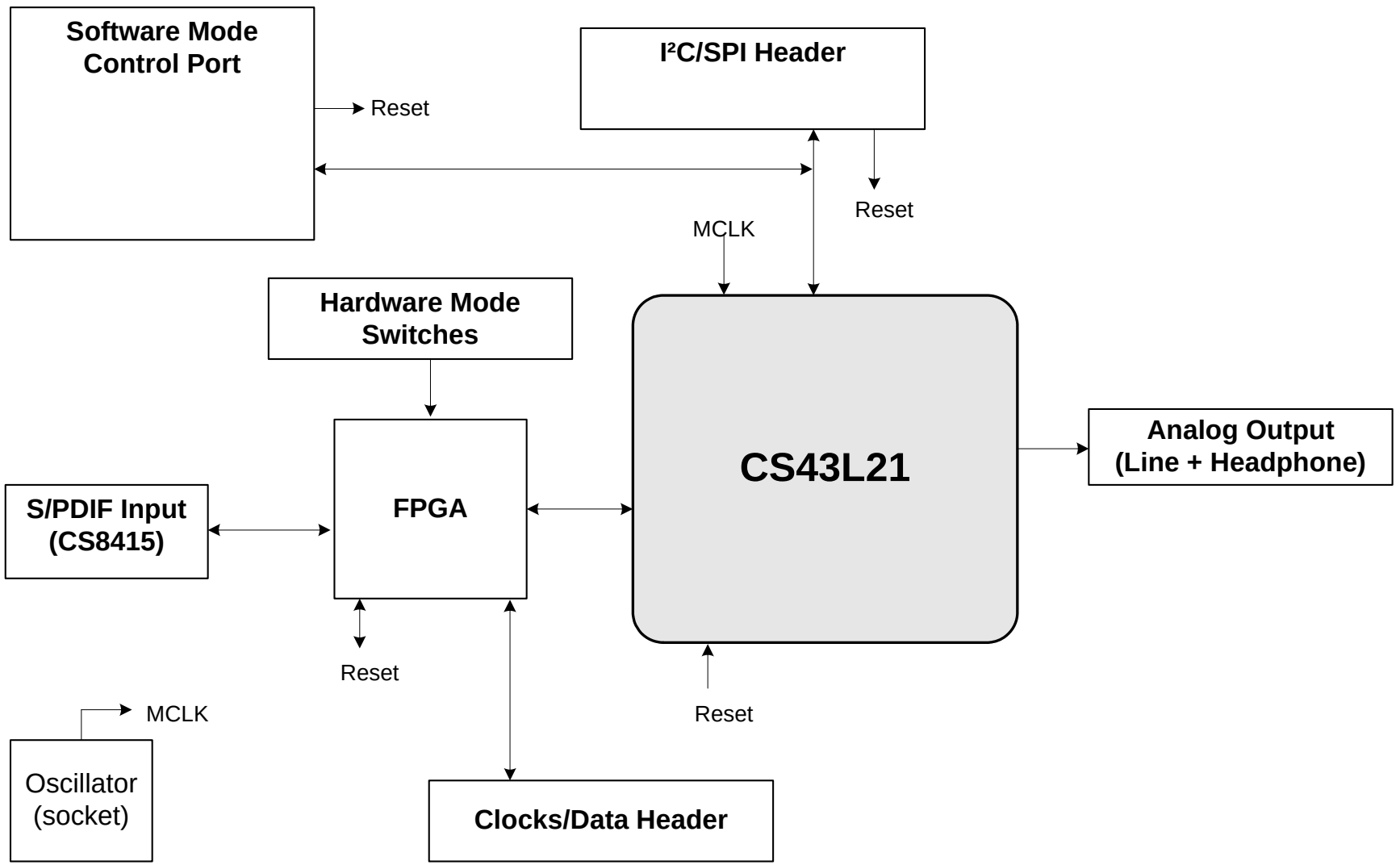


Figure 9. Block Diagram

7. CS43L21 SCHEMATICS

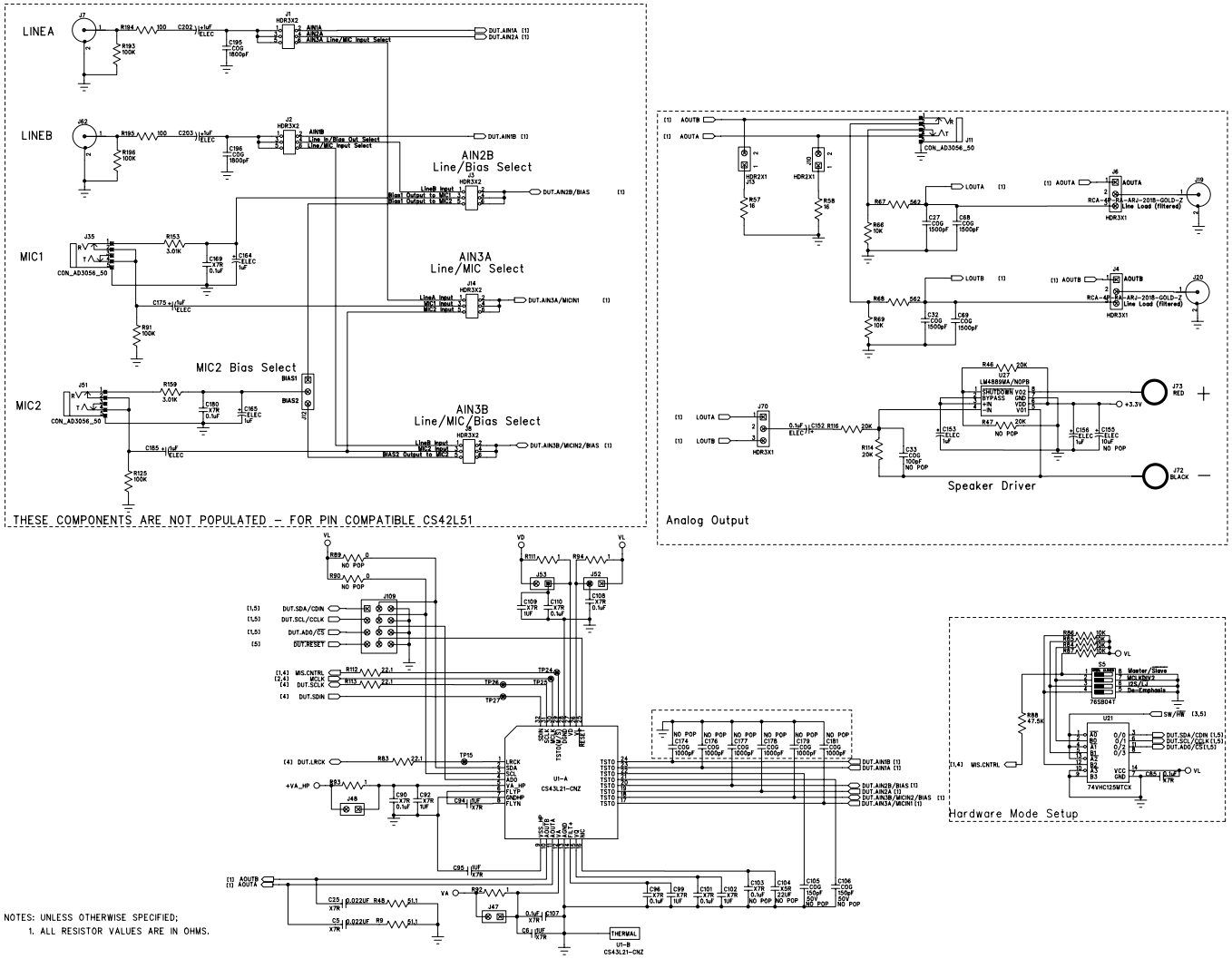


Figure 10. CS43L21 and Analog I/O (Schematic Sheet 1)

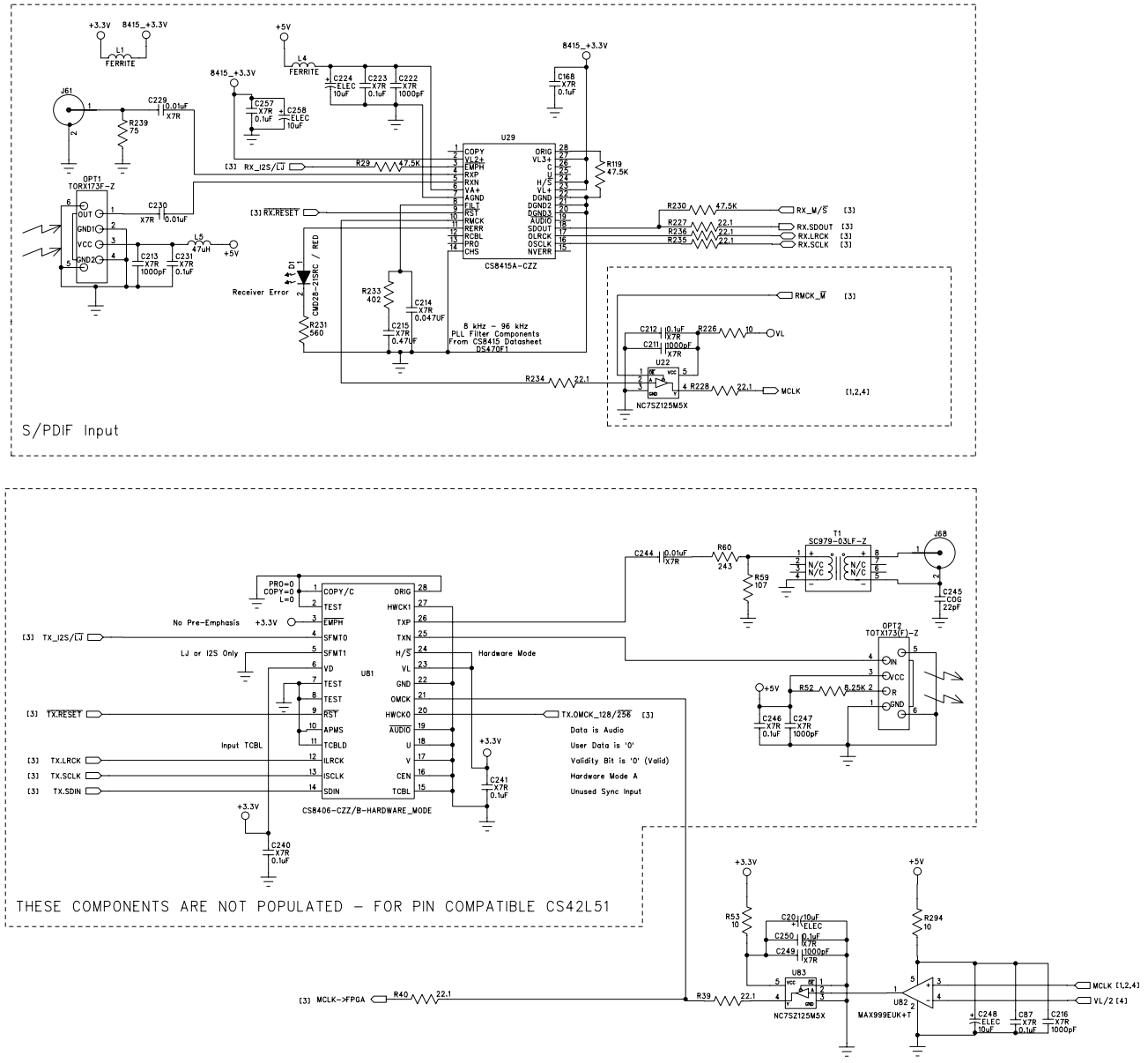


Figure 11. S/PDIF I/O (Schematic Sheet 2)

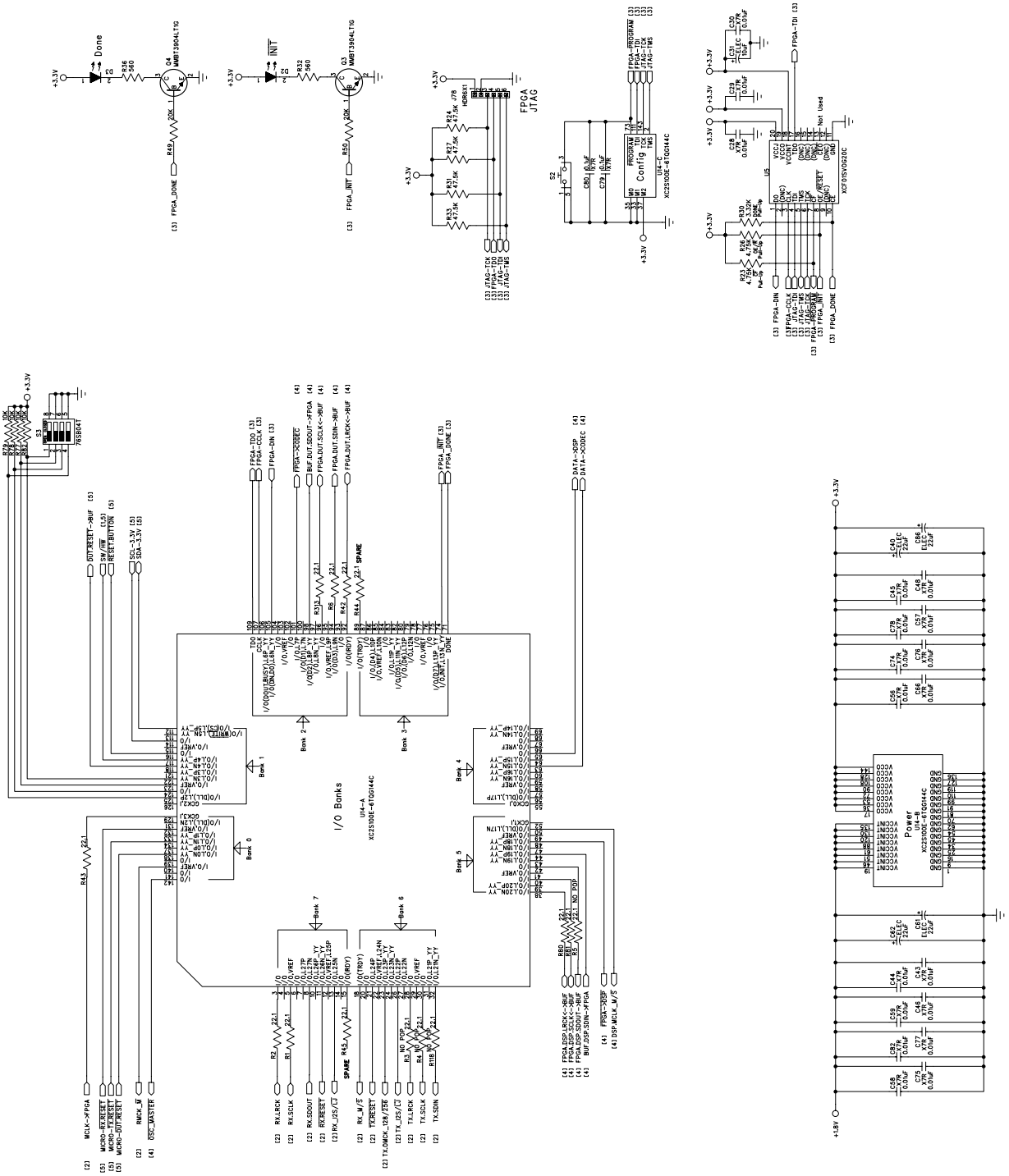


Figure 12. FPGA (Schematic Sheet 3)

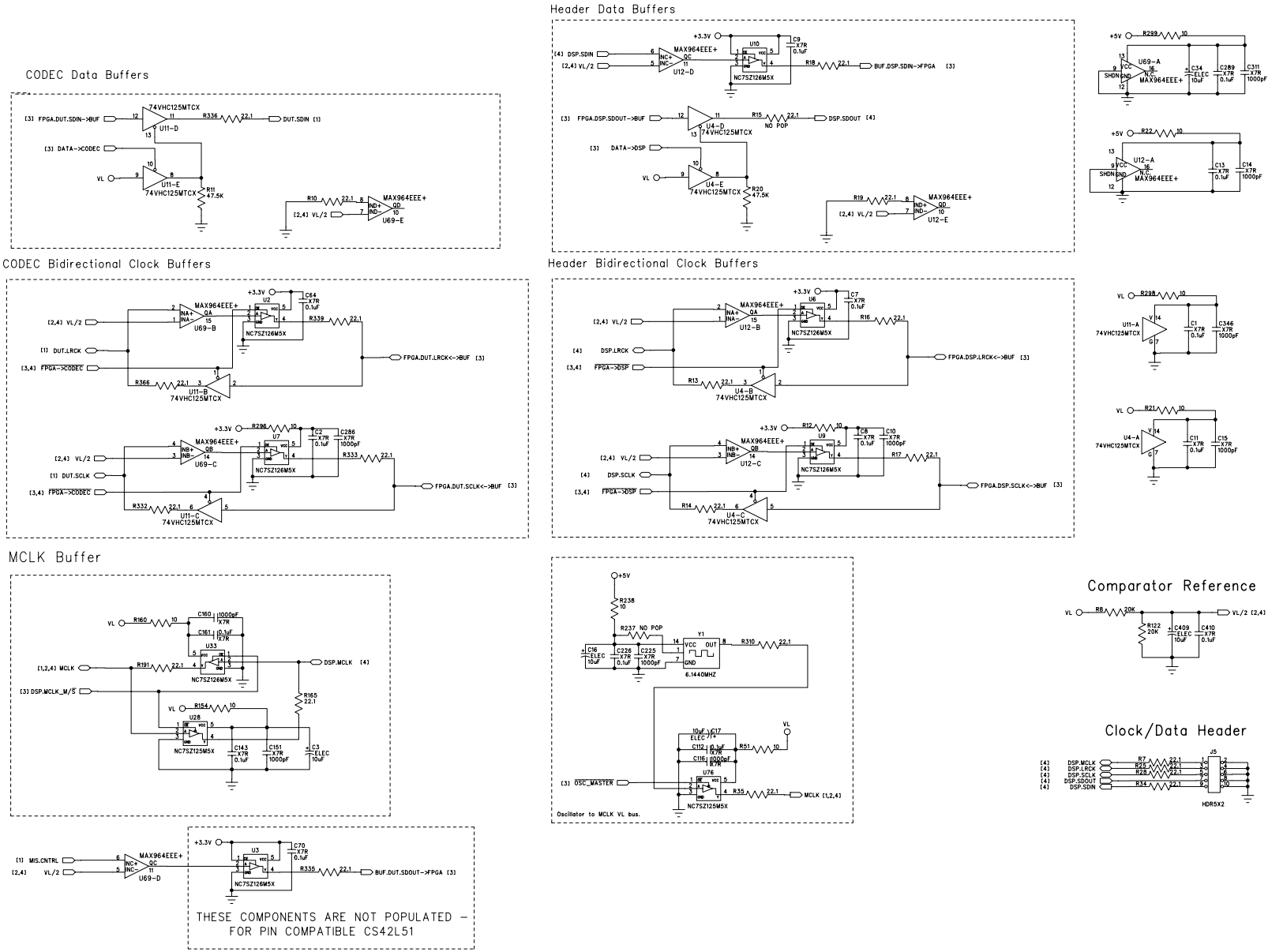


Figure 13. Level Shifters & I/O Stake Header (Schematic Sheet 4)

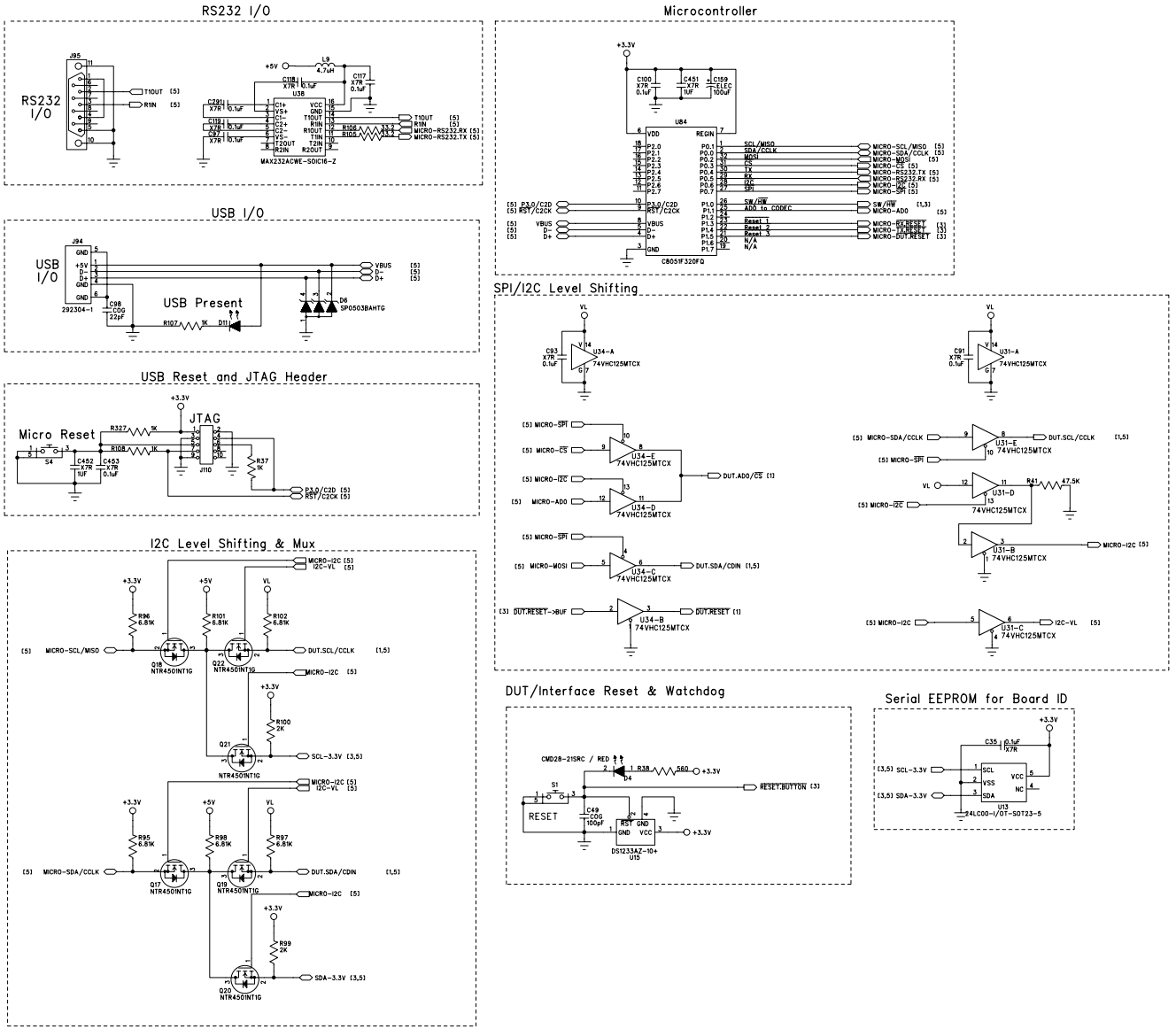


Figure 14. Control Port I/O (Schematic Sheet 5)

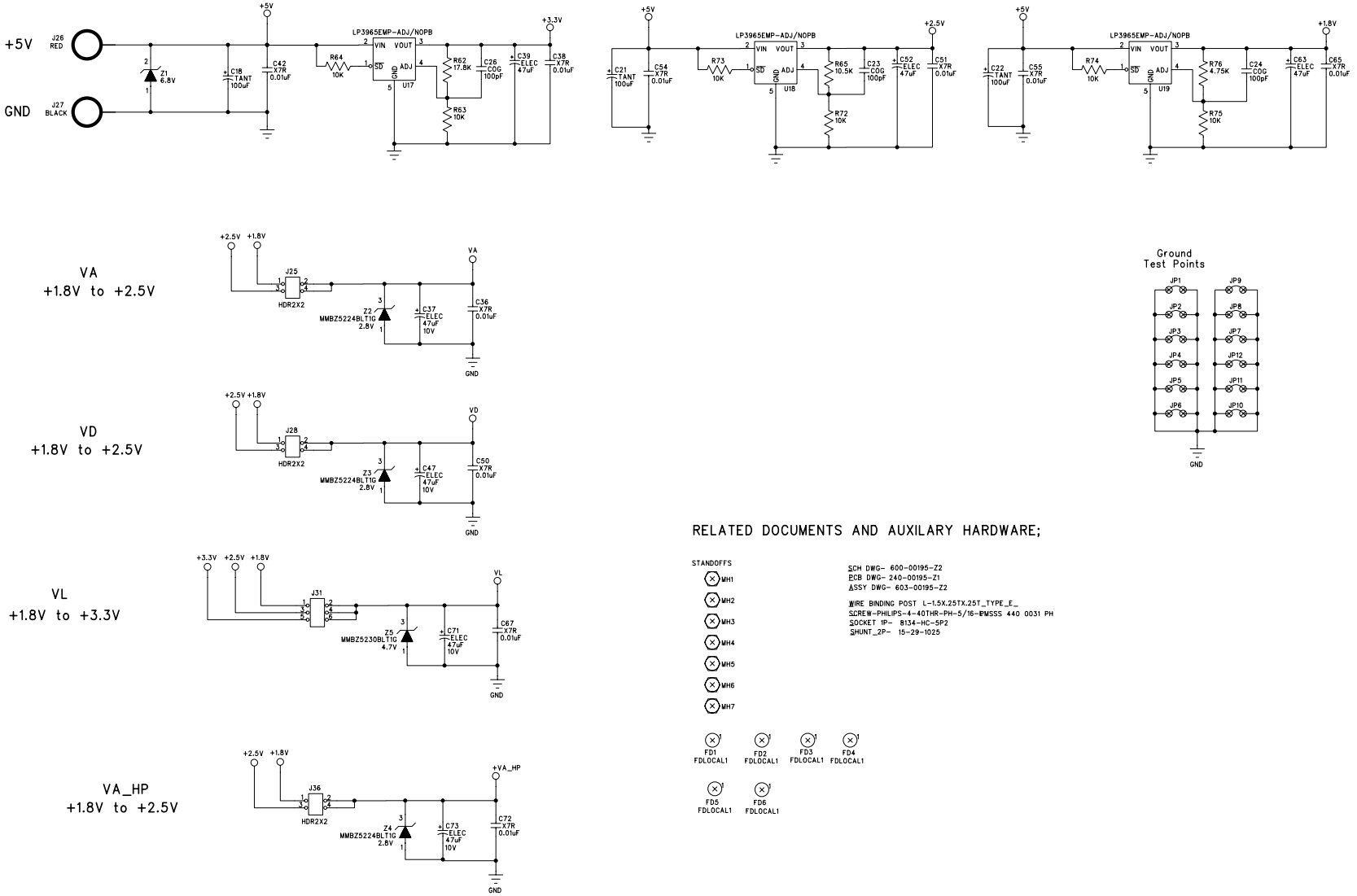


Figure 15. Power (Schematic Sheet 6)

8. CDB43L21 LAYOUT

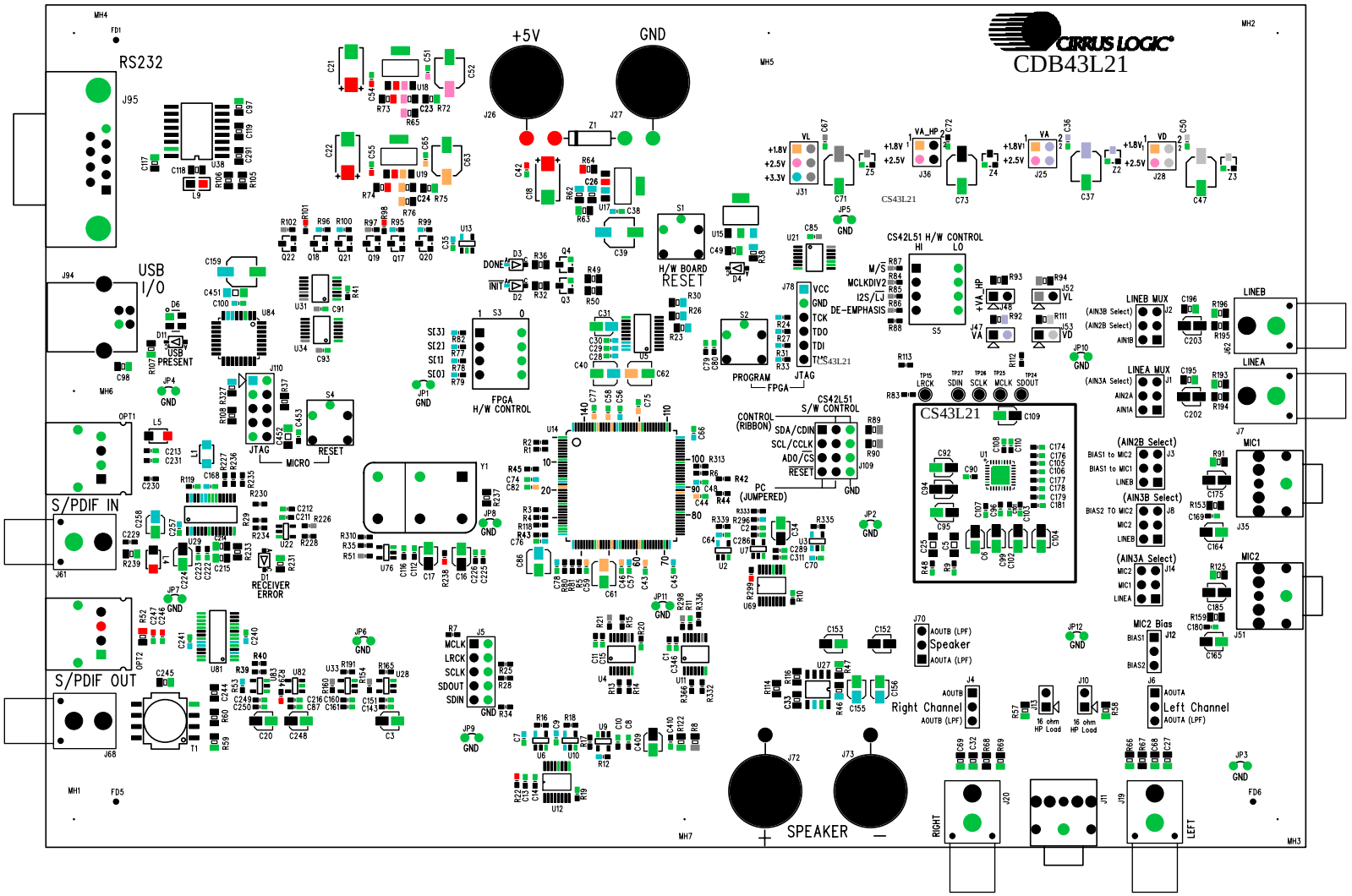


Figure 16. Silk Screen

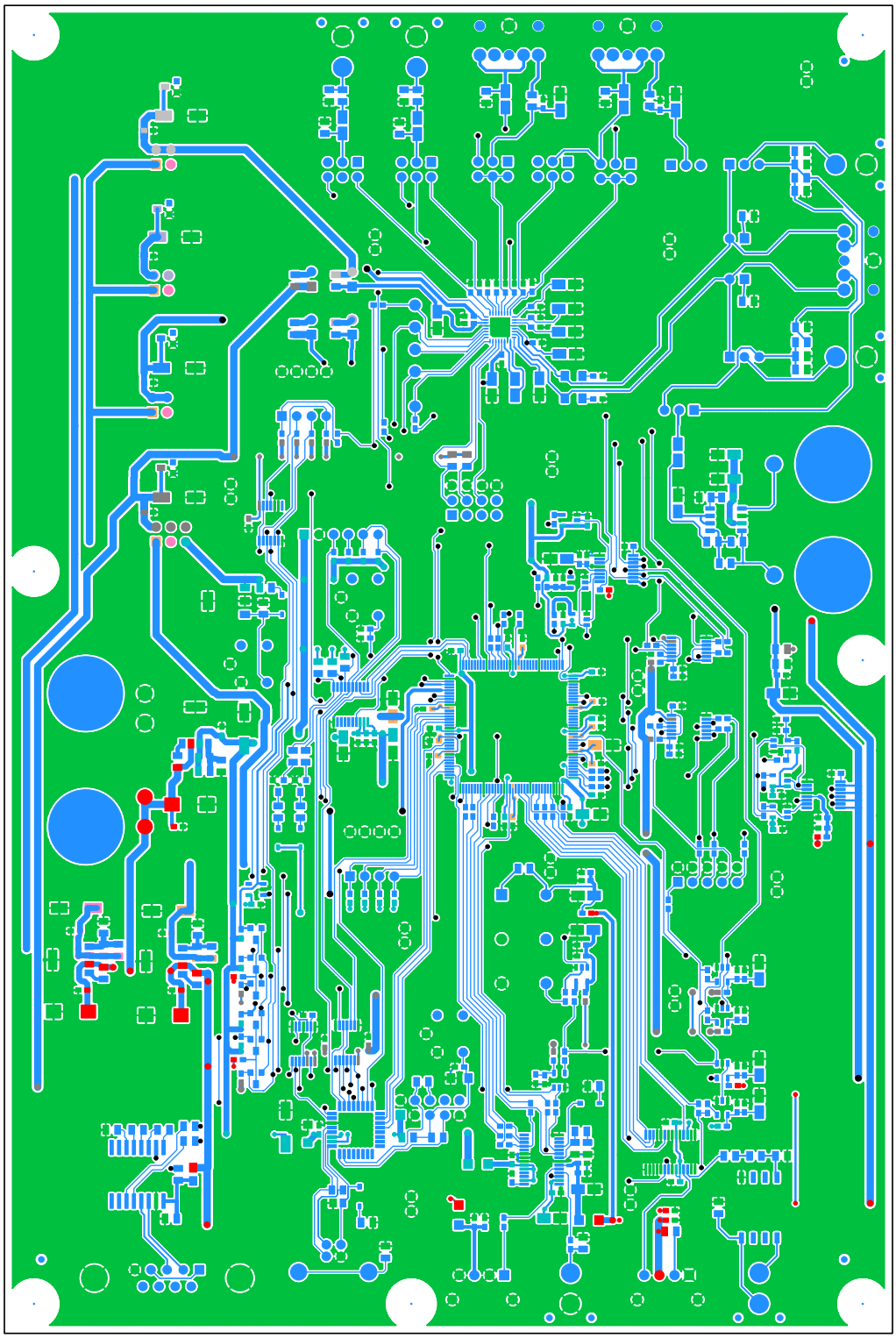


Figure 17. Top-Side Layer

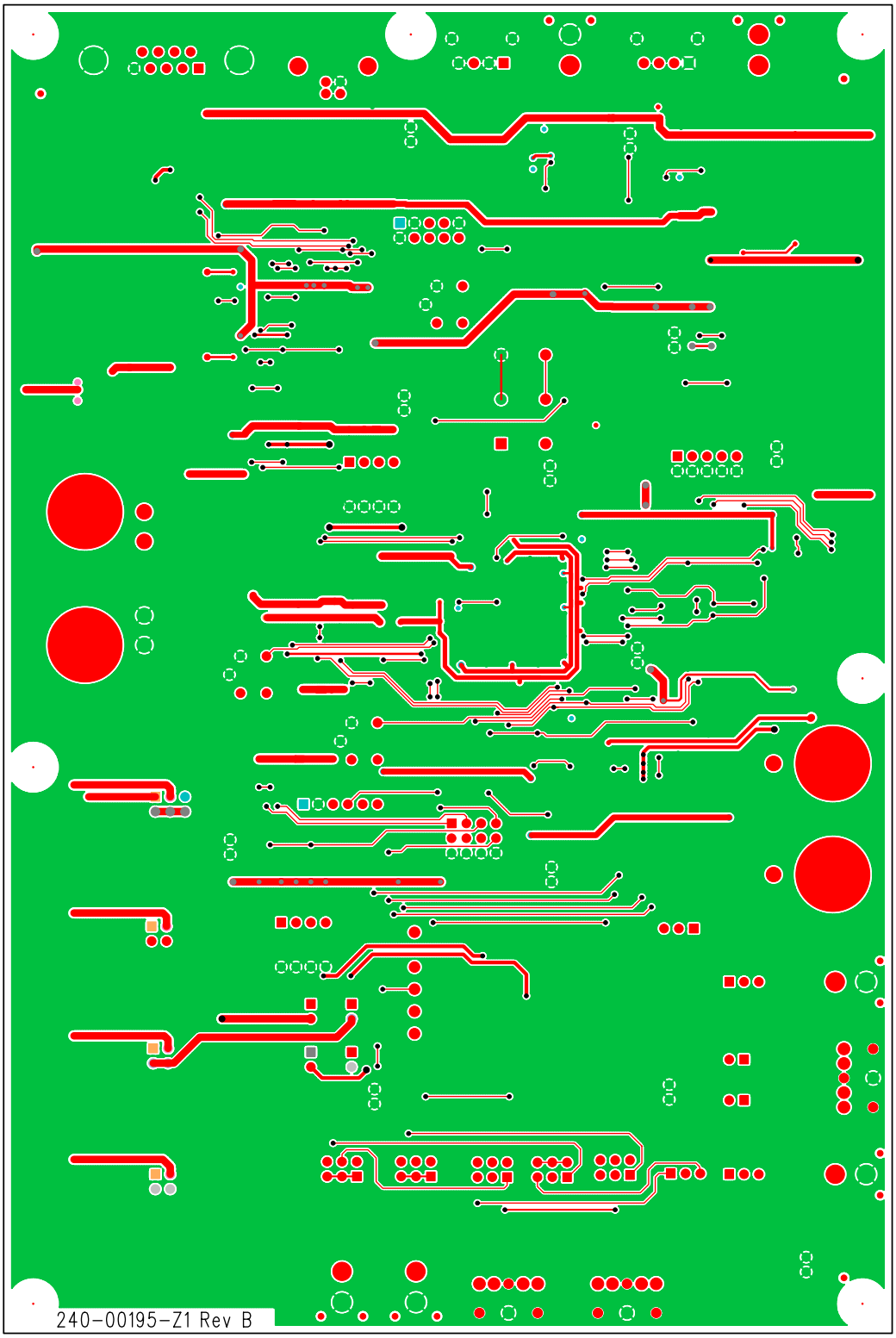


Figure 18. Bottom-Side Layer

9. ERRATA

The CDB43L21 currently does not support the +1.8 V and +2.5 V power supply options on header J31 (VL). This header must be set to +3.3 V to ensure correct board operation. This issue is not device related; the allowed voltage levels are specified in the CS43L21 data sheet.

10.REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.