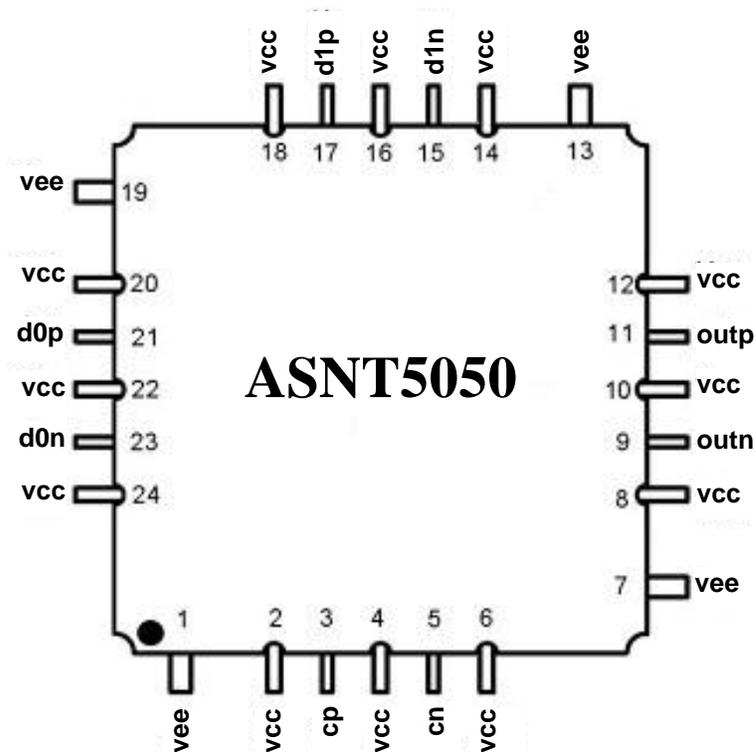# ASNT5050-KMC
DC-32*Gbps* Broadband Digital 2:1 Multiplexer/Selector

- High speed broadband 2:1 Multiplexer/Selector (MUX)

- Exhibits low jitter and limited temperature variation over industrial temperature range

- Ideal for use as a high isolation selector switch or as a high speed 2-to-1 serializer

- Ideal for high speed proof-of-concept prototyping

- Fully differential CML input interfaces

- Fully differential CML output interface with 400*mV* single-ended swing

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 450*mW*

- Fabricated in SiGe for high performance, yield, and reliability
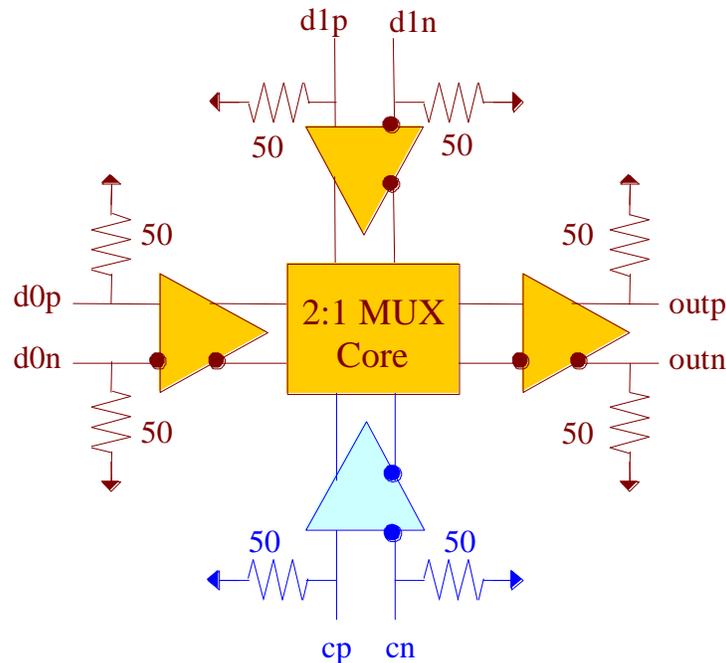
- Custom CQFP 24-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram

The temperature stable ASNT5050-KMC SiGe IC can be utilized as either a high isolation selector switch or a high speed 2:1 serializer, and is intended for use in high-speed measurement / test equipment. When employed as a selector switch, the IC shown in Fig. 1 can route one of its differential data input signals d0p/d0n or d1p/d1n to its differential output outp/outn while effectively blocking the other data input. Selection of a specific data input is achieved through an appropriate external DC biasing of the selector signal inputs cp/cn. The logic is shown in Table 1.

Table 1. Truth Table

c	d0	d1	out
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

As a 2:1 serializer, the IC can receive high speed input data signals into d0p/d0n and d1p/d1n and effectively multiplex them into a double frequency rate NRZ output data signal to its differential output outp/outn by using a high speed input clock signal on its selector signal inputs cp/cn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0V = ground and vee = −3.3V), or positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.5	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	^oC
Storage Temperature	-40	+100	^oC
Operational Humidity	10	98	$\%$
Storage Humidity	10	98	$\%$

TERMINAL FUNCTIONS

Name	No.	Type	DESCRIPTION
	TERMINAL		DESCRIPTION
High-Speed I/Os			
d0p	21	CML input	Differential data input signals with internal SE 50Ohm termination to vcc
d0n	23		
d1p	17	CML input	Differential data input signals with internal SE 50Ohm termination to vcc
d1n	15		
cp	3	CML input	Differential clock input signals with internal SE 50Ohm termination to vcc
cn	5		
outp	11	CML output	Differential data output signals with internal SE 50Ohm termination to vcc. Also require external SE 50Ohm termination to vcc
outn	9		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		135		*mA*	
Power consumption		450		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (d0p/d0n, d1p/d1n)					
Data rate / Frequency	DC		32/16	*Gbps/GHz*	When used as a selector
Data rate	DC		16	*Gbps*	When used as a multiplexer
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		16	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty cycle	45	50	55	*%*	
HS Output Data (outp/outn)					
Data rate / Frequency	DC		32/16	*Gbps/GHz*	When used as a selector
Data rate	DC		32	*Gbps*	When used as a multiplexer
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	12	13	14	*ps*	20%-80%
Output Jitter			2	*ps*	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5050-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.
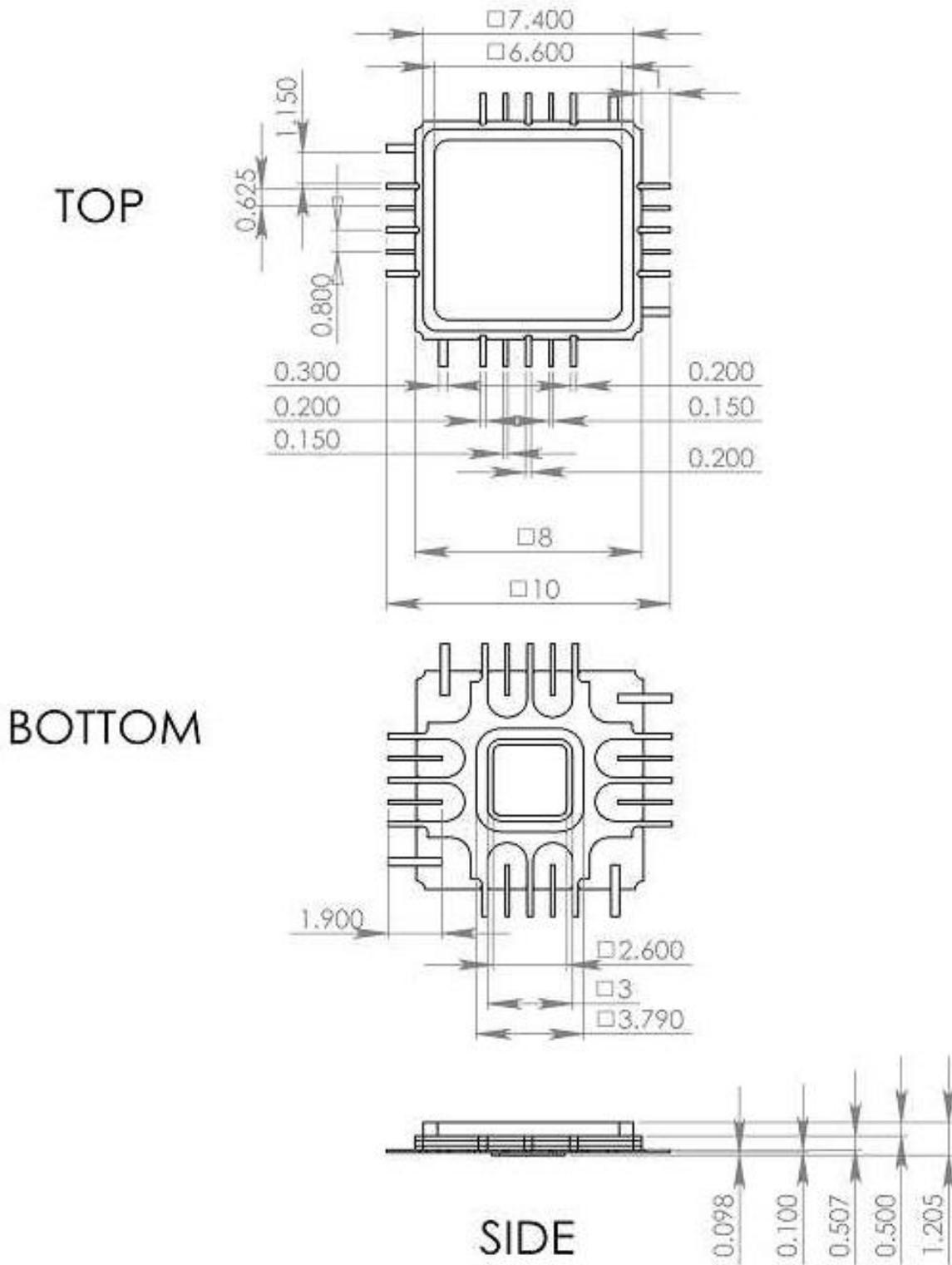
Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
2.2.2	05-2020	Updated Package Information
2.1.2	07-2019	Updated Letterhead
2.1.1	02-2019	Added truth table
		Revised package information section
2.0.1	02-2012	Format correction
		Revised title
		Added pinout drawing
		Revised functional block diagram
		Revised description section
		Added power supply configuration section
		Added absolute maximum ratings table
		Revised electrical characteristics section
		Revised package information section
		Added package mechanical drawing
1.0	10-2008	First release