



# MX775EBA644M531

Ultra-Low Jitter 644.53125MHz LVPECL XO

with Integrated Quartz Crystal

## General Description

The MX775EBA644M531 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

## Applications

- SONET FEC/OTN

## Features

- 644.53125MHz LVPECL
- Typical phase noise:
  - 82fs (Integration range: 12kHz-20MHz)
- $\pm 50$ ppm total frequency stability
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range
- Standard 6-Pin 7mm x 5mm LGA package
- Both the package and the crystal are MSL-1

## Absolute Maximum Ratings<sup>1</sup>

Supply Voltage (VDD).....+4.6V  
 Input Voltage (VIN).....-0.50V to VDD +4.6V  
 ESD Protection (HBM).....2kV  
 ESD Protection (MM).....200V

## Operating Ratings<sup>2</sup>

Supply Voltage (VDD).....+2.375V to +3.465V  
 Junction Thermal Resistance  
 LGA ( $\theta_{JA}$ ) .....52.8°C/W

## Electrical Characteristics

VDD = 3.3V  $\pm 5\%$  to 2.5V  $\pm 5\%$ , TA =  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted. RL = 50 $\Omega$  to VDD - 2V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Supply Voltage	VDD	2.375 3.135	2.5 3.3	2.625 3.465	V	2.5V Operation 3.3V Operation
Current Consumption	IDD	-	135	180	mA	@3.3V
Frequency Stability				$\pm 50$	ppm	Note 4
Output High Voltage	VOH	VDDO - 1.35	VDDO - 1.01	VDDO - 0.8	V	50 $\Omega$ to VDDO - 2V
Output Low Voltage	VOL	VDDO - 2	VDDO - 1.78	VDDO - 1.6	V	50 $\Omega$ to VDDO - 2V
Peak-to-Peak Output Voltage	VSWING	0.65	0.77	0.95	V	
Output Rise/Fall Time	tR/tF	85	135	350	ps	LVPECL output
Output Duty Cycle	ODC	45 48	50 50	55 52	%	All output frequencies < 450MHz output frequencies
PLL Lock Time	TLOCK	-	5	20	ms	Time from 90% VDD
RMS Phase Jitter <sup>3</sup>	tJIT( $\emptyset$ )	-	82	-	fs	644.53125MHz, Integration range (12kHz-20MHz)

### Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. All phase noise measurements were taken with an Agilent 5052B phase noise system.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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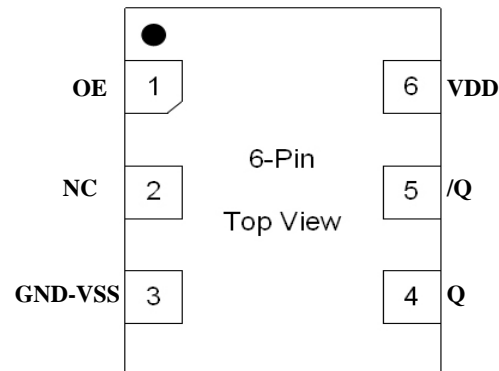
Revision 1.0  
[tcghelp@microchip.com](mailto:tcghelp@microchip.com)

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX775EBA644M531	MX775EB	A644M531	Tube	6-Pin 7mm x 5mm LGA
MX775EBA644M531-TR	MX775EB	A644M531	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables to tri-state, 0 = Disabled, 1 = Enabled, 75kΩ Pull-Up (Internal)
2	NC			No connect No internal connections to the ASIC are made
3	GND-VSS	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 644.53125MHz
6	VDD	PWR		Power Supply

## Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10 <sup>-8</sup> atm cc/s
MSL Level	Crystal and Package MSL-1
Solvent Resistance	MIL-STD-202, Method 215

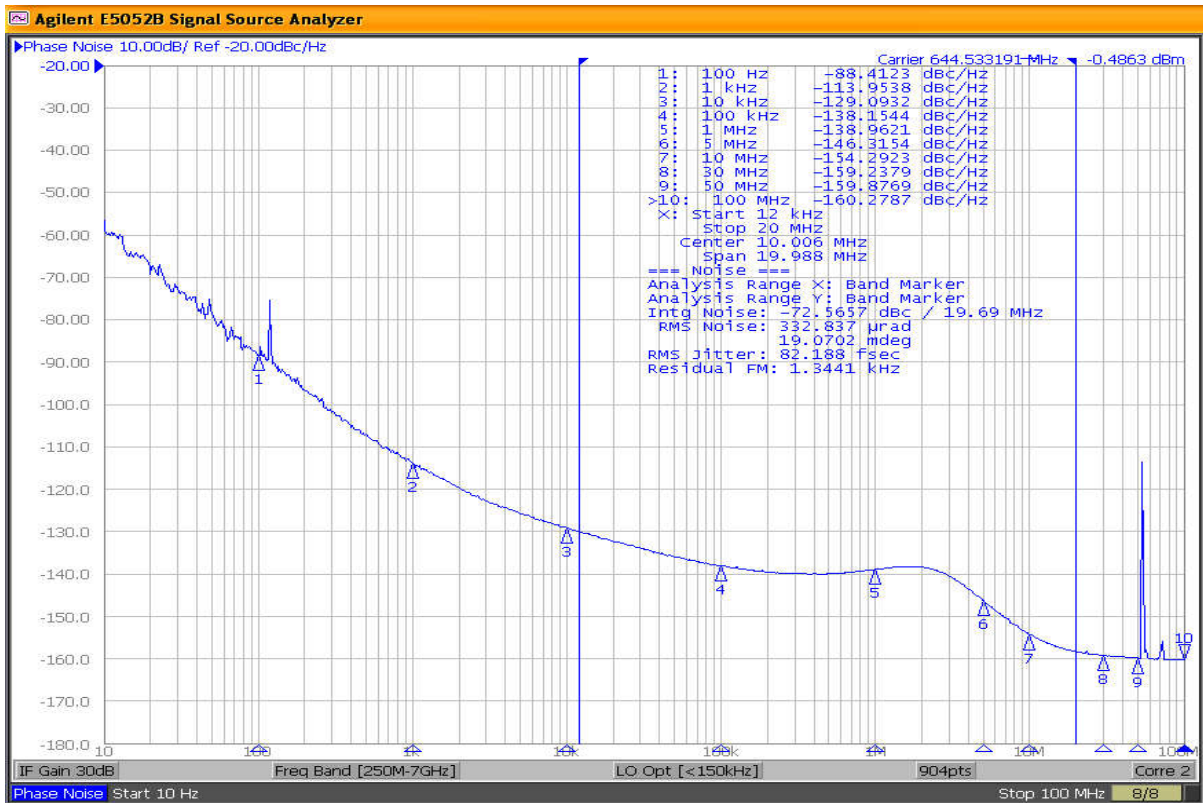


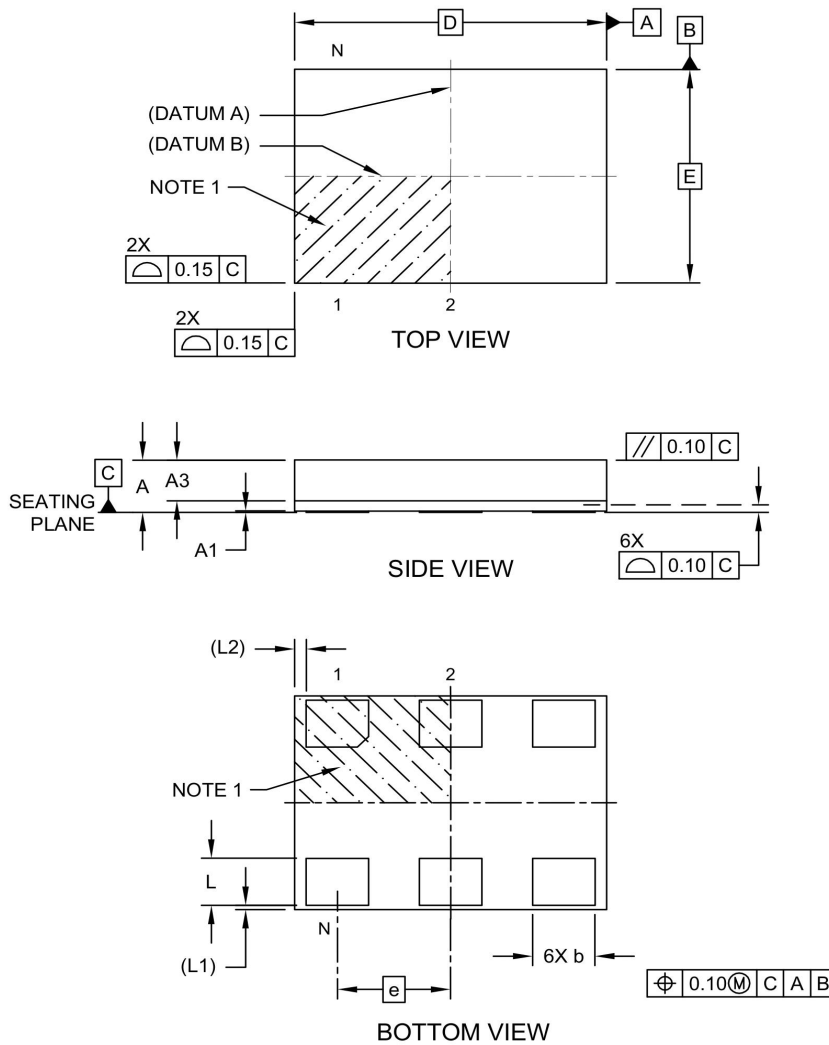
Figure 1. LVPECL Output 644.53125MHz 12kHz-20MHz 82fs

Package Information



6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



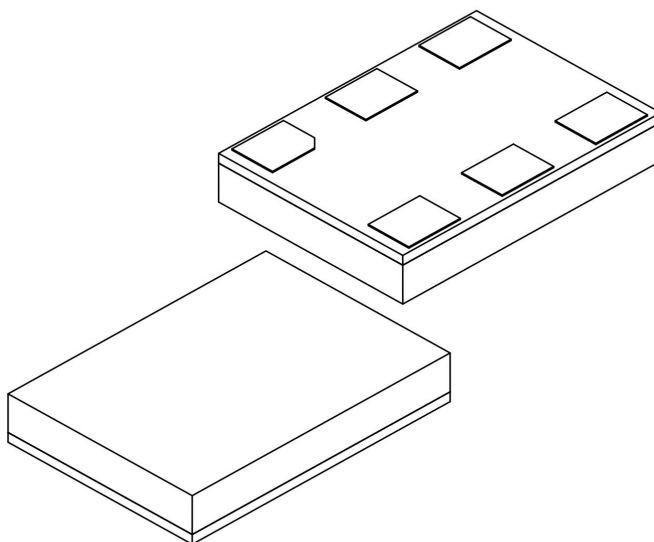
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### 6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	2.54 BSC		
Overall Height	A	1.08	1.15	1.22
Standoff	A1	–	–	0.03
Mold Cap Thickness	A3	0.85	0.90	0.95
Overall Length	D	7.00 BSC		
Overall Width	E	5.00 BSC		
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.05	1.10	1.15
Terminal Pullback	L1	0.10 REF		
Terminal Offset	L2	0.26 REF		

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

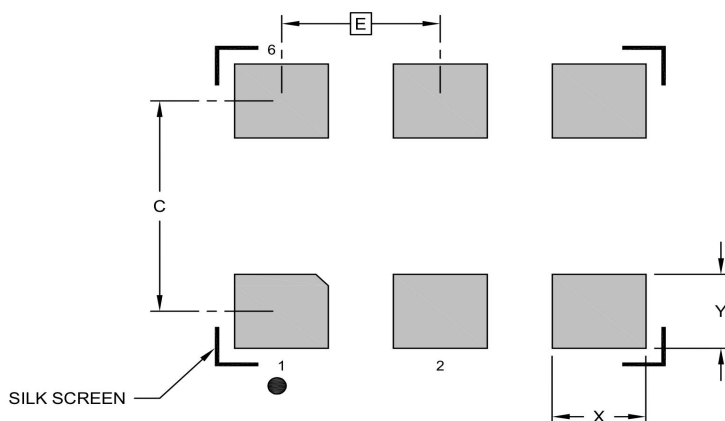
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**6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**RECOMMENDED LAND PATTERN**

Dimension Limits	Units	MILLIMETERS		
	E	MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Contact Pad Spacing	C		3.70	
Contact Pad Width (Xnn)	X			1.50
Contact Pad Length (Xnn)	Y			1.30

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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