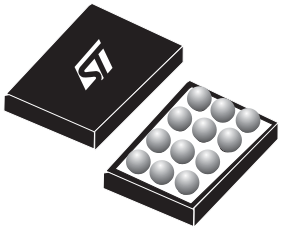
STG5678

Low voltage dual SPDT switch with negative rail capability

Features

- Distortion-free negative signal throughput down to V_{CC} - 5.5 V
- Wide operating voltage range: V_{CC} (opr) = 1.65 to 4.5 V single supply
- Ultra low power dissipation: I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- Low ON resistance: R_{ON} = 0.5 Ω (max. T_A = 25 °C) at V_{CC} = 3.6 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 1.65 V to 4.5 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
  - 2000-V human-body model (IEC61340-3-1:2002 level 2)
  - 200-V machine model (IEC61340-3-2 level M2)
  - 1000-V charge device model (JESD22-C101-A level III)



Flip-chip 12

Description

The STG5678 is a high-speed CMOS low voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/de-multiplexer switch fabricated in silicon gate CMOS technology. It is designed to operate from 1.65 to 4.5 V.

The device is capable of handling signals with negative voltages from V_{CC} - 5.5 V to V_{CC} without any distortion.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

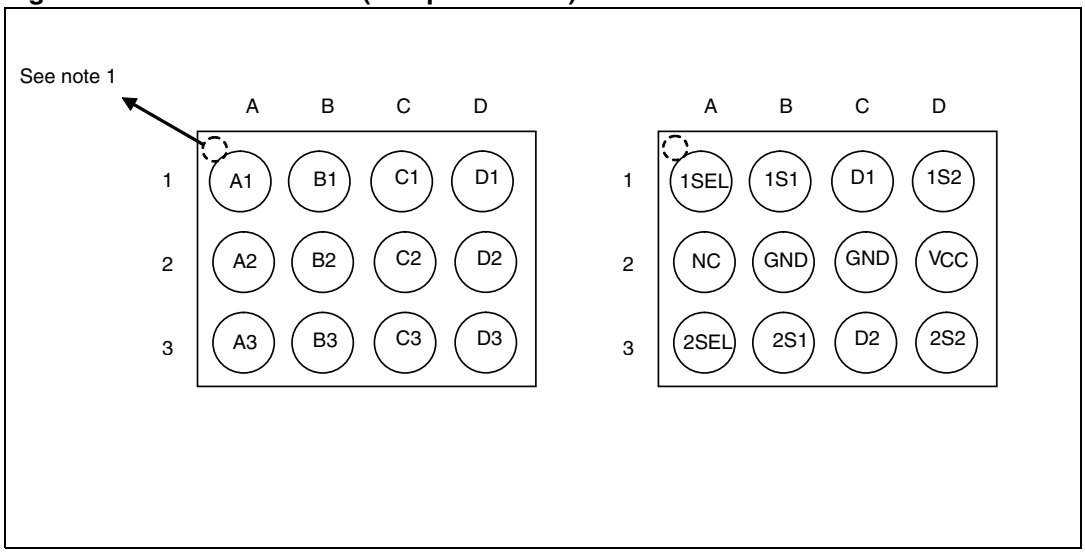
Order code	Package	Packaging
STG5678BJR	Flip-chip 12	Tape and reel
STG5678CJR	Flip-chip 12 (with back side coating)	Tape and reel

Contents

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (bump side view)



1. Note 1: bump A1 is distinguished by a circular dot on the top-side. There is no circular dot on the bump-side.

1.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
A1	1SEL	Selection control for switch 1
A2	NC	No connection
A3	2SEL	Selection control for switch 2
B1	1S1	Independent channel for switch 1
B2	GND	Ground (0 V)
B3	2S1	Independent channel for switch 2
C1	D1	Common channel for switch 1
C2	GND	Ground (0 V)
C3	D2	Common channel for switch 2
D1	1S2	Independent channel for switch 1
D2	V_{CC}	Positive supply voltage
D3	2S2	Independent channel for switch 2

2 STG5678 device summary

Figure 2. Functional diagram

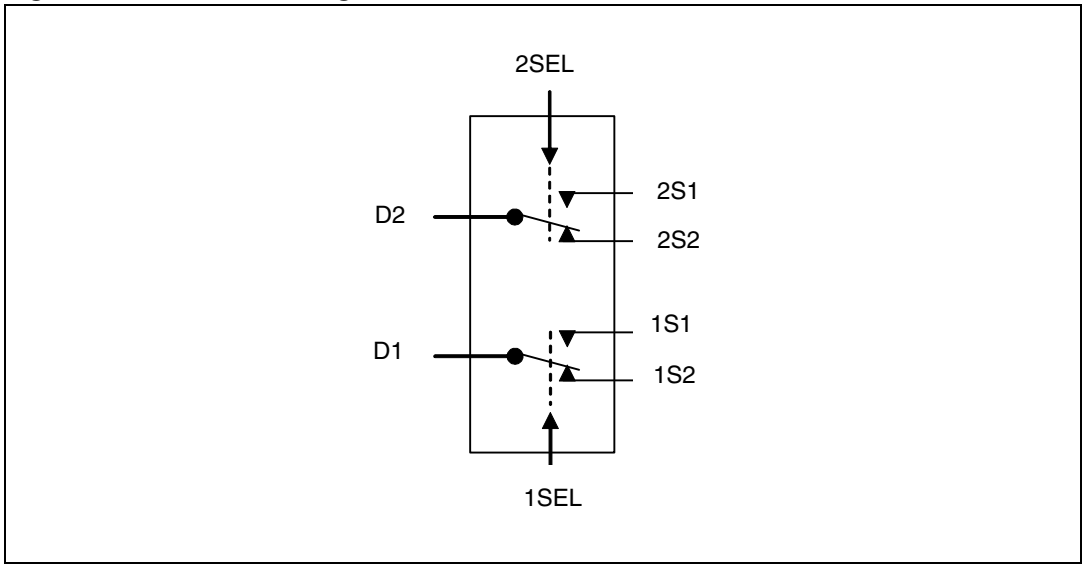


Figure 3. Input equivalent circuit

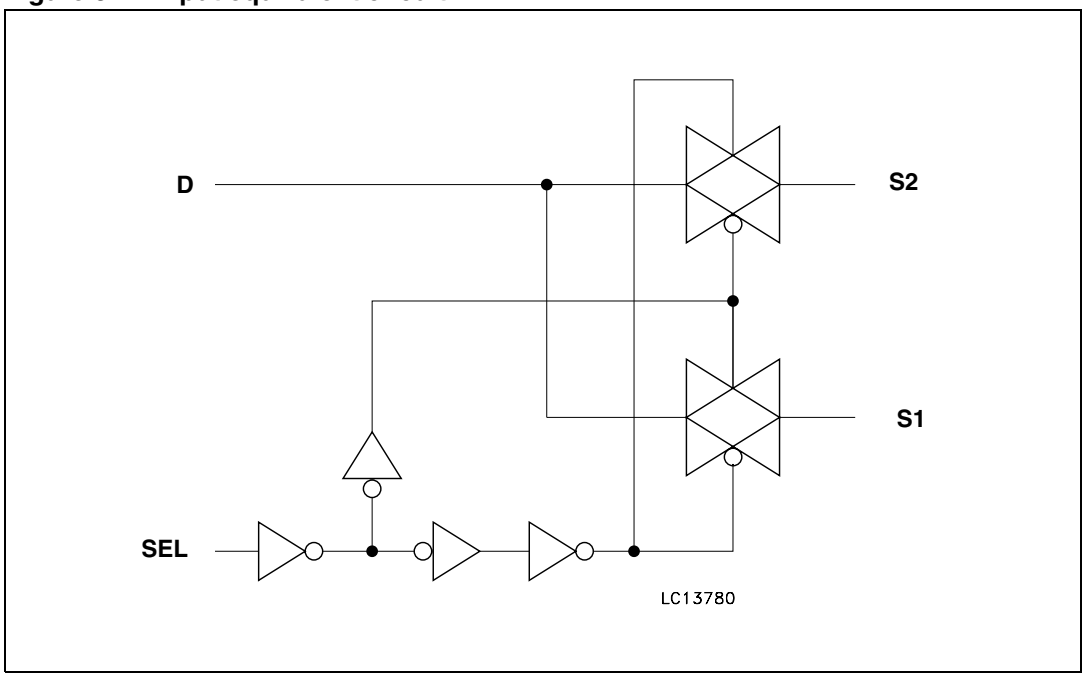


Table 3. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF (1)
L	OFF (1)	ON

1. High impedance

3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	- (V_{CC} - 6.0) to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	- (V_{CC} - 6.0 V) to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL} < 0 V)	-50	mA
I_{IK}	DC input diode current (V_{IN} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±150	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70°C (1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 ºC by 18.5 mW/C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.5	V
V_I	Input voltage		V_{CC} -5.5 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.5	V
V_O	Output voltage		V_{CC} -5.5 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.5 V	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 –1.95		0.9	–	–	0.9	–	V
		2.25 –2.7		0.9	–	–	0.9	–	
		3.0 –4.3		1.0	–	–	1.0	–	
		4.5		1.1	–	–	1.1	–	
V_{IL}	Low level input voltage	1.65 –1.95		–	–	0.6	–	0.6	V
		2.25 –2.7		–	–	0.6	–	0.6	
		3.0 –4.3		–	–	0.7	–	0.7	
		4.5		–	–	0.7	–	0.7	
R_{ON}	Switch ON resistance	1.8	$V_S = V_{CC}$ –5.5 V to V_{CC}; I_S = 100 mA	–	3.80	4.60	–	7.0	Ω
		2.7		–	0.77	0.90	–	1.2	
		3.0		–	0.64	0.80	–	1.0	
		3.6		–	0.51	0.65	–	1.0	
ΔR_{ON}	ON resistance match between channels (1)	1.8	V_S at R_{ON} max I_S = 100 mA	–	50	–	–	500	mΩ
		2.7		–	20	–	–	500	
		3.0		–	15	–	–	500	
		3.6		–	15	–	–	500	
R_{FLAT}	ON resistance flatness (2)	1.8	$V_S = V_{CC}$ –5.5 V to V_{CC}; I_S = 100 mA	–	3.5	–	–	6.6	Ω
		2.7		–	0.50	–	–	0.8	
		3.0		–	0.40	–	–	0.6	
		3.6		–	0.25	–	–	0.5	
I_{OFF}	Sn OFF state leakage current	3.6	V_S = -1.2 to 3.6 V V_D = 3.6 to -1.2 V	–	-0.55	–	-2	1	µA
I_{ON}	Sn ON state leakage current	3.6	V_S = -1.2 to 3.6 V V_D = open	–	-0.55	–	-2	1	µA

Table 6. DC specifications (continued)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
I_D	D ON state leakage current	3.6	V_S = open V_D = -1.2 V to 3.6 V	–	0.55	–	-2	1	µA
I_{IH},I_{IL}	SEL leakage current	3.6	V_{SEL}= 3.6 V or GND	-0.1		0.1	-1	1	µA
I_{CCLV}	Quiescent supply current low voltage driving	3.6	V_{1SEL}, V_{2SEL} = 1.80 V	–	7	–	–	10	µA
I_{CC}	Quiescent supply current(3)	2.5	V_{1SEL}= V_{2SEL} = V_{CC}	–	5.6	–	–	10	µA
		3.6		–	8	–	–	16	
		1.65 –4.5	V_{1SEL}= V_{2SEL} = GND	–	0.05	–	–	0.1	

1. Note 1: $\Delta R_{ON} = R_{ON(max)} - R_{ON\ (min)}$
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
3. When V_{1SEL} and V_{2SEL} is both low, the I_{CC} consumption will reduce to less than 0.1 µA (max)

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, t_r = t_f ≤5 ns)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 – 1.95		–	0.45	–	–	–	ns
		2.3 – 2.7		–	0.40	–	–	–	
		3.0 – 3.3		–	0.30	–	–	–	
		3.6		–	0.25	–	–	–	
t_{ON}	Turn ON time	1.65 – 1.95	V_S = 0.8 V	–	220	265	–	–	ns
		2.3 – 2.7	V_S = 1.5 V	–	140	175	–	–	
		3.0 – 3.3		–	110	135	–	–	
		3.6		–	105	130	–	–	
t_{OFF}	Turn OFF time	1.65 – 1.95	V_S = 0.8	–	120	150	–	–	ns
		2.3 – 2.7	V_S = 1.5 V	–	77	92	–	–	
		3.0 – 3.3		–	77	92	–	–	
		3.6		–	77	92	–	–	
t_D	Break-before-make time delay	1.65 – 1.95	C_L = 35 pF, R_L = 50 Ω, V_S = V_{CC}/2	–	120	–	–	–	ns
		2.3 – 2.7		–	66	–	–	–	
		3.0 – 3.3		–	40	–	–	–	
		3.6		–	30	–	–	–	
Q	Charge injection	1.65 – 1.95	C_L = 100 pF, V_{GEN} = 0 V	–	55	–	–	–	pC
		2.3 – 2.7		–	76	–	–	–	
		3.0 – 3.3		–	94	–	–	–	
		3.6		–	126	–	–	–	

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
O_{IRR}	OFF isolation (1)	2.7 – 3.6	V_S = 1 V_{RMS}, f = 100 kHz	–	-86	–	–	–	dB
			V_S = 1 V_{RMS}, f = 1 MHz	–	-70	–	–	–	
			V_S = 1 V_{RMS}, f = 5 MHz	–	-54	–	–	–	
X_{talk}	Crosstalk(2)	2.7 – 3.6	V_S = 1 V_{RMS}, f = 100 kHz	–	-96	–	–	–	dB
			V_S = 1 V_{RMS}, f = 1 MHz	–	-87	–	–	–	
			V_S = 1 V_{RMS}, f = 5 MHz	–	-74	–	–	–	
T_{HD}	Total harmonic distortion	2.7 – 3.6	R_L = 32 Ω V_{IN} = 0.5 V_{PP} DC bias = 0 f = 20 Hz to 20 kHz	–	0.01	–	–	–	%
BW	-3dB bandwidth	2.7 – 3.6	R_L = 50 Ω Signal = 0 dBm	–	30	–	–	–	MHz
C_{SEL}	Control pin input capacitance	3.3	f = 1 MHz	–	12	–	–	–	pF
$C_{Sn(OFF)}$	OFF Sn port capacitance	3.3	f = 1 MHz	–	120	–	–	–	pF
C_D	D port capacitance when switch is enabled	3.3	f = 1 MHz	–	290	–	–	–	pF

1. Off isolation = 20Log10 (V_D/V_S), V_D = output. V_S = input to off switch.
2. Crosstalk values are measured between two switches.

5 Test circuit

Figure 4. ON resistance

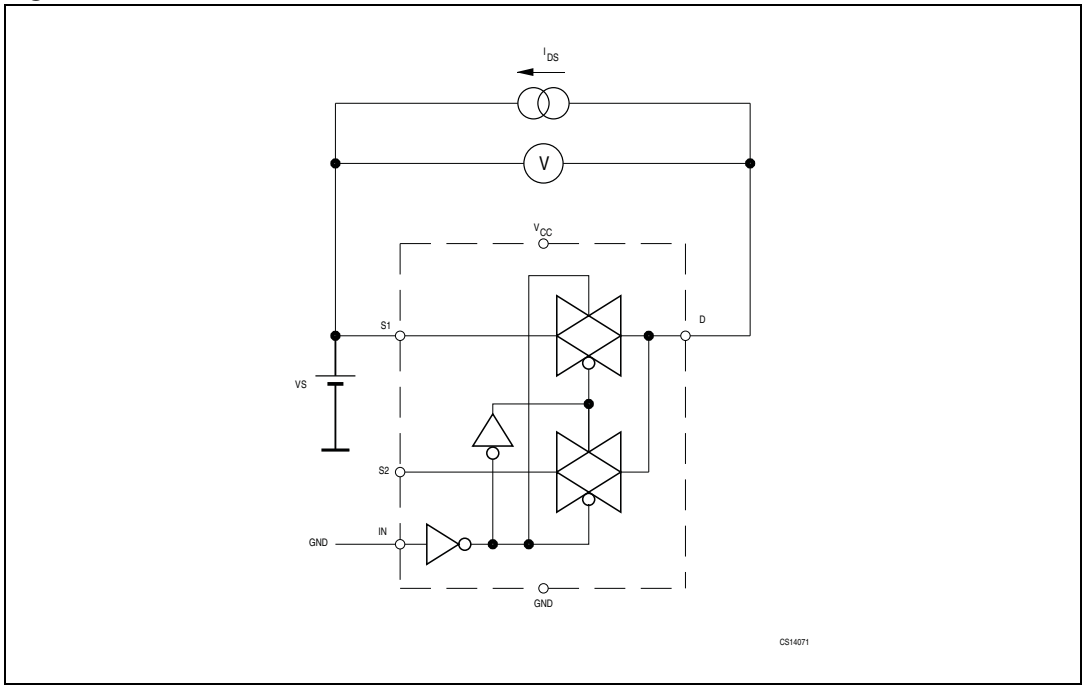


Figure 5. OFF leakage

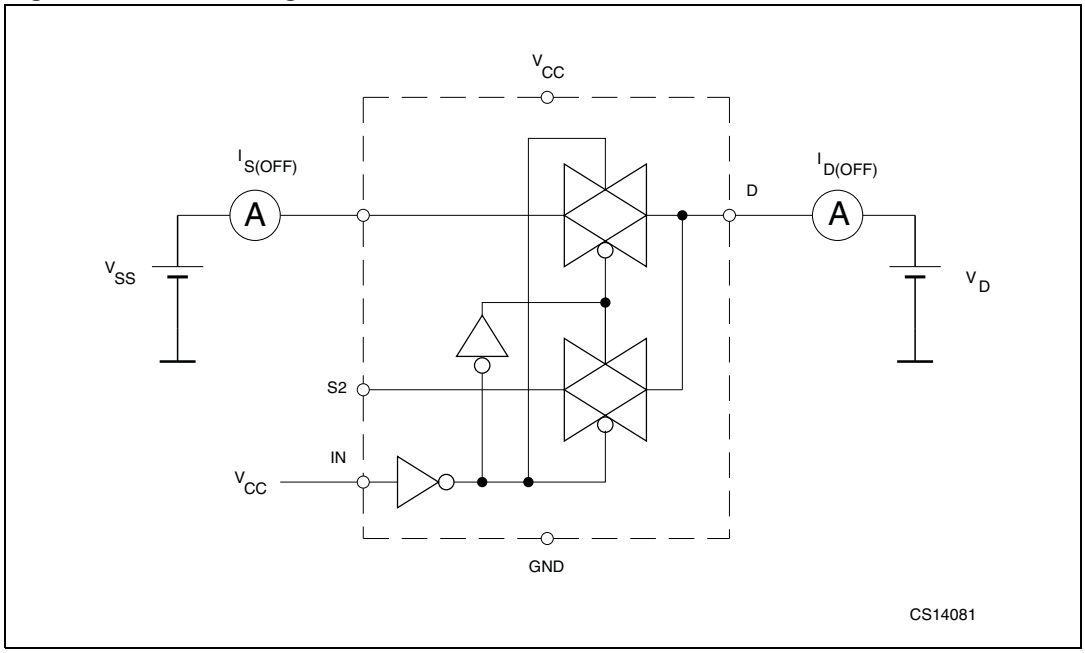


Figure 6. OFF isolation

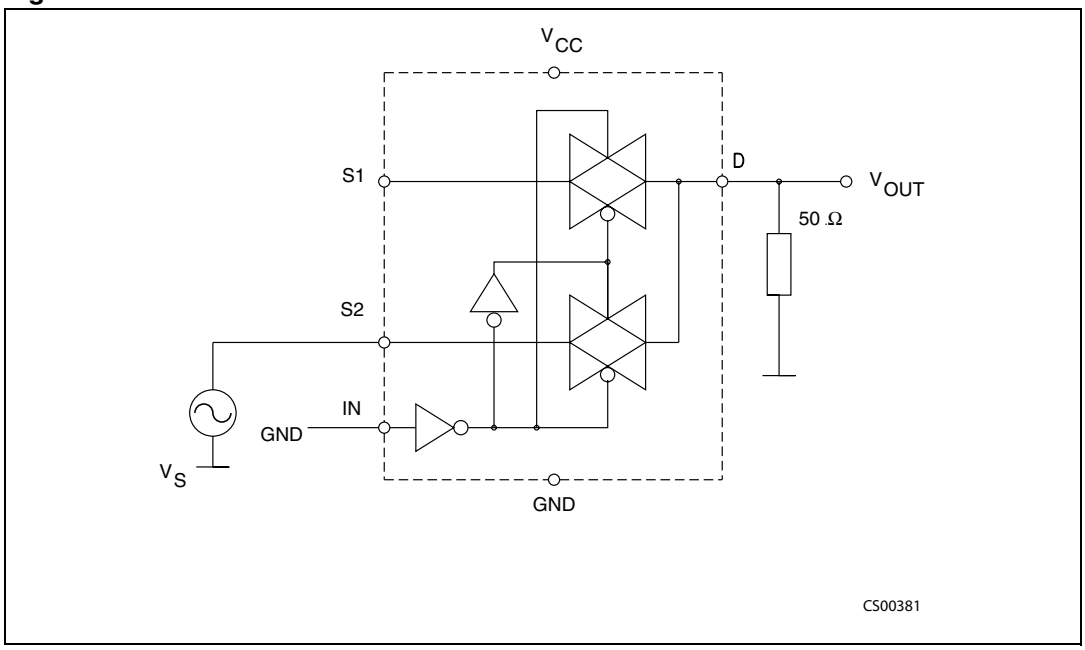


Figure 7. Bandwidth

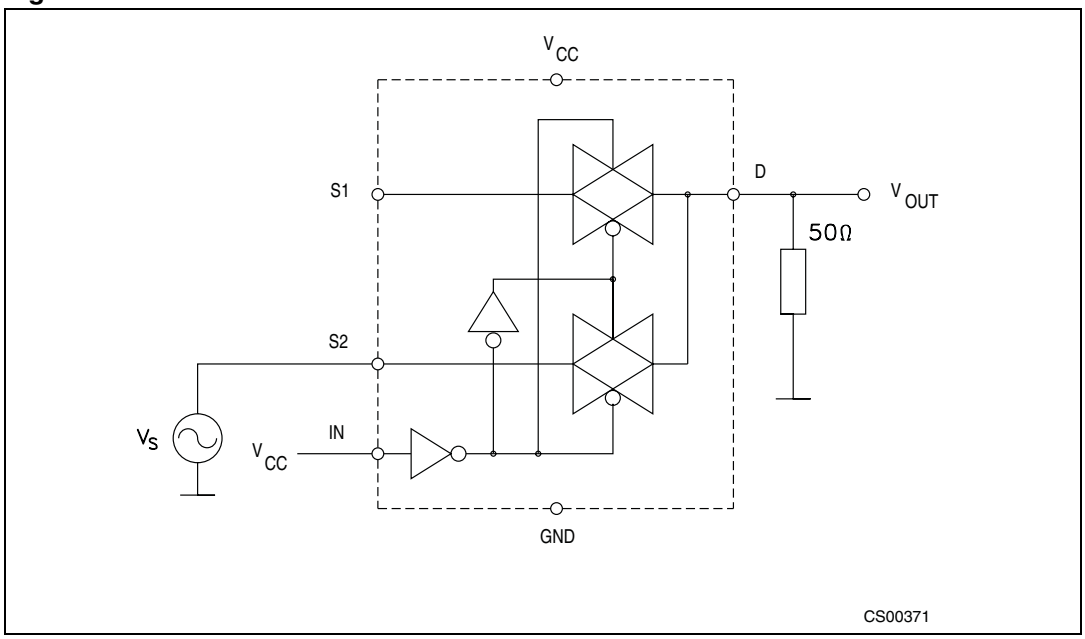


Figure 8. Channel-to-channel crosstalk

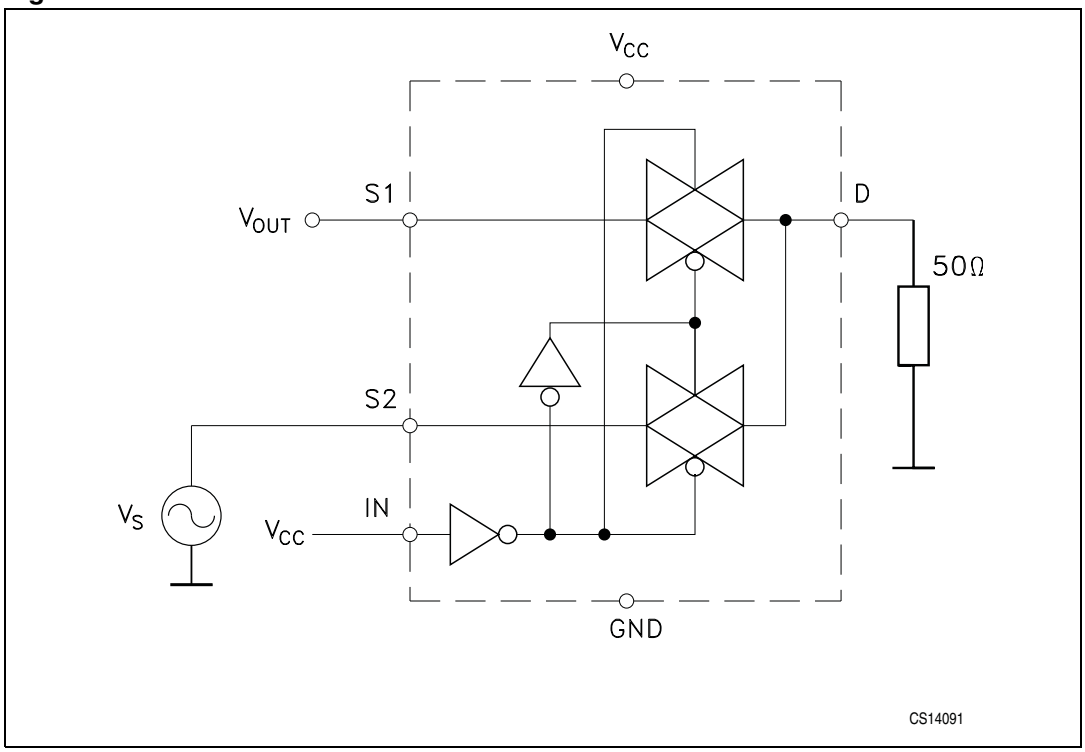
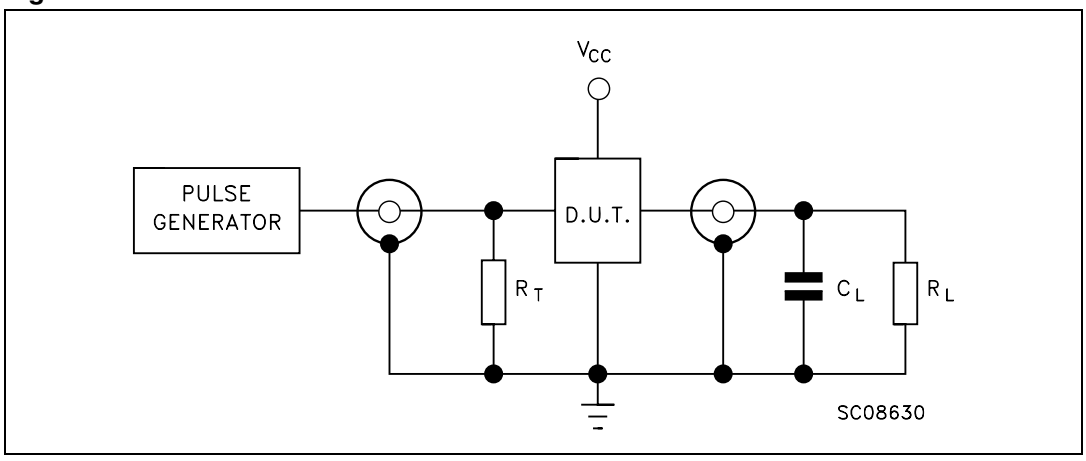


Figure 9. Test circuit



2. C_L = 5/35 pF or equivalent (includes jig and probe capacitance)
3. R_L = 50 Ω or equivalent
4. $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 10. Break-before-make time delay

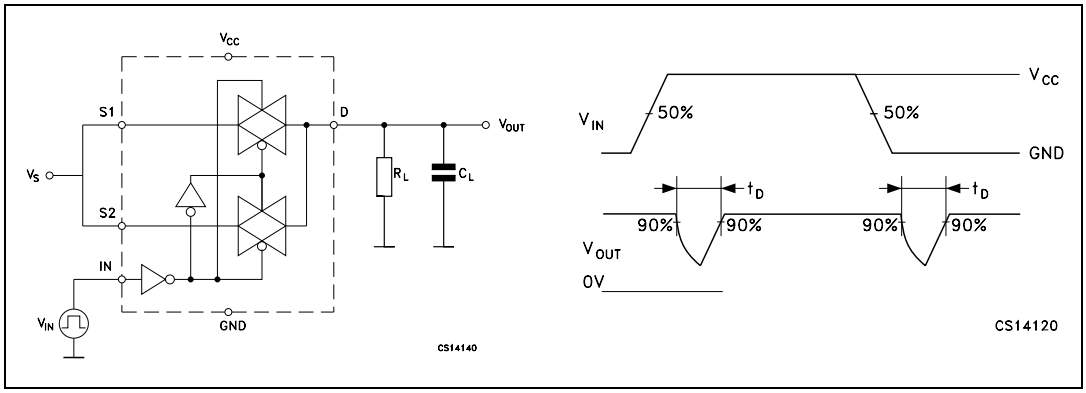


Figure 11. Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

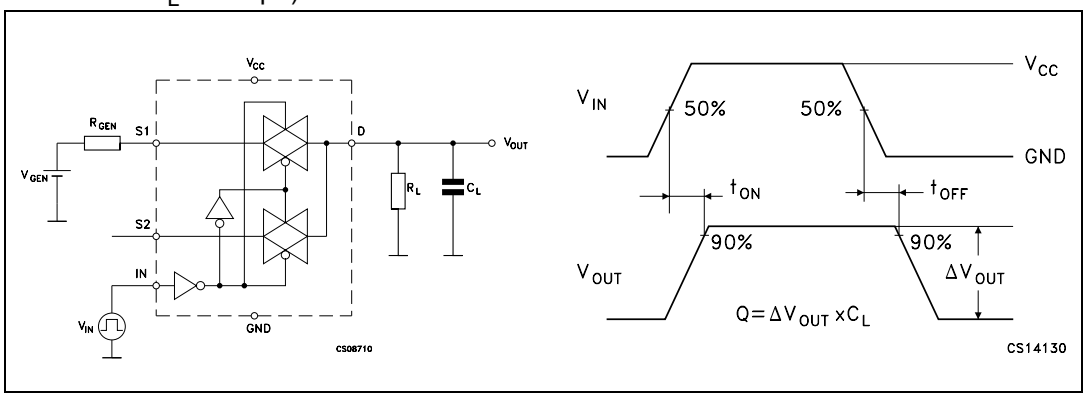
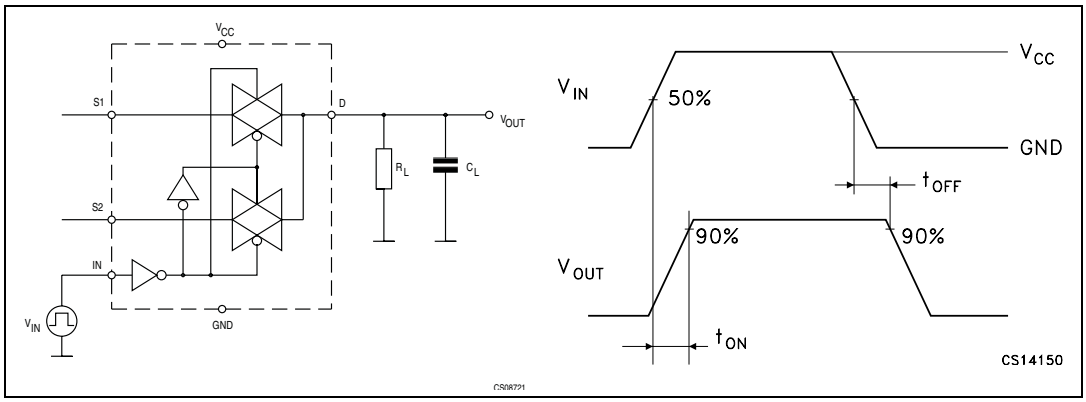


Figure 12. Turn on, turn off delay time



6 Application hint

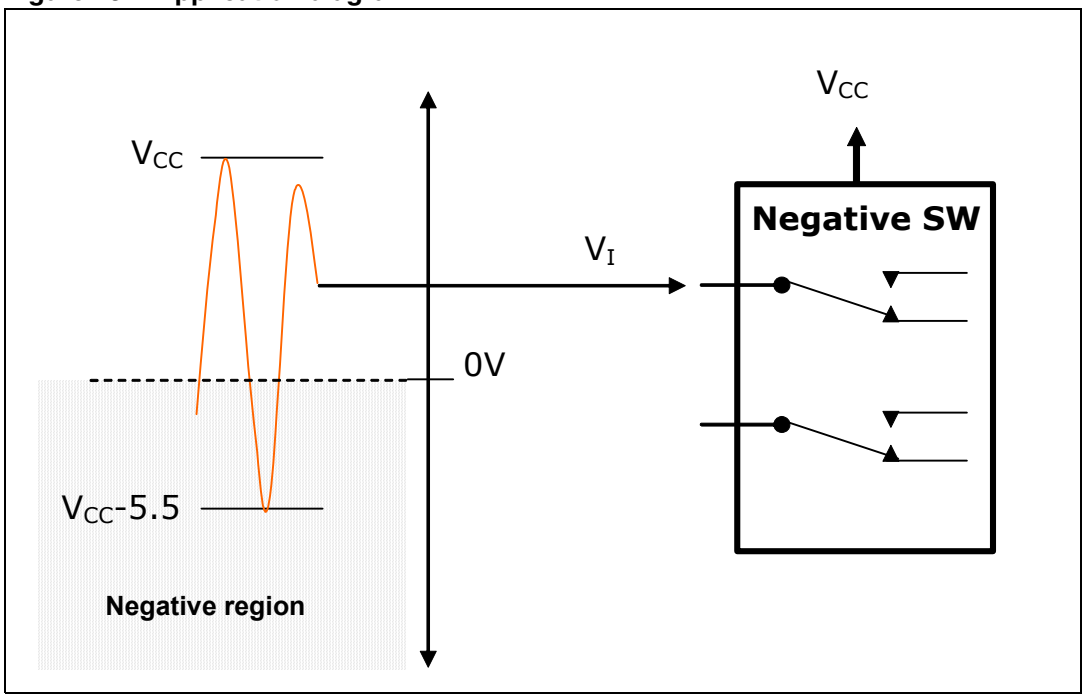
6.1 Input signal dynamic range

The STG5678 negative analog switch allows input signals that fall below 0 V to pass through the switch without signal distortion. The input signal dynamic range VI consists of a positive-region and a negative-region.

The positive-region is limited by the level of V_{CC}. The negative-region is limited by the difference between V_{CC} and 5.5 V. The effect of this is that, the higher the V_{CC}, the smaller the operating range in the negative region.

For example, if V_{CC} = 3.6 V, the input signal dynamic range is from -1.9 V to 3.6 V.

Figure 13. Application diagram



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. Package outline for Flip-chip 12

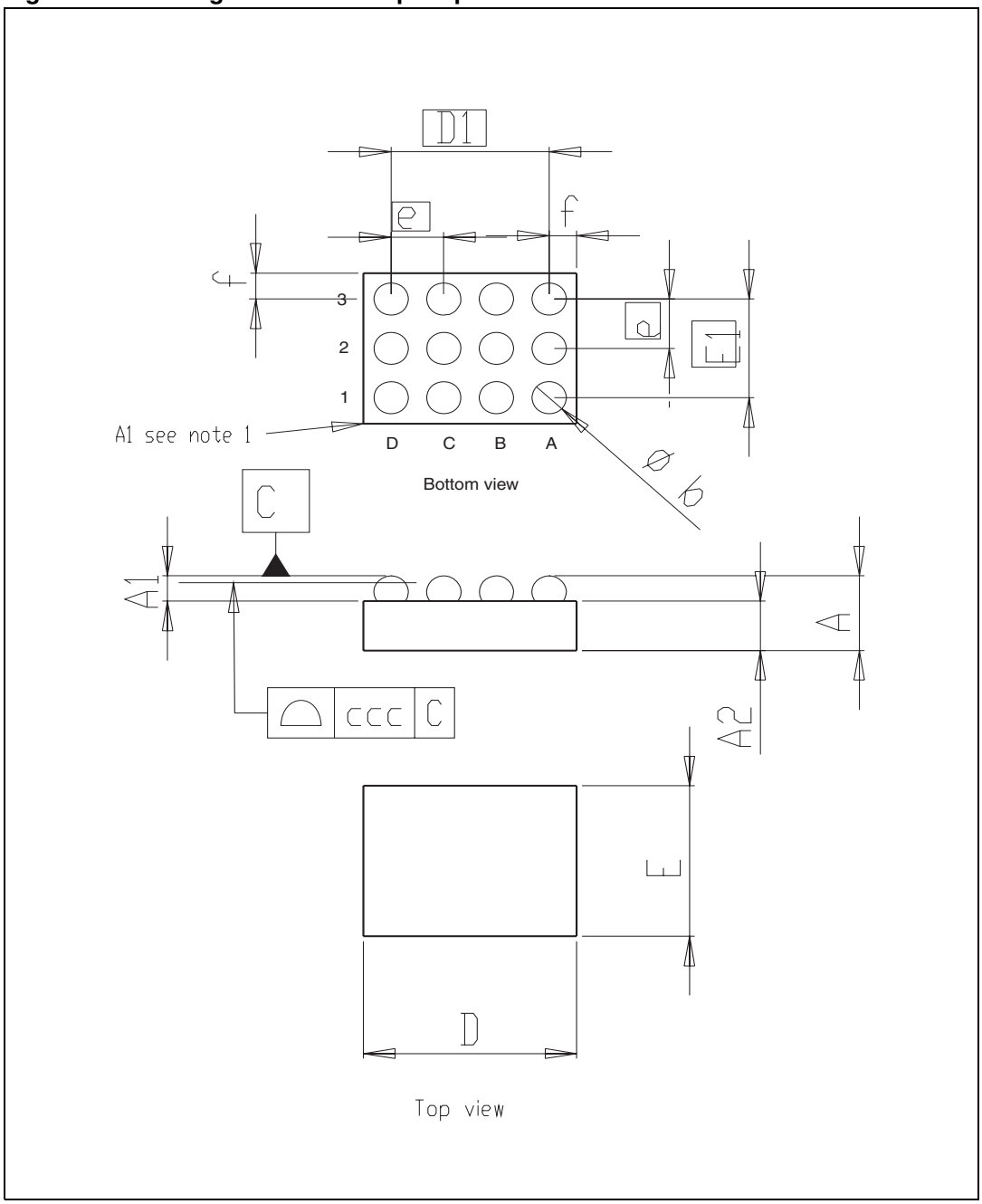


Table 9. Mechanical data for Flip-chip 12

Symbol	Millimeters		
	Min	Typ	Max
A	0.55	0.605	0.66
A1	0.17	0.205	0.24
A2	0.38	0.4	0.42
b	0.215	0.255	0.295
D	1.568	1.598	1.628
D1	–	1.2	–
E	1.168	1.198	1.228
E1	–	0.8	–
e	0.36	0.4	0.44
f	0.189	0.199	0.209
ccc	–	0.05	–

Figure 15. Footprint recommendation

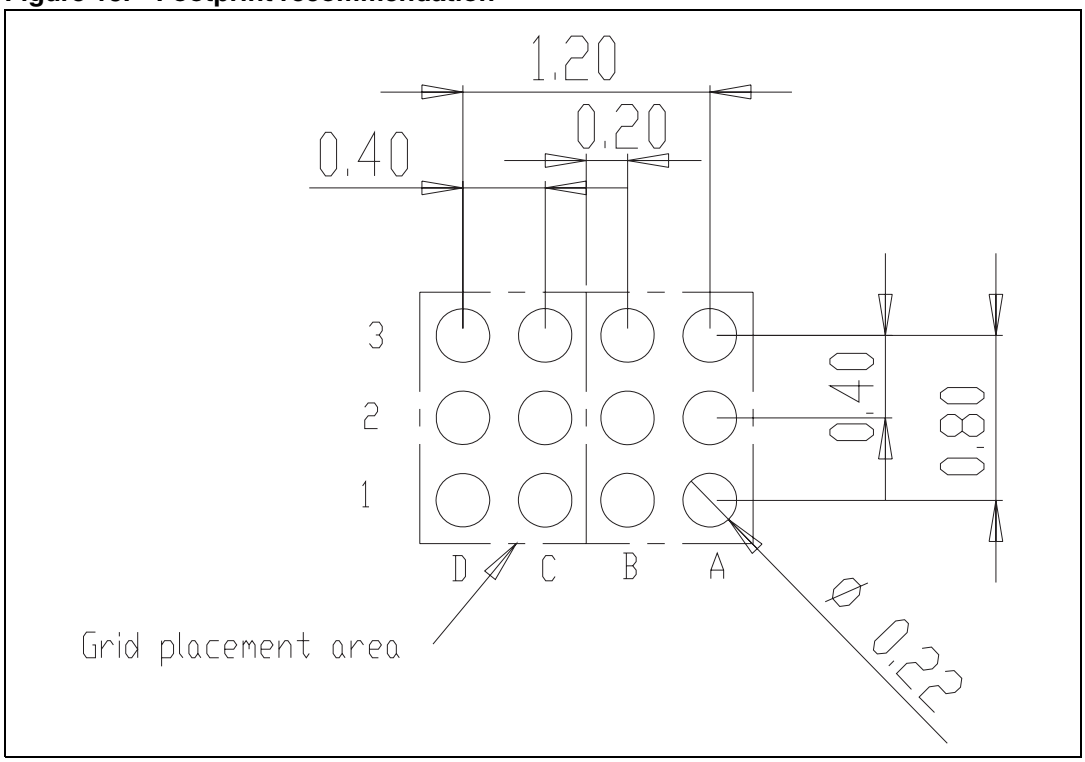


Figure 16. Package outline for Flip-chip 12 with back side coating

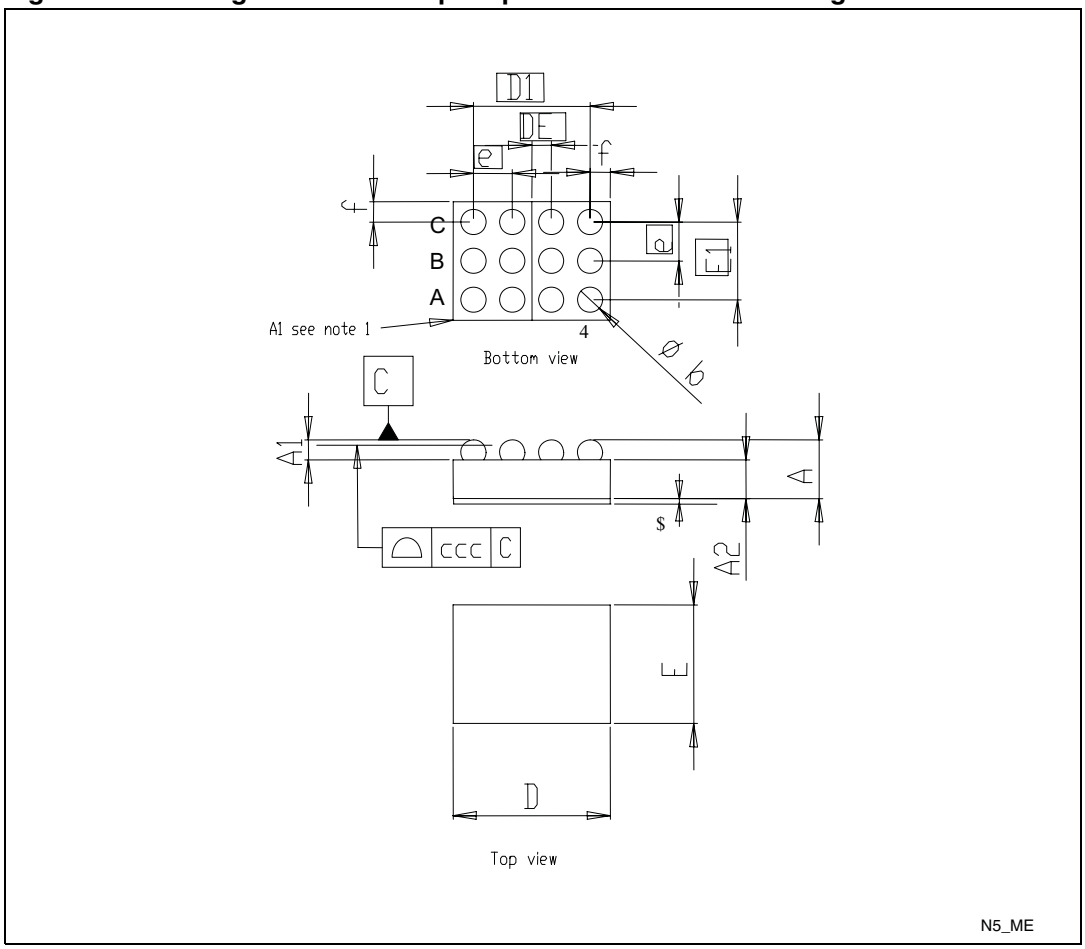


Table 10. Mechanical data for Flip-chip 12 with back side coating

Symbol	Millimeters		
	Min	Typ	Max
A	0.595	0.65	0.705
A1	0.165	0.20	0.235
A2	0.38	0.4	0.42
b	0.215	0.255	0.295
D	1.568	1.598	1.628
D1	–	1.2	–
E	1.168	1.198	1.228
E1	–	0.8	–
e	0.36	0.4	0.44
f	0.189	0.199	0.209
ccc	–	0.05	–

Figure 17. Footprint recommendation

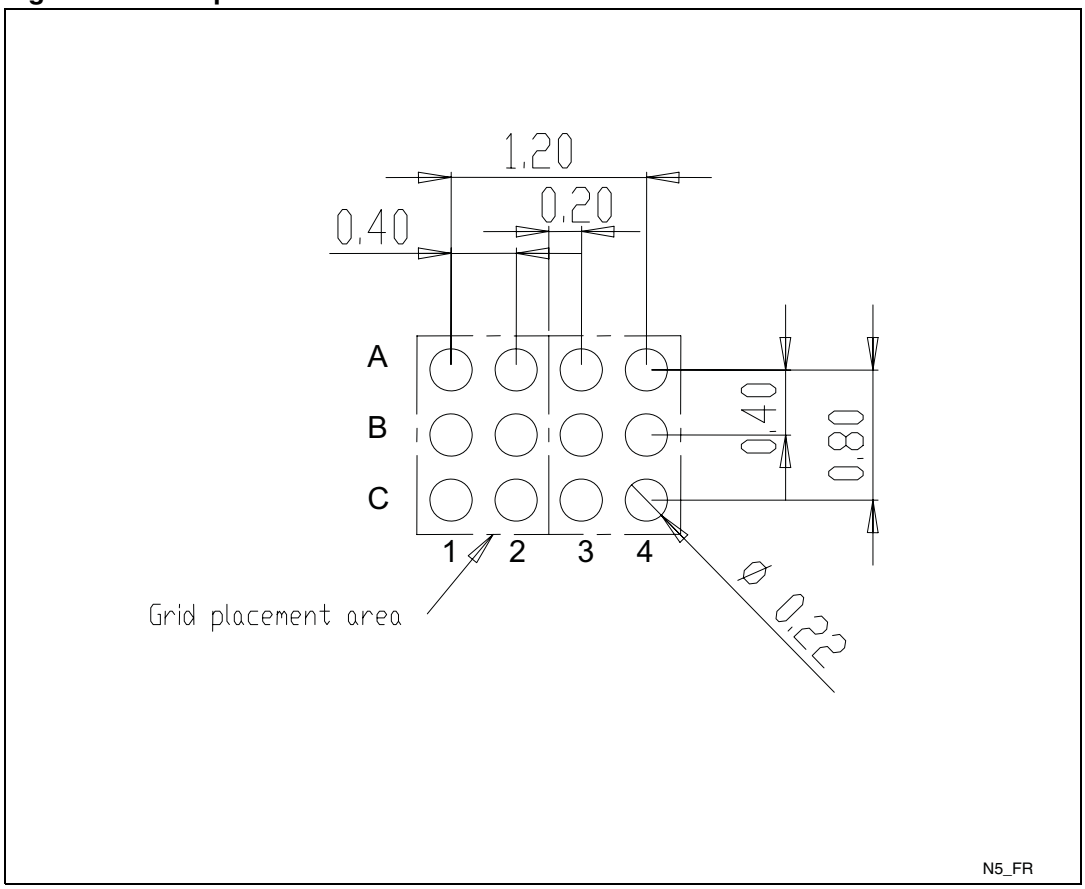


Figure 18. Tape information

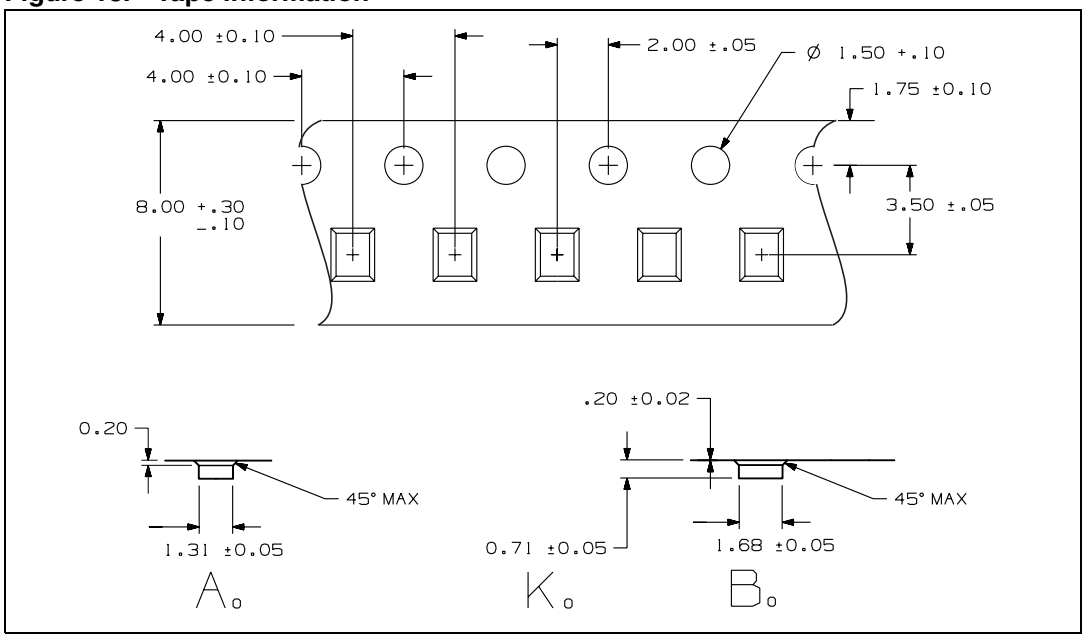


Figure 19. Tape orientation

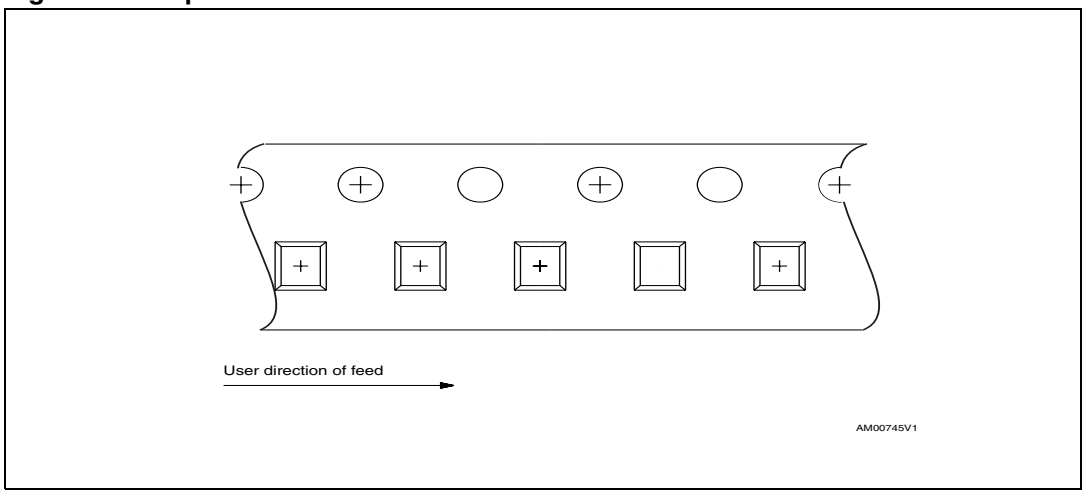
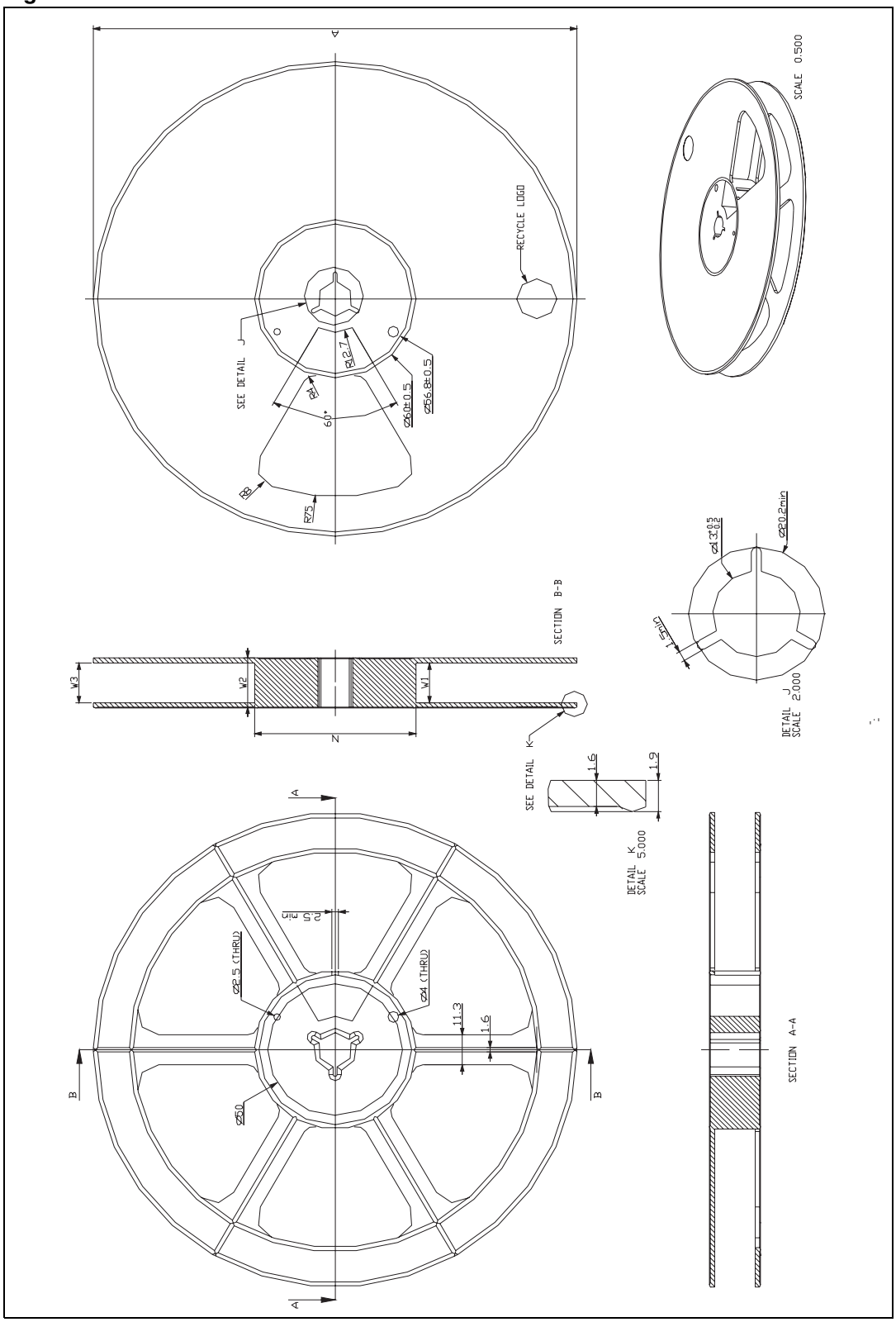


Table 11. Reel measurement

Tape width (mm)	A	N	W1		W2	W3	
	Max	Min			Max	Min	Max
8	180	54	8.4	+1.5/-0	14.4	7.9	10.9

Figure 20. Reel information



8 Revision history

Table 12. Document revision history

Date	Revision	Changes
01-Apr-2008	1	Initial release.
10-Sep-2008	2	Document status promoted from preliminary data to datasheet. Modified: *Figure 19 on page 20*. Updated: *Table 9 on page 17*.
04-Jun-2010	3	Added: Flip-chip 12 with back side coating. Document reformatted.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com