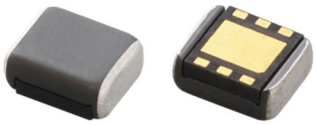
"PicoBK™" MYRGP-W/B-RF 0.6A series

Inductor Built-in Step-Down "mini DC/DC" Converters

☆Green Operation Compatible

■GENERAL DESCRIPTION



The MYRGP-W/B series is a synchronous step-down mini DC/DC converter which integrates an inductor and a control IC in one tiny package (2.5mm×2.0mm, H=1.0mm). A stable power supply with an output current of 600mA is configured using only two capacitors connected externally. Operating voltage range is from 1.8V to 6.0V.
Output voltage is adjustable from 0.9V to 4.0V by an external resistor divider.
The device is operated by 3.0MHz, and includes 0.42Ω P-channel driver transistor and 0.52Ω N-channel switching transistor. As for operation mode, the MYRGP-W series is PWM control, the MYRGP-B series is automatic PWM/PFM switching control.
During stand-by, the device is shutdown to reduce current consumption to as low as 1.0μA or less. With the built-in UVLO (Under Voltage Lock Out) function, the internal driver transistor is forced OFF when input voltage becomes 1.4V or lower.
MYRGP-x-RF series provide short-time turn-on by the soft start function internally set in 0.25ms (TYP).
MYRGP-x-RF integrate C_L auto discharge function which enables the electric charge stored at the output capacitor C_L to be discharged via the internal auto-discharge switch located between the L_X and V_{SS} pins.
When the devices enter stand-by mode, output voltage quickly returns to the V_{SS} level as a result of this function.

■APPLICATIONS

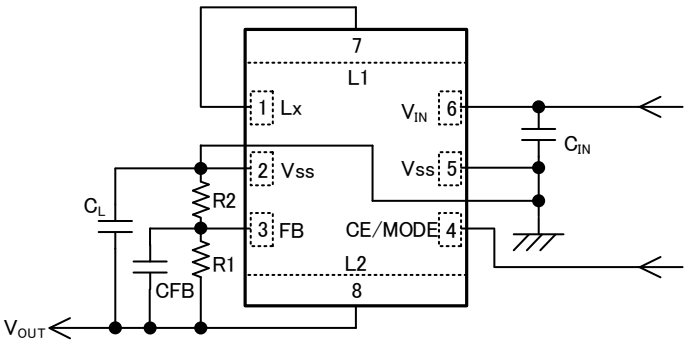
- ●Mobile phones, Smart phones
- ●Bluetooth Headsets
- ●WiMAX PDAs, MIDs, UMPCs
- ●Portable game consoles
- ●Digital cameras, Camcorders
- ●Electronic dictionaries

■FEATURES

Ultra-Small	: 2.5mm×2.0mm, H=1.0mm
Input Voltage	: 1.8V ~ 6.0V
Output Voltage	: 0.9V ~ 4.0V (±2.0%)
High Efficiency	: 90% (V_{IN}=4.2V, V_{OUT}=3.3V)
Output Current	: 600mA
Oscillation Frequency	: 3.0MHz (±15%)
Maximum Duty Cycle	: 100%
Capacitor	: Low ESR Ceramic
CE Function	: Active High Soft-Start Circuit Built-In C_L High Speed Auto Discharge
Protection Circuits	:Current Limiter Circuit Built-In (Constant Current & Latching)
Control Methods	: PWM (MYRGP-W) PWM/PFM Auto (MYRGP-B)
Operating Ambient Temperature	: -40℃ ~ 85℃
Environmentally Friendly	: EU RoHS Compliant, Pb Free Halogen Free

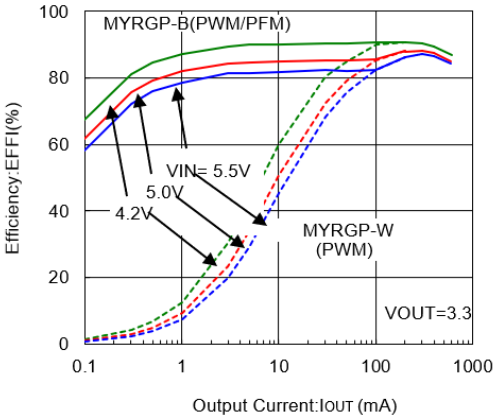
■TYPICAL APPLICATION CIRCUIT

MYRGP-x-RF Series



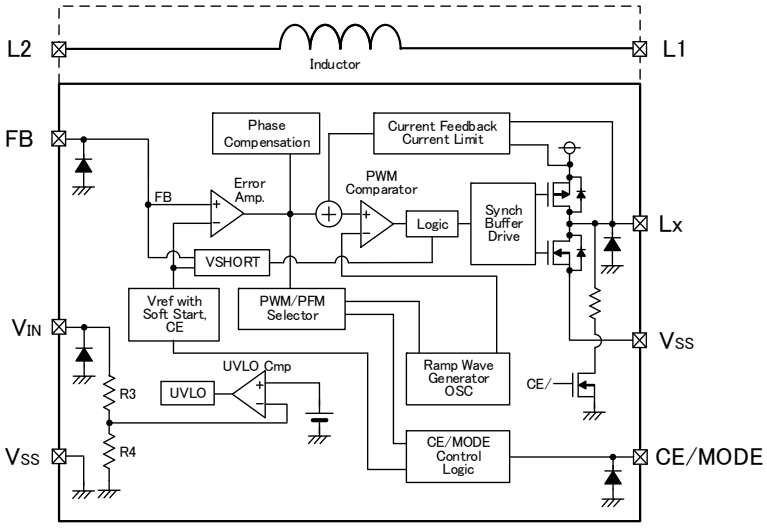
■TYPICAL PERFORMANCE CHARACTERISTICS

MYRGP080060x21RF



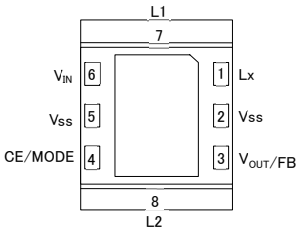
■BLOCK DIAGRAM

3) MYRGP-x-RF series



NOTE: The MYRGP-W offers a fixed PWM control, a signal from CE/MODE Control Logic to PWM/PFM Selector is fixed to "L" level inside. The MYRGP-B control scheme is PWM/PFM automatic switching, a signal from CE/MODE Control Logic to PWM/PFM Selector is fixed to "H" level inside. The diodes placed inside are ESD protection diodes and parasitic diodes.

■PIN CONFIGURATION



(BOTTOM VIEW)

* It should be connected the Vss pin (No. 2 and 5) to the GND pin.
* If the dissipation pad needs to be connected to other pins, it should be connected to the GND pin.
* Please refer to pattern layout page for the connecting to PCB.

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	L_X	Switching Output
2,5	V_{SS}	Ground
3	FB	Output Voltage Sense Pin
4	CE / MODE	Chip Enable & Mode Switch
6	V_{IN}	Power Input
7	L1	Inductor Electrodes
8	L2	

■FUNCTION

CE/MODE	OPERATIONAL STATES	
	MYRGP-W	MYRGP-B
H Level (*1)	Synchronous PWM Fixed Control	Synchronous PWM/PFM Automatic Switching
L Level (*2)	Stand-by	Stand-by

※series CE/MODE pin voltage level range
(*1)H Level :0.65V ≦ H Level ≦ 6V (MYRGP-W/B)
(*2)L Level :0V ≦ L Level ≦ 0.25V

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage	V_{IN}	-0.3 ~ 6.5	V
L_X Pin Voltage	VL_X	-0.3 ~ V_{IN} + 0.3	V
V_{FB} Pin Voltage	V_{FB}	-0.3 ~ 6.5	V
CE/MODE Pin Voltage	V_{CE}	-0.3 ~ 6.5	V
L_X Pin Current	IL_X	±1500	mA
Power Dissipation(Ta=25℃)	Pd	1000 (40mm x 40mm Standard board) (*1)	mW
Operating Ambient Temperature	Topr	-40 ~ 85	℃
Storage Temperature	Tstg	-40 ~ 125	℃

(*1) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS (Continued)

●MYRGP-x-RF

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
FB Voltage	V_{FB}	V_{IN}=V_{CE}=5.0V, V_{FB} voltage which Decrease V_{FB} from 0.9V, Lx becomes "H" (*10) level	0.784	0.800	0.816	V	③
Operating Voltage Range	V_{IN}		1.8	-	6.0	V	⑪
Maximum Output Current	I_{OUTMAX}	V_{IN}=$V_{OUT(T)}$+2.0V, V_{CE}=1.0V When connected to external components (*8)	600	-	-	mA	⑪
UVLO Voltage	V_{UVLO}	V_{CE}=V_{IN},V_{FB}= 0.4V, Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	③
Supply Current (MYRGP-W)	I_{DD}	V_{IN} =V_{CE}=5.0V, V_{FB}= 0.88V	-	46	65	μA	②
Supply Current (MYRGP-B)			-	21	35		
Stand-by Current	I_{STB}	V_{IN} =5.0V, V_{CE}=0V, V_{FB}= 0.88V	-	0	1.0	μA	②
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN} =3.2V, V_{CE}=1.0V, I_{OUT}=100mA	2550	3000	3450	kHz	⑪
PFM Switching Current (*11)	I_{PFM}	When connected to external components, V_{IN} =3.2V, V_{CE} = V_{IN} , I_{OUT}=1mA	170	220	270	mA	⑫
PFM Duty Limit (*11)	DTY_{LIMIT_PFM}	V_{CE}= V_{IN} = 2.2V, I_{OUT}=1mA	-	200	300	%	⑪
Maximum Duty Cycle	MAXDTY	V_{IN} = V_{CE} =5.0V, V_{FB} = 0.72V	100	-	-	%	③
Minimum Duty Cycle	MINDTY	V_{IN} = V_{CE} =5.0V, V_{FB} = 0.88V	-	-	0	%	③
Efficiency(*2)	EFFI	When connected to external components, V_{CE} = V_{IN} = 2.4V, I_{OUT} = 100mA	-	86	-	%	⑪
Lx SW "H" ON Resistance 1	$R_{Lx H}$	V_{IN} = V_{CE} = 5.0V, V_{FB} = 0.72V,IL_X = 100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	$R_{Lx H}$	V_{IN} = V_{CE} = 3.6V, V_{FB} = 0.72V,IL_X = 100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	$R_{Lx L}$	V_{IN} = V_{CE} = 5.0V (*4)	-	0.45	0.65	Ω	-
Lx SW "L" ON Resistance 2	$R_{Lx L}$	V_{IN} = V_{CE} = 3.6V (*4)	-	0.52	0.77	Ω	-
Lx SW "H" Leakage Current (*5)	I_{LEAKH}	V_{IN}= V_{FB} =5.0V, V_{CE} =0V, L_X=0V	-	0.01	1.0	μA	⑨
Current Limit (*9)	I_{LIM}	V_{IN} = V_{CE}= 5.0V, V_{FB} = 0.72V (*7)	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	ΔV_{OUT}/ (V_{OUT}・ΔTopr)	I_{OUT} =30mA -40℃≦Topr≦85℃	-	±100	-	ppm/ ℃	⑪
CE "H" Voltage	V_{CEH}	V_{FB}=0.72V, Applied voltage to V_{CE}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
CE "L" Voltage	V_{CEL}	V_{FB}=0.72V, Applied voltage to V_{CE}, Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
CE "H" Current	I_{CEH}	V_{IN} = V_{CE} =5.0V, V_{FB} = 0.72V	- 0.1	0.0	0.1	μA	⑤
CE "L" Current	I_{CEL}	V_{IN} =5.0V, V_{CE} = 0V, V_{FB} = 0.72V	- 0.1	0.0	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{CE}=0V→V_{IN} , I_{OUT}=1mA	-	0.25	0.40	ms	⑪
Latch Time	t_{LAT}	V_{IN}=V_{CE}=5.0V, V_{FB}=0.64 Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	V_{IN}=V_{CE}=5.0V, V_{FB} voltage which Decrease V_{FB} from 0.4V, Lx becomes "L" (*10)level within 1ms	0.15	0.20	0.25	V	⑦
C_L Discharge	R_{DCHG}	V_{IN} = 5.0V L_X = 5.0V V_{CE} = 0V, V_{FB} = open	200	300	450	Ω	⑧
Inductance Value	L	Test frequency=1MHz	-	1.5	-	μH	-
Allowed Inductor Current	I_{DC}	ΔT=40℃	-	1000	-	mA	-

Test conditions: V_{OUT}=1.2V when the external components are connected. Unless otherwise stated, V_{IN}=5.0V, applied voltage sequence is V_{FB}→V_{IN}→V_{CE}

NOTE:

(*1) Including hysteresis operating voltage range.

(*2) EFFI = { (output voltage × output current) / (input voltage × input current) } × 100

(*3) ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA

(*4) Design value

(*5) When temperature is high, a current of approximately 10μA (maximum) may leak.

(*6) Time until it short-circuits V_{FB} with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

(*7) When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.

(*8) When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

(*9) Current limit denotes the level of detection at peak of coil current.

(*10)"H"=V_{IN}~V_{IN}-1.2V, "L"=+0.1V~-0.1V

(*11) I_{PFM} and DTY_{LIMIT_PFM} are defined only for the MYRGP-B series which have PFM control function. (Not for the MYRGP-W series)

■TEST CIRCUITS

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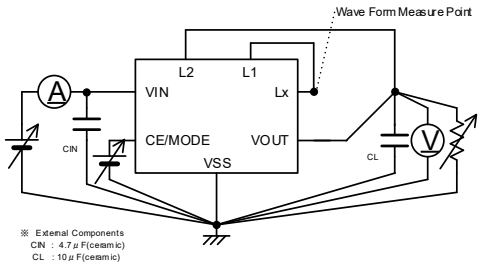
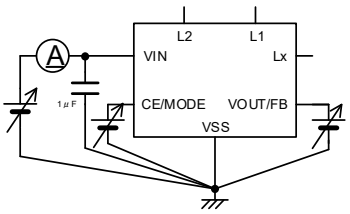


※ External Components
CIN : 4.7μF(ceramic)
CL : 10μF(ceramic)

< Circuit No.2 >



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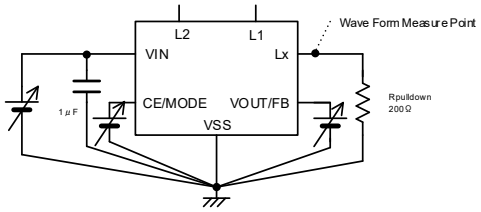

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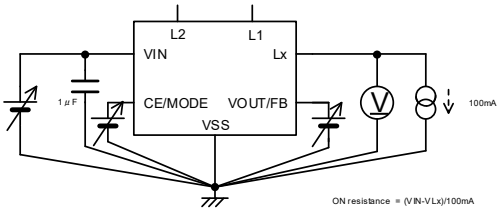

ON resistance = (VIN-VLx)/100mA

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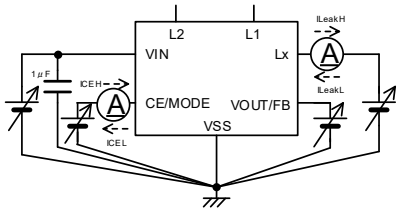

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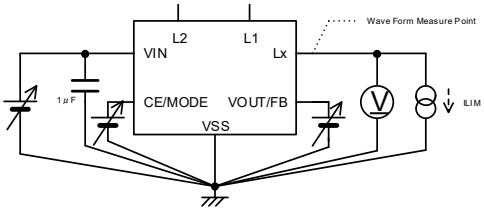

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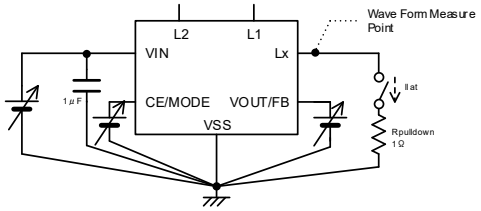

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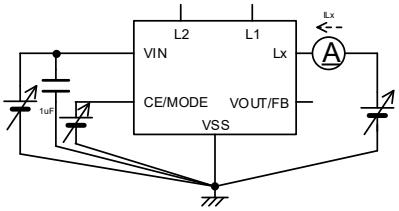

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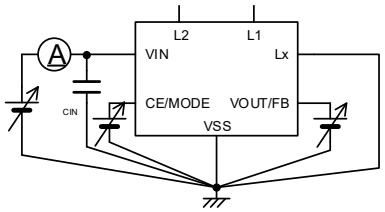

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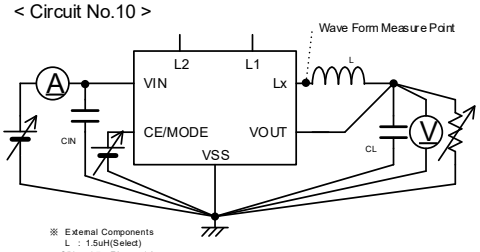
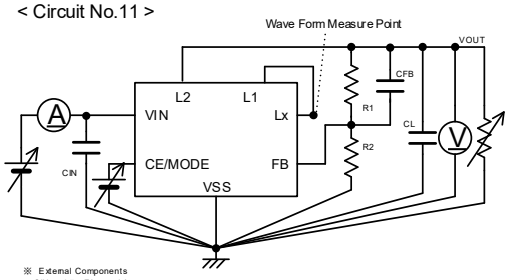


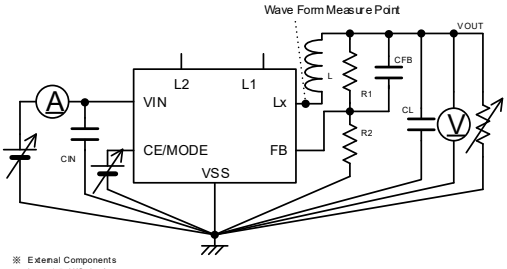
※ External Components
L : 1.5uH(Select)
CIN : 4.7μF(ceramic)
CL : 10μF(ceramic)

< Circuit No.11 >



※ External Components
CIN : 4.7μF(ceramic)
CL : 10μF(ceramic)
R1 : 150kΩ
R2 : 300kΩ
CFB : 100pF(ceramic)
※VOUT(T)=1.2V

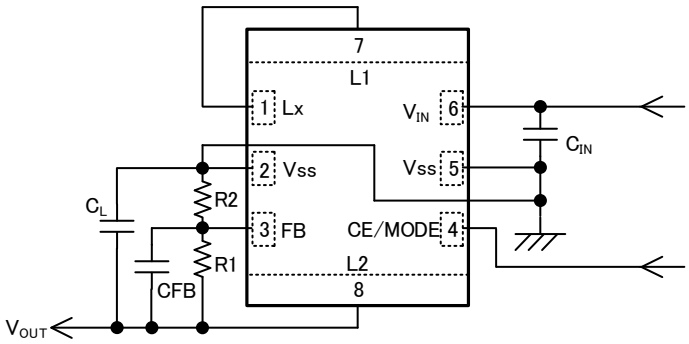
< Circuit No.12 >



※ External Components
L : 1.5uH(Select)
CIN : 4.7μF(ceramic)
CL : 10μF(ceramic)
R1 : 150kΩ
R2 : 300kΩ
CFB : 100pF(ceramic)
※VOUT(T)=1.2V

■TYPICAL APPLICATION CIRCUIT

● MYRGP-x-RF Series



● External Components

CIN : 10V/4.7μF(Ceramic)
C_L : 6.3V/10μF(Ceramic)
R1 : 300kΩ
R2 : 240kΩ
CFB : 150pF
NOTE
The Inductor can be used only for this DC/DC converter.
Please do not use this inductor for the other reasons.
Please use B, X5R, and X7R grades in temperature characteristics for CIN and CL capacitors.
These grade ceramic capacitors minimize capacitance-loss as a function of voltage stress.

< MYRGP-x-RF output voltage setting>

The output voltage can be set by adding external dividing resistors. The output voltage is determined by R1 and R2 in the equation below. The sum of R1 and R2 is normally kept 1MΩor less. The output voltage range can be set from 0.9V to 4.0V based on the 0.8V ±2.0% reference voltage source.

Note that when the input voltage (V_{IN}) is less than or equal to the set output voltage, an output voltage (V_{OUT}) higher than the input voltage (V_{IN}) cannot be output.

$V_{OUT}=0.8\times (R1+R2)/R2$

Adjust the value of the phase compensation speedup capacitor CFB so that fzfb=1/ (2×π×CFB×R1) is 10 kHz or less. It is optimum to adjust to a value from 1kHz to 20kHbased on the components used and the board layout.

[Calculation example]
When R1=470kΩ, R2=150kΩ,
V_{OUT}=0.8× (470k+150k)/150k=3.3V

●V_{OUT} setting example

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	CFB(pF)
0.9	100	820	150
1.2	150	300	100
1.5	130	150	220
1.8	300	240	150
2.5	510	240	100
3.0	330	120	150
3.3	470	150	100
4.0	120	30	470

■OPERATIONAL DESCRIPTION

The MYRGP-W/B series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOSFET driver transistor, N-channel MOSFET switching transistor for the synchronous switch, current limiter circuit, UVLO circuit with control IC, and an inductor. (See the block diagram above.)

Using the error amplifier, the voltage of the internal voltage reference source is compared with the feedback voltage from the V_{OUT} pin through split resistors, R1 and R2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage.

The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor such as a ceramic capacitor is used ensuring stable output voltage.

<Reference Voltage Source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>

The ramp wave circuit determines switching frequency. The frequency is fixed internally 3.0MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R1 and R2. When a feedback voltage is lower than the reference voltage, the output voltage of the error amplifier is increased. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

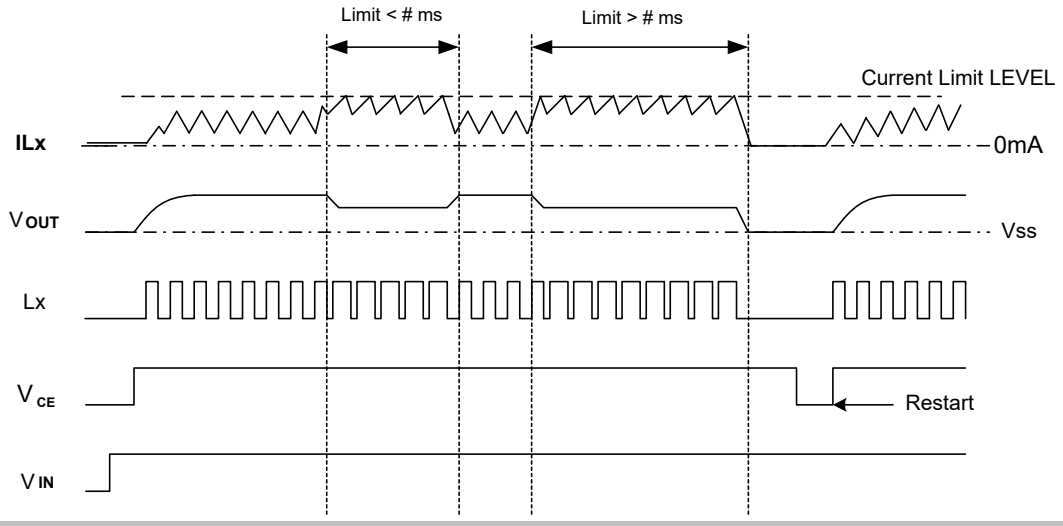
<Current Limit>

The current limiter circuit of the MYRGP-W/B series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the operation suspension mode.

① When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing.
② When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③ At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
④ When the over current state is eliminated, the IC resumes its normal operation.

The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for a few milliseconds and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor, and goes into operation suspension state. Once the IC is in suspension state, operations can be resumed by either turning the IC off via the CE/MODE pin, or by restoring power to the V_{IN} pin. The suspension state does not mean a complete shutdown, but a state in which pulse output is suspended; therefore, the internal circuitry remains in operation. The current limit of the MYRGP-W/B series can be set at 1050mA at typical.

Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, an input capacitor is placed as close to the IC as possible.



■OPERATIONAL DESCRIPTION (Continued)

<Short-Circuit Protection>

The short-circuit protection circuit monitors the internal R1 and R2 divider voltage from the V_{OUT} pin (refer to FB point in the block diagram shown in the previous page). In case where output is accidentally shorted to the Ground and when the FB point voltage decreases less than half of the reference voltage (Vref) and a current more than the I_{LIM} flows to the driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor. For the G/F series, it does not matter how much the current limit, once the FB voltage become less than the quarter of reference voltage (VREF), the short-circuit protection operates to latch the Pch MOS driver transistor

In the latch state, the operation can be resumed by either turning the IC off and on via the CE/MODE pin, or by restoring power supply to the V_{IN} pin.

When sharp load transient happens, a voltage drop at the V_{OUT} is propagated to the FB point through C_{FB}, as a result, short circuit protection may operate in the voltage higher than 1/2 V_{OUT} voltage.

<UVLO Circuit>

When the V_{IN} pin voltage becomes 1.4V or lower, the P-channel output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage becomes 1.8V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the V_{IN} pin voltage falls momentarily below the UVLO operating voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

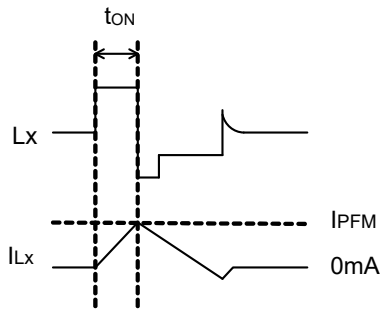
<PFM Switch Current>

In PFM control operation, until coil current reaches to a specified level (I_{PFM}), the IC keeps the P-ch MOSFET on. In this case, on-time (t_{ON}) that the P-ch MOSFET is kept on can be given by the following formula.

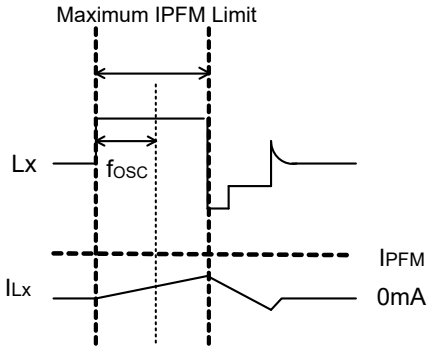
$$t_{ON} = L \times I_{PFM} / (V_{IN} - V_{OUT}) \quad \rightarrow I_{PFM}①$$

<PFM Duty Limit>

In the PFM control operation, the PFM Duty Limit (DTY_{LIMIT_PFM}) is set to 200% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-down ratio is small), it's possible for P-ch MOSFET to be turned off even when coil current doesn't reach to I_{PFM}. →I_{PFM}②



I_{PFM}①



I_{PFM}②

■OPERATIONAL DESCRIPTION (Continued)

＜C_L High Speed Discharge＞

The MYRGP-x-RF series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the L_X pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R] and an output capacitor value (C_L) as τ (τ =C x R), discharge time of the output voltage after discharge via the N channel transistor is calculated by the following formula.

$V = V_{OUT(T)} \times e^{-t/\tau}$ or $t = \tau \ln (V_{OUT(T)} / V)$

V : Output voltage after discharge

$V_{OUT(T)}$: Output voltage

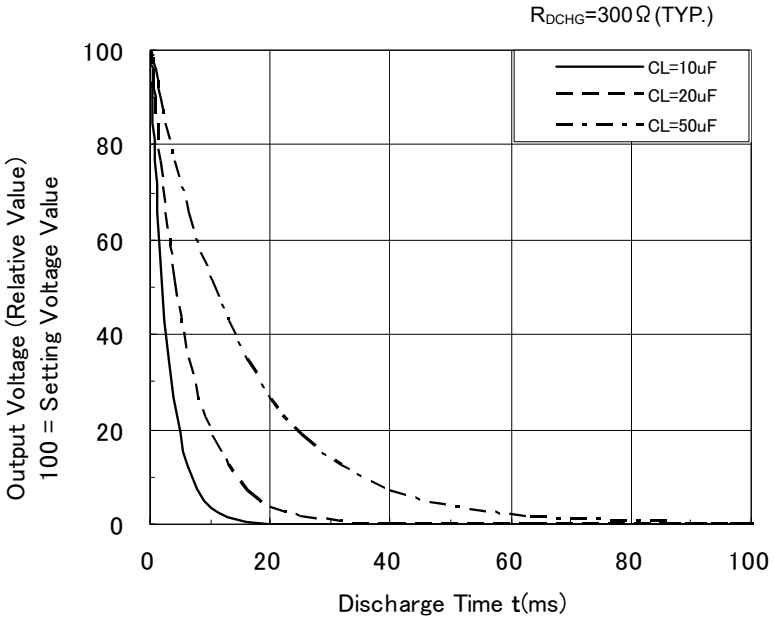
t: Discharge time,

τ : C x R

C= Capacitance of Output capacitor (C_L)

R= C_L auto-discharge resistance

Output Voltage Discharge Characteristics

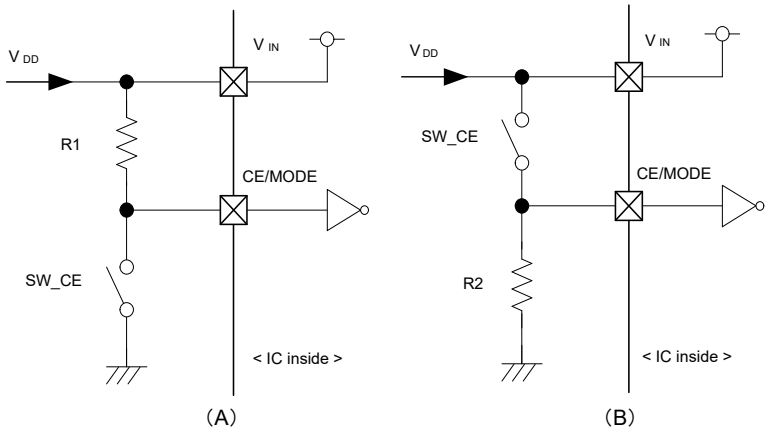


■OPERATIONAL DESCRIPTION (Continued)

<CE/MODE Pin Function>

The operation of the MYRGP-W/B series will enter into the shutdown mode when a low level signal is input to the CE/MODE pin. During the shutdown mode, the current consumption of the IC becomes 0μA (TYP.), with a state of high impedance at the Lx pin and VOUT pin. The IC starts its operation by inputting a high level signal to the CE/MODE pin. The input to the CE/MODE pin is a CMOS input and the sink current is 0μA (TYP.).

●MYRGP-W/B series - Examples of how to use CE/MODE pin



(A)

SW_CE	SELECTED STATUS
ON	Stand-by
OFF	Operation

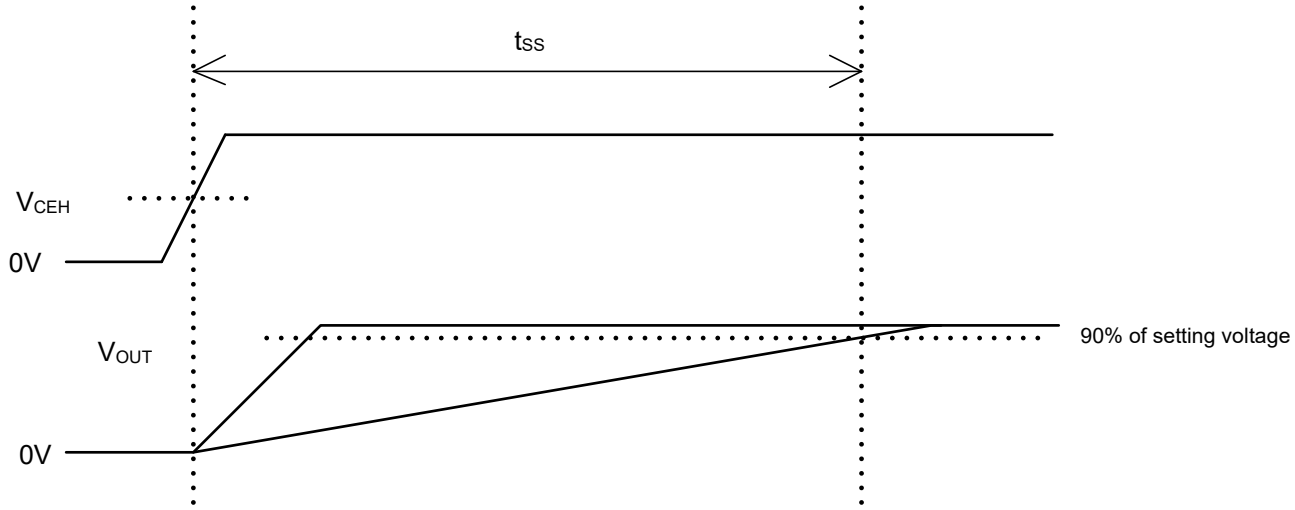
(B)

SW_CE	SELECTED STATUS
ON	Operation
OFF	Stand-by

■OPERATIONAL DESCRIPTION (Continued)

〈Soft Start〉

The MYRGP-x-RF series provide 0.32ms (TYP) however, when V_{OUT} is less than 1.8V, provide 0.25ms (TYP.). Soft start time is defined as the time to reach 90% of the output nominal voltage when the CE pin is turned on.



■FUNCTION CHART

CE/MODE VOLTAGE LEVEL	OPERATIONAL STATES	
	MYRGP-W	MYRGP-B
H Level (*1)	Synchronous PWM Fixed Control	Synchronous PWM/PFM Automatic Switching
L Level (*2)	Stand-by	Stand-by

Note on CE/MODE pin voltage level range
(*1) H level: 0.65V ≦ H level ≦ 6V (for MYRGP-W/B)
(*2) L level: 0V ≦ L level ≦ 0.25V

■NOTE ON USE

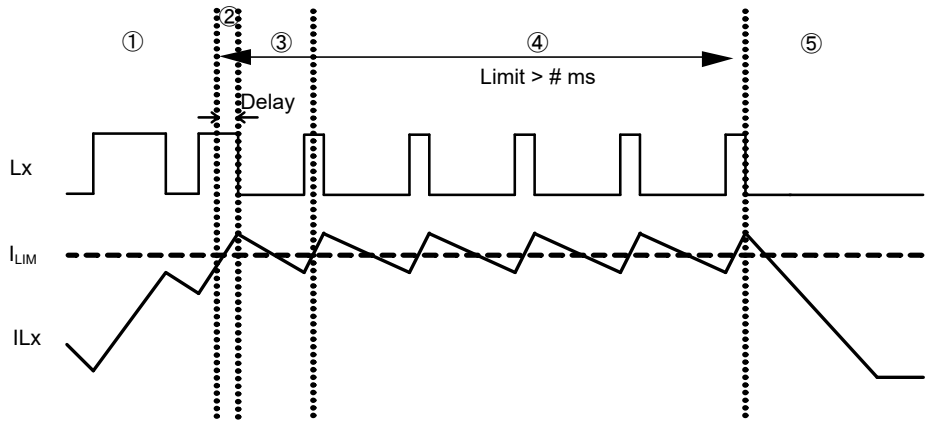
1. The MYRGP-W/B series is designed for use with ceramic output capacitors. If, however, the potential difference is too large between the input voltage and the output voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.
2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.
3. Depending on the input-output voltage differential, or load current, some pulses may be skipped, and the ripple voltage may increase.
4. When the difference between V_{IN} and V_{OUT} is large in PWM control, very narrow pulses will be outputted, and there is the possibility that some cycles may be skipped completely.
5. When the difference between V_{IN} and V_{OUT} is small, and the load current is heavy, very wide pulses will be outputted and there is the possibility that some cycles may be skipped completely.
6. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operation, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:

   $Ipk = (V_{IN} - V_{OUT}) \times OnDuty / (2 \times L \times f_{OSC}) + I_{OUT}$

   L: Coil Inductance Value

   f_{OSC}: Oscillation Frequency
7. When the peak current which exceeds limit current flows within the specified time, the built-in P-ch driver transistor turns off. During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the external components such as a coil.
8. When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.
9. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.
10. Use of the IC at voltages below the recommended voltage range may lead to instability.
11. This IC should be used within the stated absolute maximum ratings in order to prevent damage to the device.
12. When the IC is used in high temperature, output voltage may increase up to input voltage level at no load because of the leak current of the driver transistor.
13. The current limit is set to 1350mA (MAX.) at typical. However, the current of 1350mA or more may flow. In case that the current limit functions while the V_{OUT} pin is shorted to the GND pin, when P-ch MOSFET is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when N-ch MOSFET is ON, there is almost no potential difference at both ends of the coil since the V_{OUT} pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. Even in this case, however, after the over current state continues for several ms, the circuit will be latched. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.

①Current flows into P-ch MOSFET to reach the current limit (I_{LIM}).
②The current of I_{LIM} or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of P-ch MOSFET.
③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
④Lx oscillates very narrow pulses by the current limit for several ms.
⑤The circuit is latched, stopping its operation.



■NOTE ON USE (Continued)

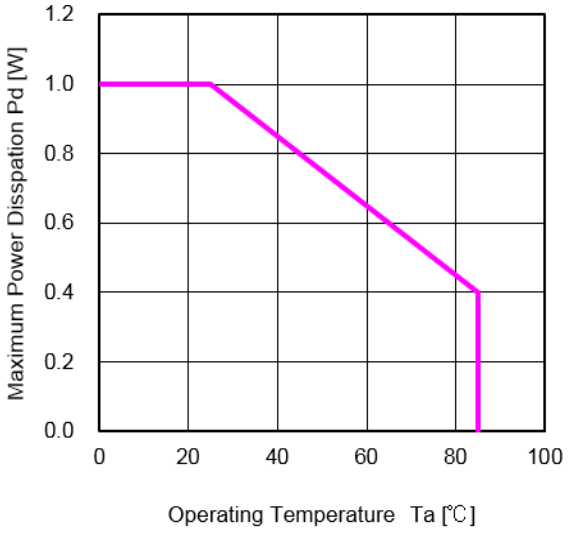
14. In order to stabilize V_{IN} voltage level and oscillation frequency, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} & V_{SS} pins.

15. High step-down ratio and very light load may lead an intermittent oscillation when PWM mode.

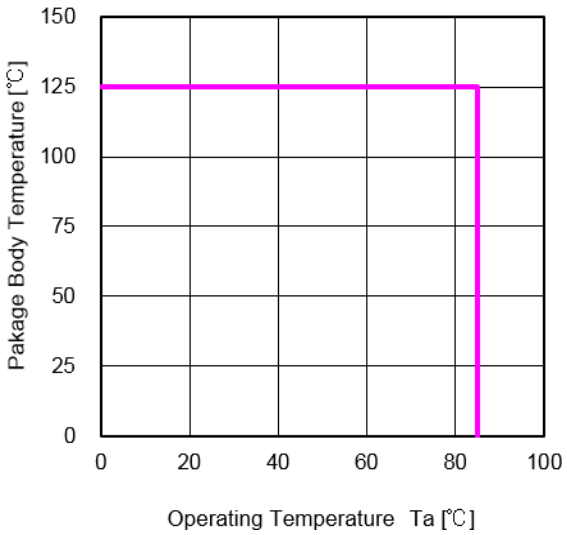
16. Please use within the power dissipation range below. Please also note that the power dissipation may change by test conditions. The power dissipation figure shown is PCB mounted.

17. The proper position of mounting is based on the coil terminal

Pd vs Operating Temperature
MYRGP-x-RF



Package Body Temperature vs Operating Temperature
MYRGP-x-RF



The power loss of mini DC/DC according to the following formula:

power loss = $V_{OUT} \times I_{OUT} \times ((100/EFFI) - 1)$ (W)

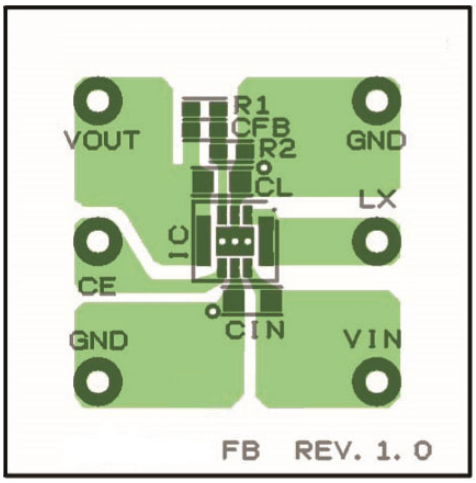
V_{OUT} : Output Voltage (V)
I_{OUT} : Output Current (A)
EFFI : Conversion Efficiency (%)

■NOTE ON USE (Continued)

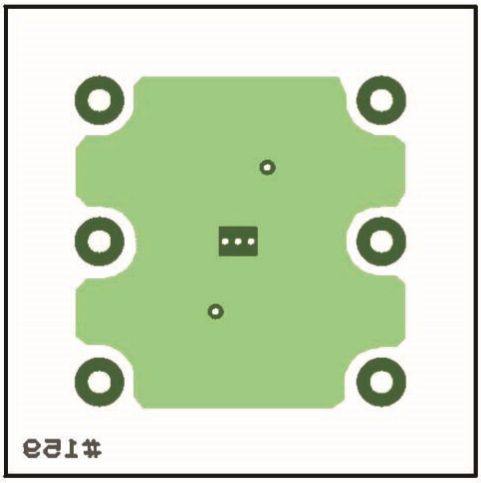
18. Instructions of pattern layouts

(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} (No.6) & V_{SS} (No.5) pins.
(2) Please mount each external component as close to the IC as possible.
(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
(4) Make sure that the PCB GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
(5) This series' internal driver transistors bring on heat because of the output current and ON resistance of driver transistors.
(6) Please connect Lx (No.1) pin and L1 (No.7) pin by wiring on the PCB.
(7) Please connect V_{OUT} (No.3) pin and L2 (No.8) pin by wiring on the PCB.

・MYRGP-x-RF



<FRONT>

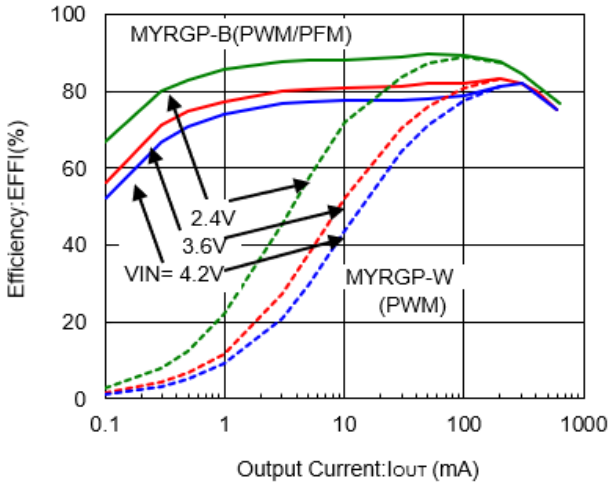


<BACK (Flip Horizontal)>

■TYPICAL PERFORMANCE CHARACTERISTICS

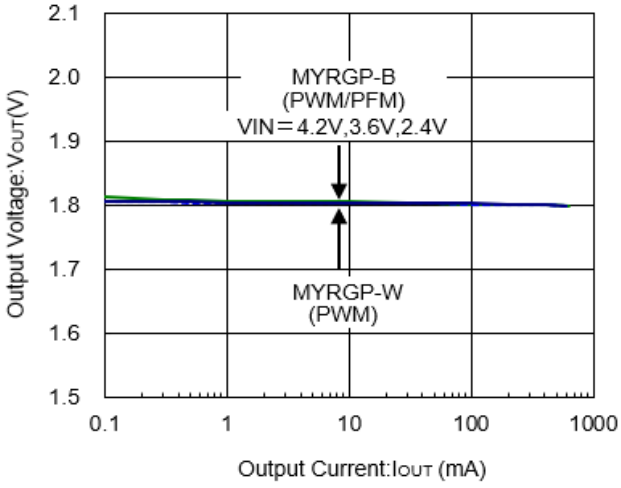
(1) Efficiency vs. Output Current

MYRGP080060W/B21RF



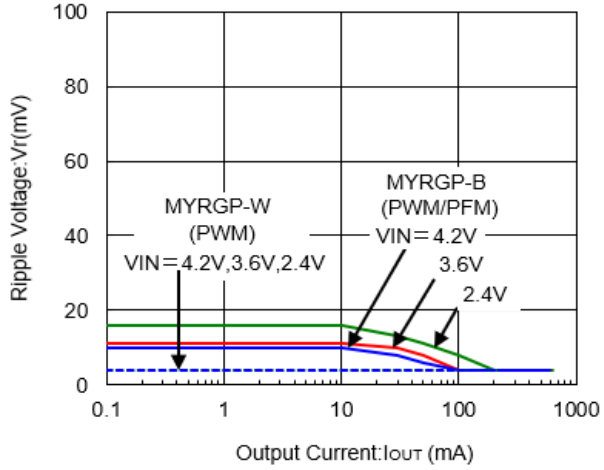
(2) Output Voltage vs. Output Current

MYRGP080060W/B21RF



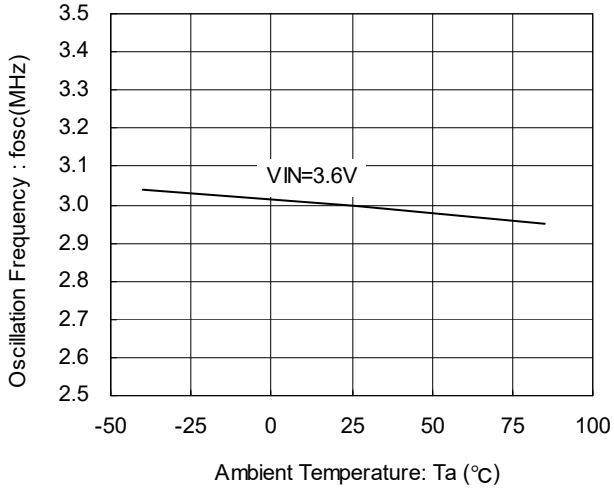
(3) Ripple Voltage vs. Output Current

MYRGP080060W/B21RF



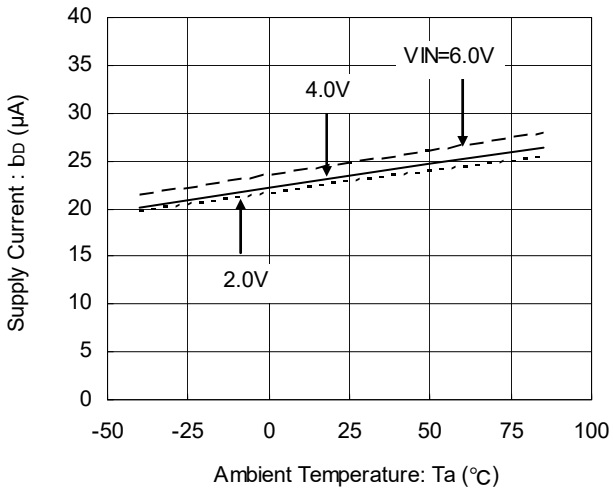
(4) Oscillation Frequency vs. Ambient Temperature

MYRGP080060W/B21RF



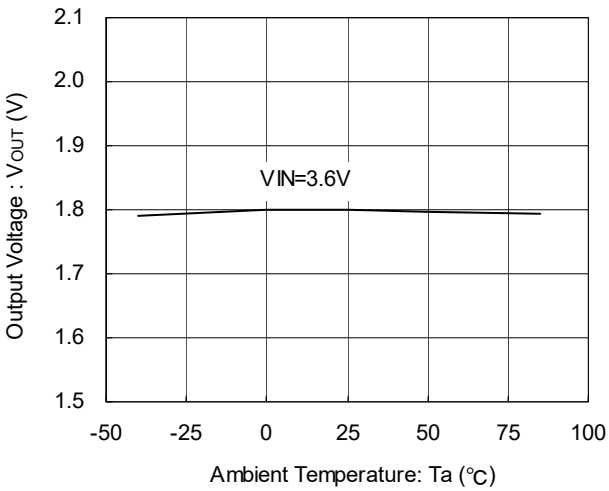
(5) Supply Current vs. Ambient Temperature

MYRGP080060B21RF



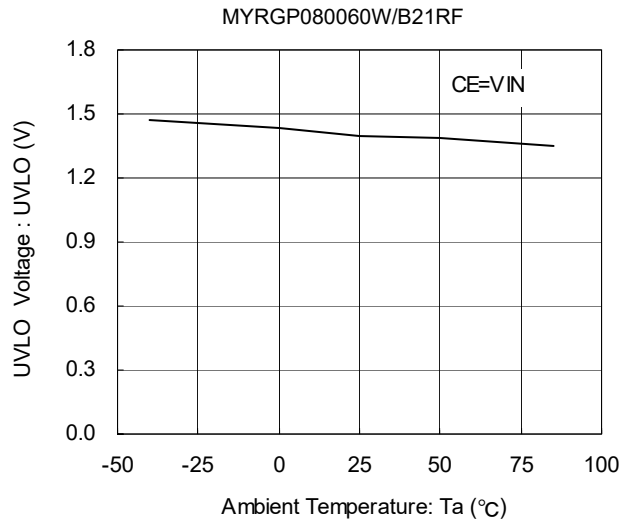
(6) Output Voltage vs. Ambient Temperature

MYRGP080060W/B21RF

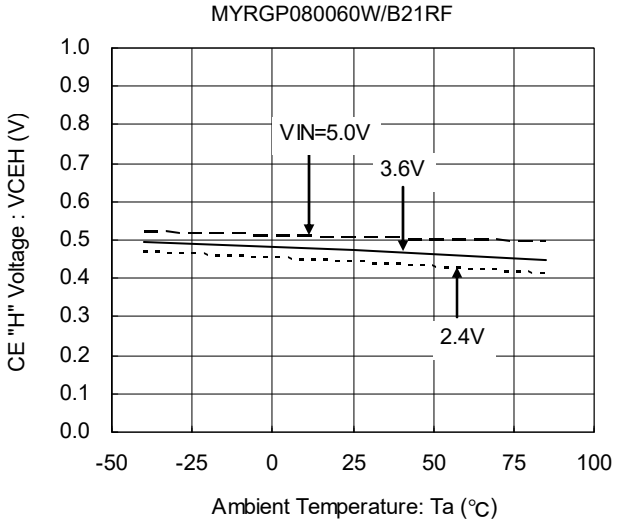


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

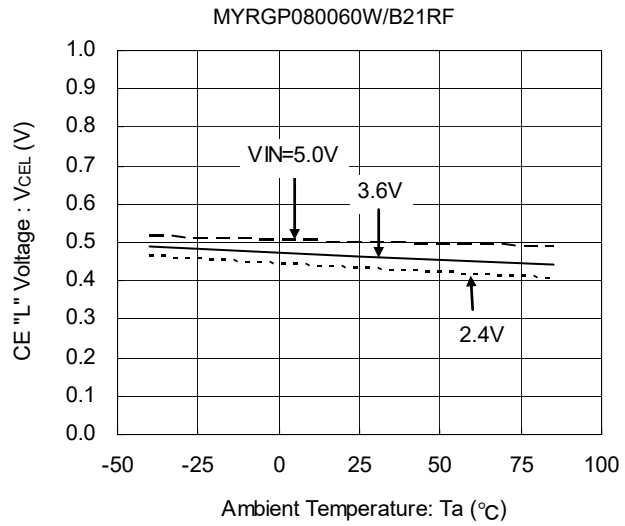
(7) UVLO Voltage vs. Ambient Temperature



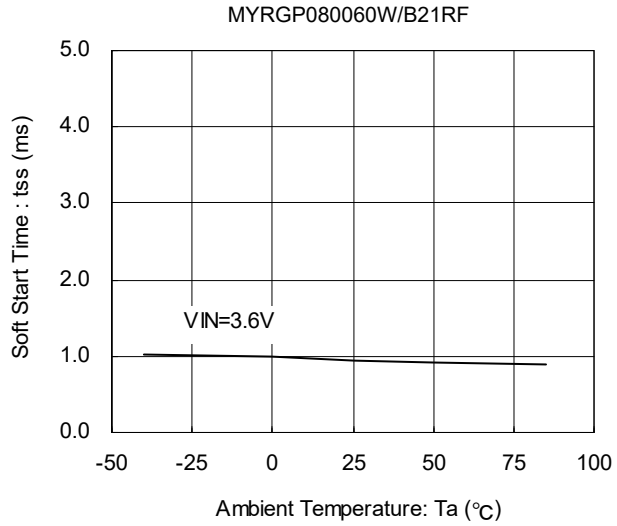
(8) CE "H" Voltage vs. Ambient Temperature



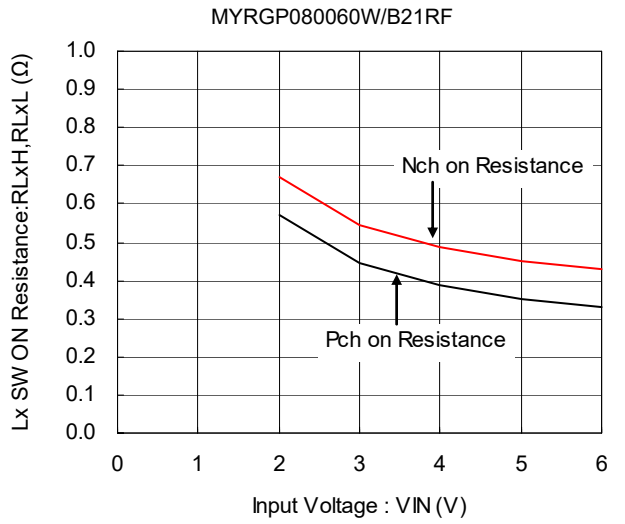
(9) CE "L" Voltage vs. Ambient Temperature



(10) Soft Start Time vs. Ambient Temperature



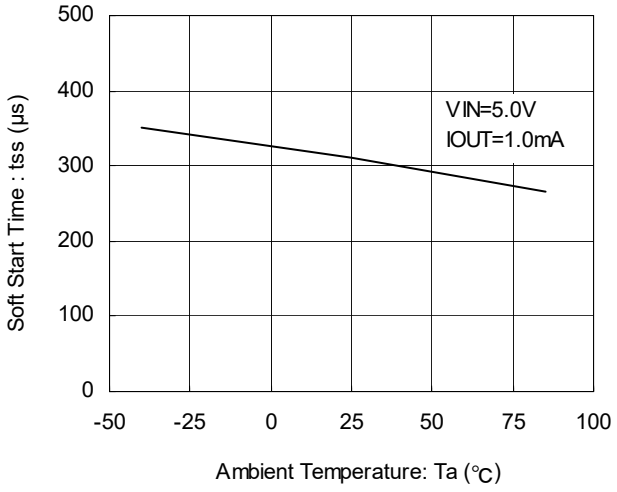
(11) "Pch / Nch" Driver on Resistance vs. Input Voltage



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

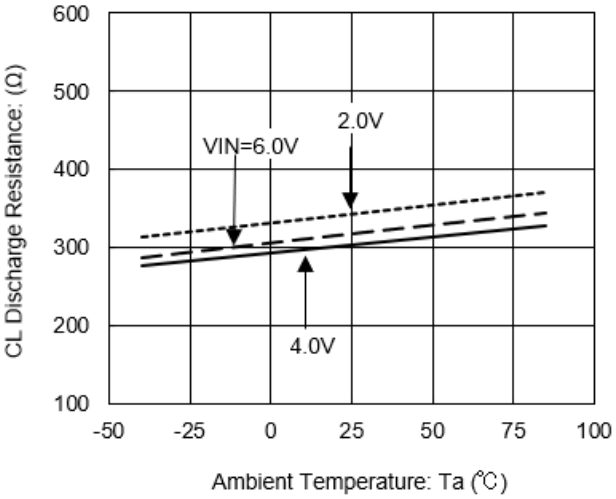
(12) Soft-Start Time vs. Ambient Temperature

MYRGP080060W/B21RF



(13) CL Discharge Resistance vs. Ambient Temperature

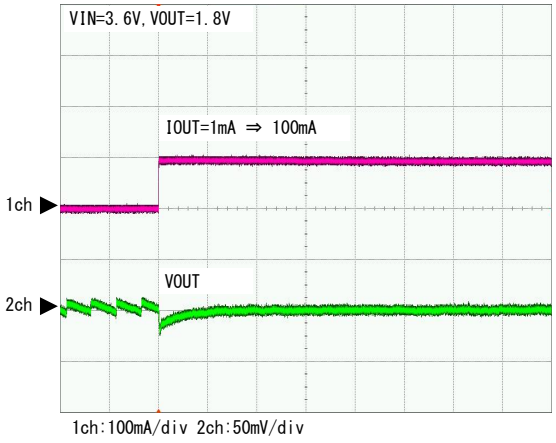
MYRGP080060W/B21RF



(14) Load Transient Response 1

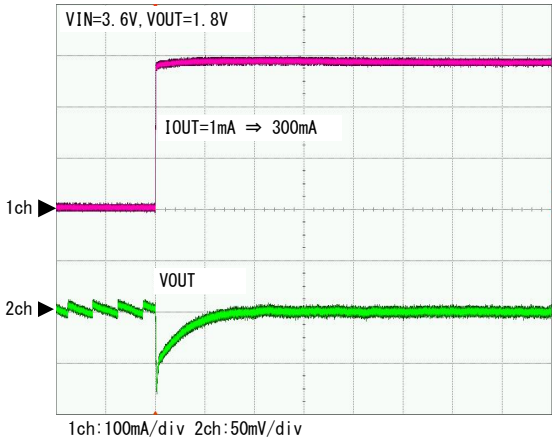
MODE：PWM/PFM Automatic Switching Control

MYRGP080060B21RF



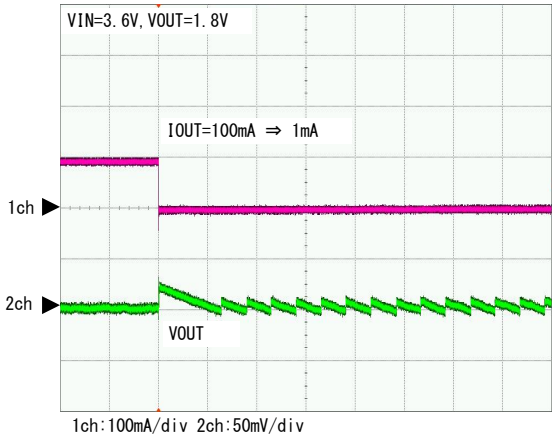
Time: 100µs /div

MYRGP080060B21RF



Time: 100µs /div

MYRGP080060B21RF



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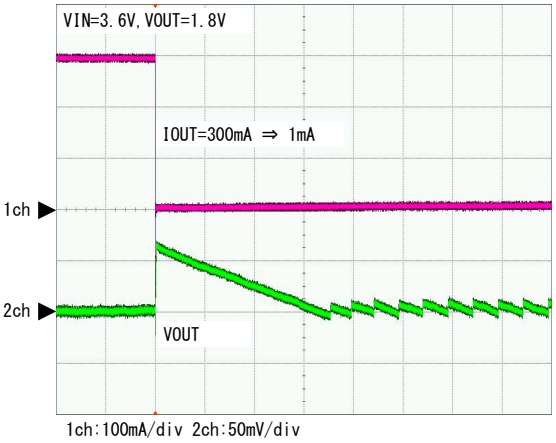
MYRGP080060B21RF



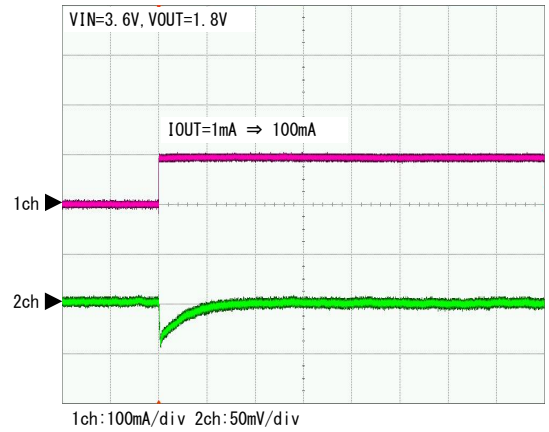
Time: 100µs /div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Load Transient Response 2

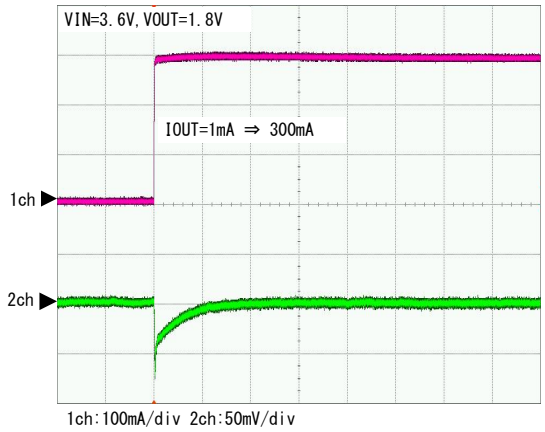
MODE：PWM Control

MYRGP080060W21RF



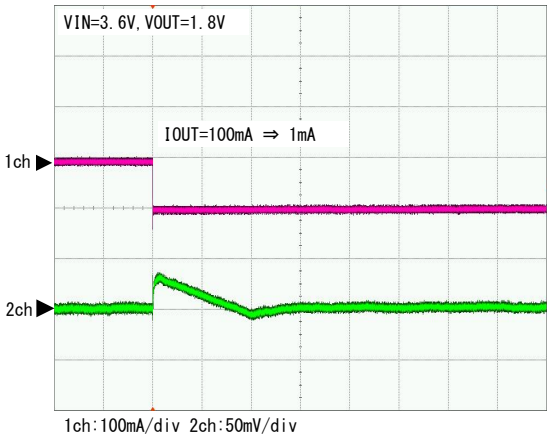
Time: 100μs /div

MYRGP080060W21RF



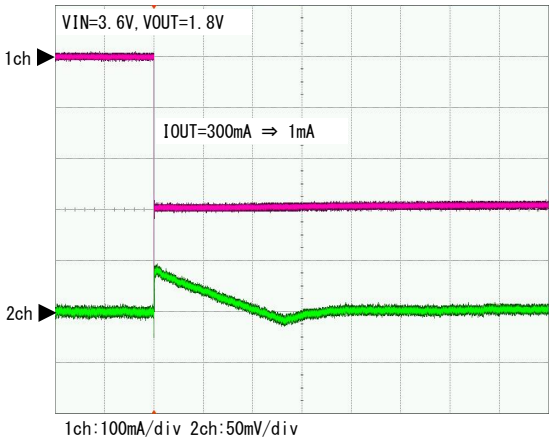
Time: 100μs /div

MYRGP080060W21RF



Time: 100μs /div

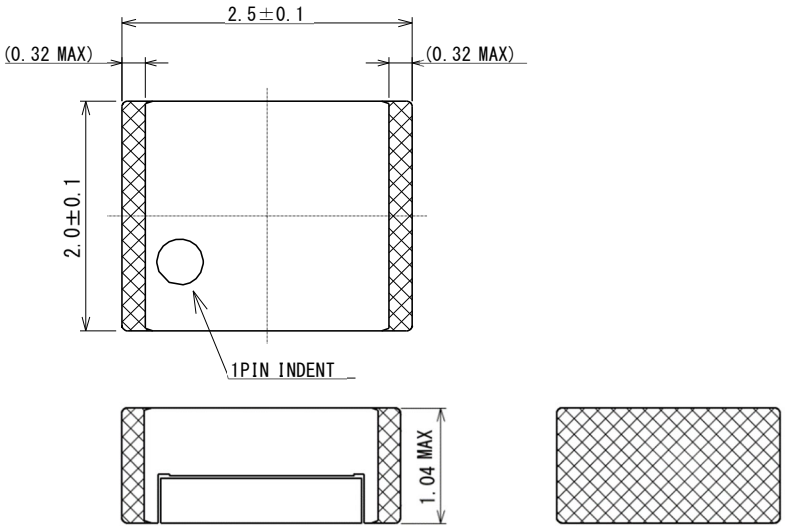
MYRGP080060W21RF

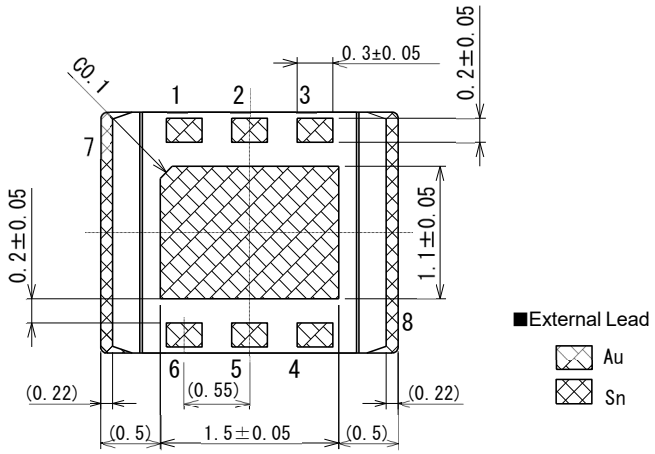


Time: 100μs /div

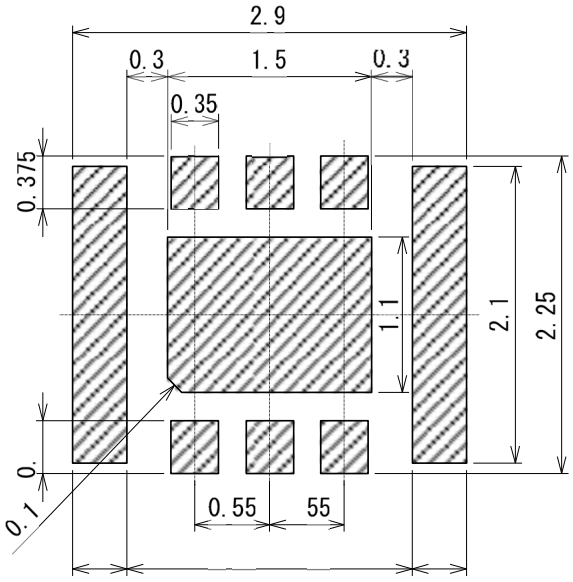
■PACKAGING INFORMATION

●Packaging (2.0mm×2.5mm, h=1.0mm)

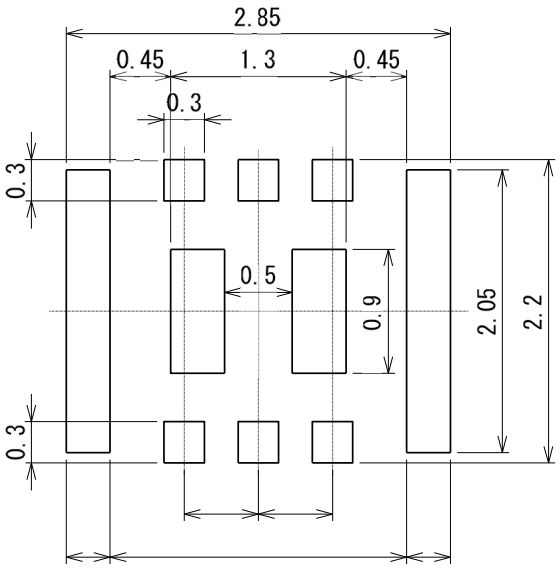




●Reference Pattern Layout (unit: mm)



●Reference Metal Mask Design (unit: mm)

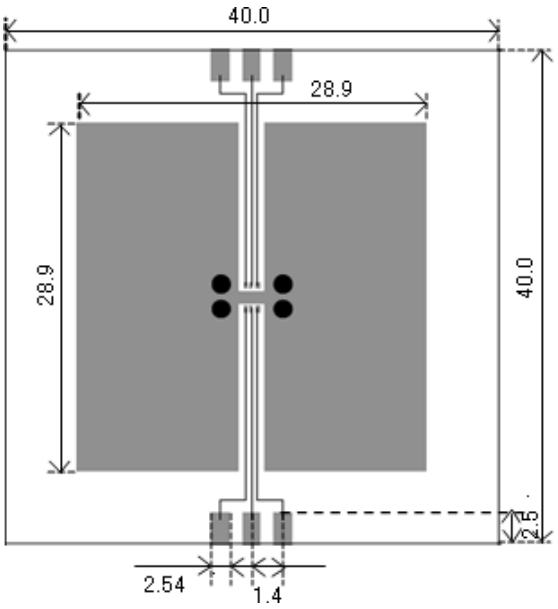


■PACKAGING INFORMATION

Power Dissipation

Power dissipation data for the package is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

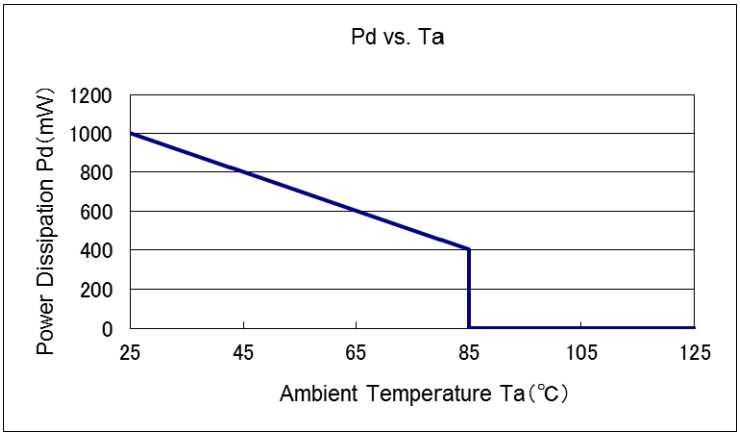
1. Measurement Condition (Reference data)
   - Condition : Mount on a board
   - Ambient : Natural convection
   - Soldering : Lead (Pb) free
   - Board Dimensions : 40 x 40 mm (1600mm2 in one side)
     Copper (Cu) traces occupy 50% of the board area in top and back faces Package heat-sink is tied to the copper traces.
   - Material : Glass Epoxy (FR-4)
   - Thickness : 1.6 mm
   - Through-hole : 4 x 0.8 Diameter



Evaluation Board (Unit:mm)

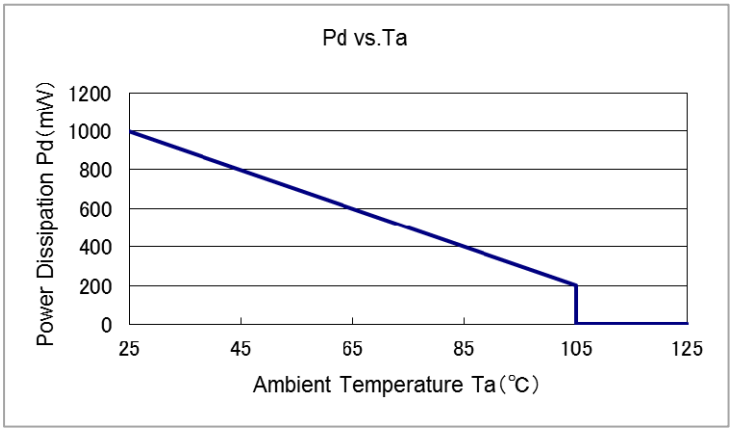
2. Power Dissipation vs. Ambient Temperature(85℃)
   Board Mount (Tjmax=125℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	1000	100.00
85	400	

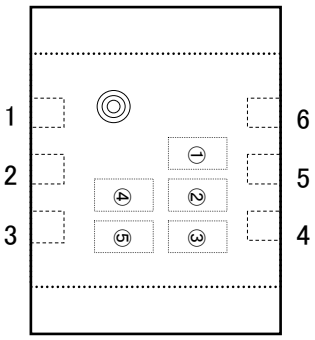


3. Power Dissipation vs. Ambient Temperature(105℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	1000	100.00
105	200	



■MARKING RULE



① represents products series

MARK	PRODUCT SERIES
4	MYRGP-W-RF
5	MYRGP-B-RF

② represents type of DC/DC converters

OUTPUT VOLTAGE (V)	MARK
	MYRGP-x-RF
0.x	U

③ represents the decimal part of output voltage

MARK	PRODUCT SERIES
8	MYRGP080060x21RF

④,⑤ represents production lot number
01～09、0A～0Z、11～9Z、A1～A9、AA～AZ、B1～ZZ in order.
(G, I, J, O, Q, W excluded)　Note: No character inversion used.

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