NUP1301QA-Q

Ultra low capacitance ESD protection array

4 July 2022 **Product data sheet**

1. General description

Ultra low capacitance ElectroStatic Discharge (ESD) protection array in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads, designed to protect one signal line in rail-to-rail configuration from the damage caused by ESD and other transients.

2. Features and benefits

- ESD protection of one signal line (rail-to-rail configuration)
- Ultra low diode capacitance: C_d = 2.3 pF
- Very low reverse leakage current: ≤ 30 nA
- ESD protection up to 30 kV
- ESD robustness exceeds IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 11 A at t_p = 8/20 µs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Telecommunication networks
- Video line protection
- Microcontroller protection
- I^2C-bus protection
- Antenna power supply
- Analog audio
- Class-D amplifier

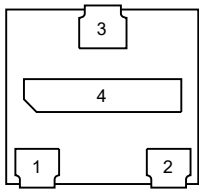
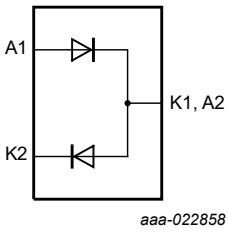
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_R	reverse voltage	T_{amb} = 25 °C		-	-	80	V
I_R	reverse current	V_R = 25 V; T_{amb} = 25 °C		-	7	30	nA
		V_R = 80 V; T_{amb} = 25 °C		-	50	500	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 1 - pin 3		-	0.5	0.75	pF
		f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 2 - pin 3		-	1.8	2	pF
		f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 3 - pins 1 and 2		-	2.3	2.75	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A1	anode (diode 1)	 Transparent top view **DFN1010D-3 (SOT1215)**	
2	K2	cathode (diode 2)		
3	K1, A2	cathode (diode 1) and anode (diode 2)		
4	K1, A2	cathode (diode1) and anode (diode2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NUP1301QA-Q	DFN1010D-3	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.75 mm pitch; 1.1 mm x 1 mm x 0.37 mm body	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
NUP1301QA-Q	X 011

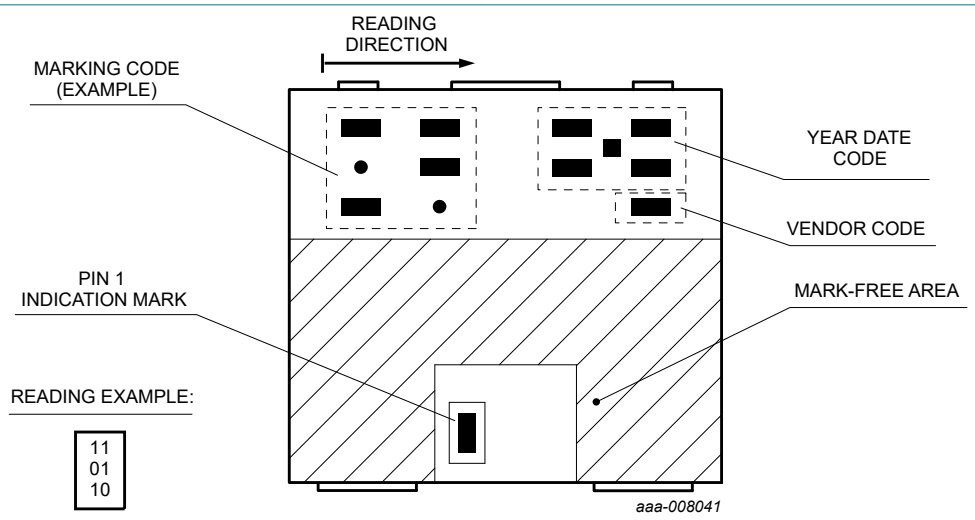


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_R	reverse voltage	T_{amb} = 25 °C		-	80	V
I_F	forward current	pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; single diode loaded; T_{amb} = 25 °C		-	290	mA
		pulsed; $t_p \leq$ 300 µs; $\delta \leq$ 0.02; double diode loaded; T_{amb} = 25 °C		-	170	mA
I_{FRM}	repetitive peak forward current	$t_p \leq$ 500 µs; $\delta \leq$ 0.25; T_j = 25 °C		-	700	mA
I_{PPM}	rated peak pulse current	t_p = 8/20 µs	[1] [2]	-	11	A
I_{FSM}	non-repetitive peak forward current	square wave; t_p = 100 µs		-	4	A
		square wave; t_p = 1 ms		-	1.5	A
		square wave; t_p = 1 s		-	0.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2] [3]	-	30	kV

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).
[3] Device stressed with ten non-repetitive ESD pulses.

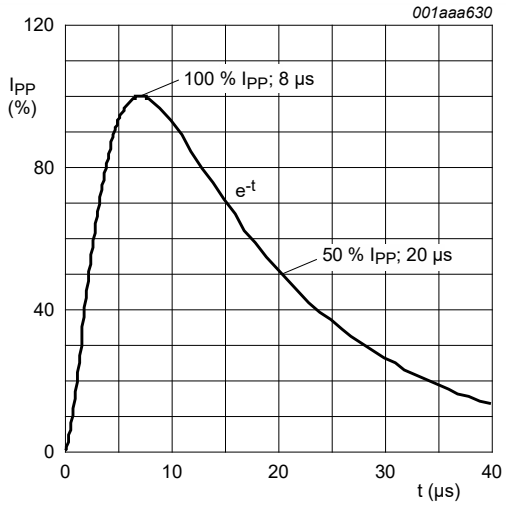


Fig. 2. 8/20 µs pulse waveform according to IEC 61000-4-5

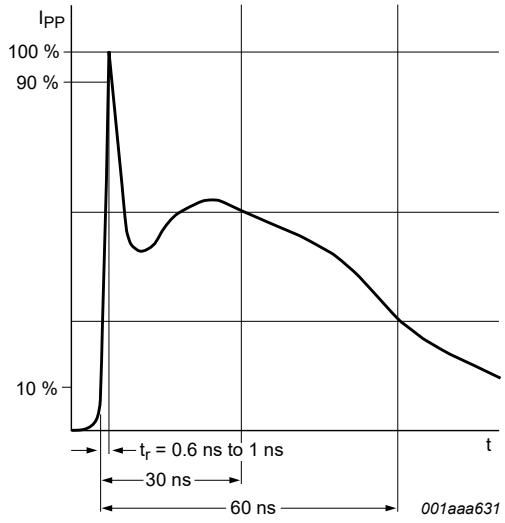


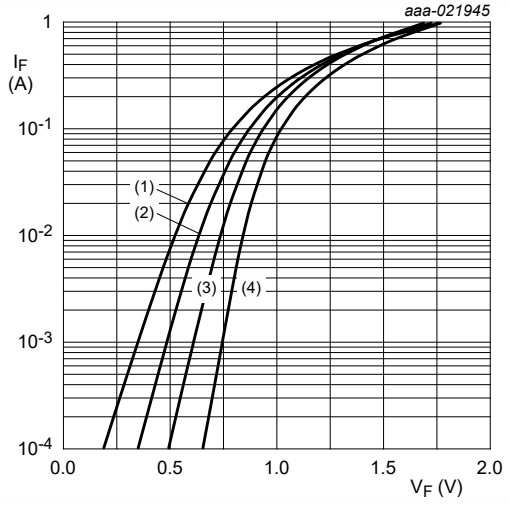
Fig. 3. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

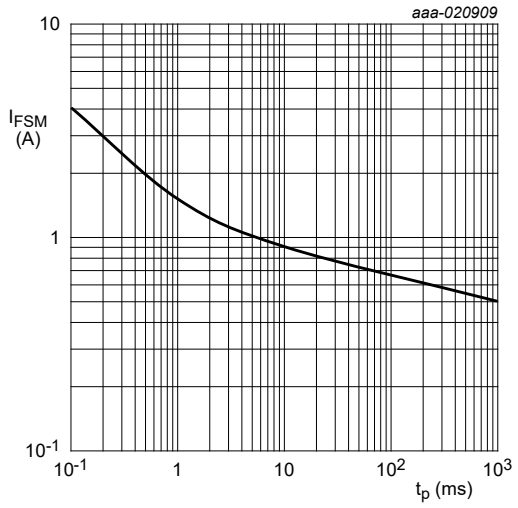
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	forward voltage	I_F = 1 mA; T_{amb} = 25 °C	[1]	-	-	715	mV
		I_F = 10 mA; T_{amb} = 25 °C	[1]	-	-	855	mV
		I_F = 50 mA; T_{amb} = 25 °C; Pulse	[1]	-	-	1	V
		I_F = 150 mA; T_{amb} = 25 °C	[1]	-	-	1.25	V
V_{BR}	breakdown voltage	I_R = 0.1 mA; T_{amb} = 25 °C		100	-	-	V
I_R	reverse current	V_R = 25 V; T_{amb} = 25 °C		-	7	30	nA
		V_R = 80 V; T_{amb} = 25 °C		-	50	500	nA
		V_R = 25 V; T_j = 150 °C		-	-	30	µA
		V_R = 80 V; T_j = 150 °C		-	-	150	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 1 - pin 3		-	0.5	0.75	pF
		f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 2 - pin 3		-	1.8	2	pF
		f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; Pin 3 - pins 1 and 2		-	2.3	2.75	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[2] [3]	-	-	3	V
		I_{PP} = 11 A; T_{amb} = 25 °C	[2] [3]	-	-	10	V
R_{dyn}	dynamic resistance	TLP = 10 A; positive; T_{amb} = 25 °C		-	0.55	-	Ω
		TLP = 10 A; negative; T_{amb} = 25 °C		-	0.3	-	Ω

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.
[2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).



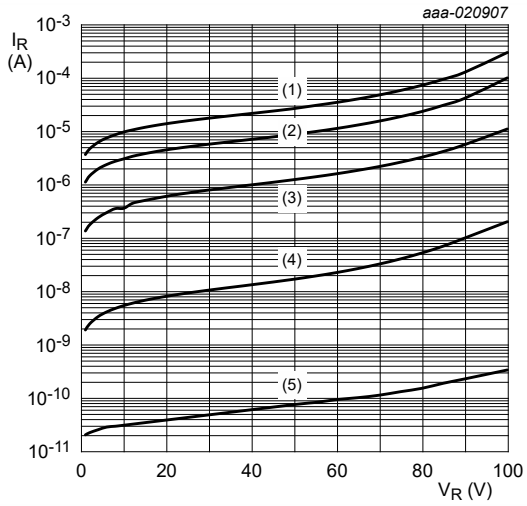
(1) T_j = 150 °C
(2) T_j = 85 °C
(3) T_j = 25 °C
(4) T_j = −40 °C

Fig. 4. Forward current as a function of forward voltage; typical values



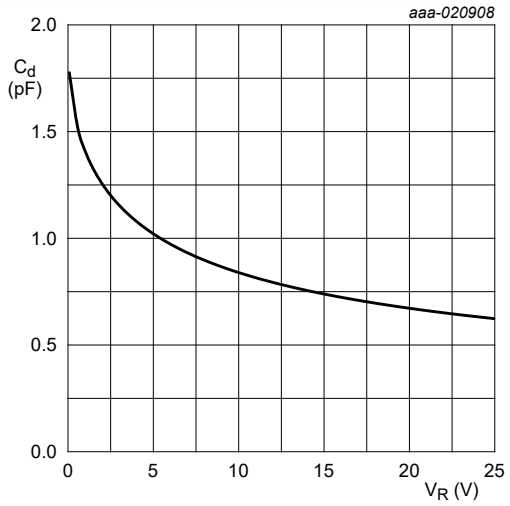
Based on square wave currents.
T_{amb} = 25 °C

Fig. 5. Non-repetitive forward current as a function of pulse duration; maximum values



(1) T_j = 150 °C
(2) T_j = 125 °C
(3) T_j = 85 °C
(4) T_j = 25 °C
(5) T_j = −40 °C

Fig. 6. Reverse current as a function of reverse voltage; typical values



f = 1 MHz; T_{amb} = 25 °C; pin 2 to GND

Fig. 7. Diode capacitance as a function of reverse voltage; typical values

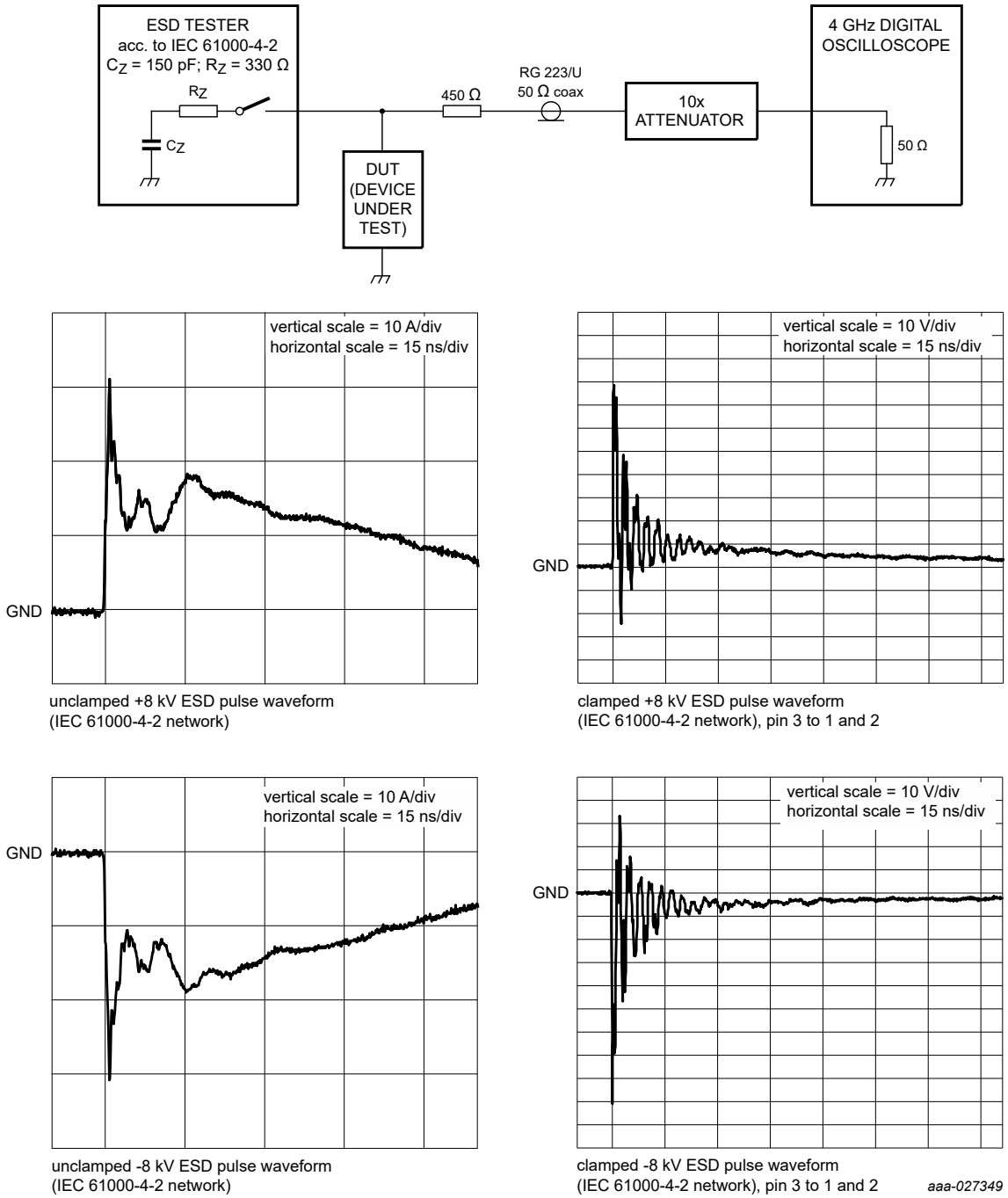
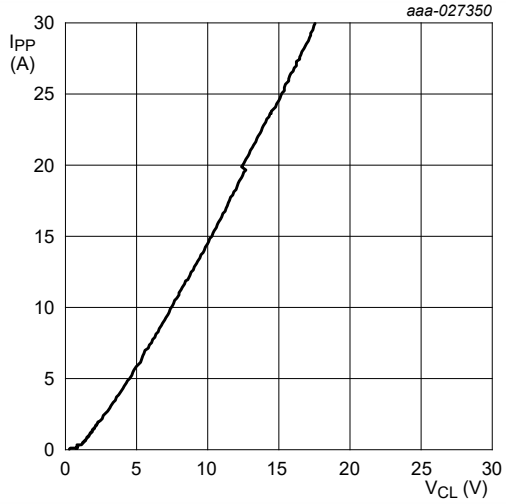
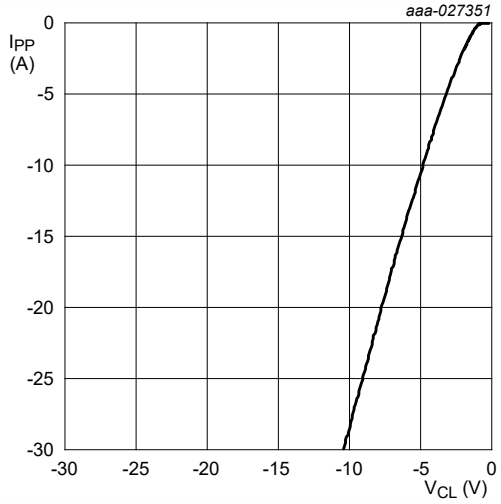


Fig. 8. ESD clamping test setup and waveforms



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 9. Positive clamping voltage (TLP); typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 10. Negative clamping voltage (TLP); typical values

10. Application information

Protection of a single (high-speed) data line in rail-to-rail configuration. The protected data line is connected to pin 3. Pin 1 is connected to ground (GND) and pin 2 is connected to the supply rail (supply voltage V_{CC}.) When the transient voltage exceeds the forward voltage drop of one diode, the transient is directed either to the supply rail or to GND. The advantages of these solutions are: low line capacitance (0.6 pF typically), fast response time, and low clamping voltage.

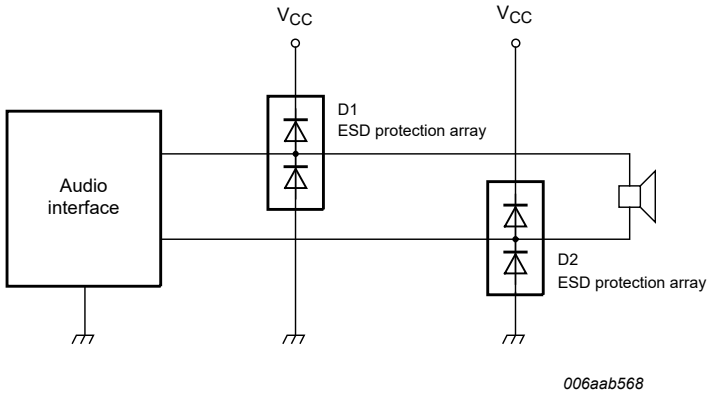


Fig. 11. Typical application for the protection of one signal line

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

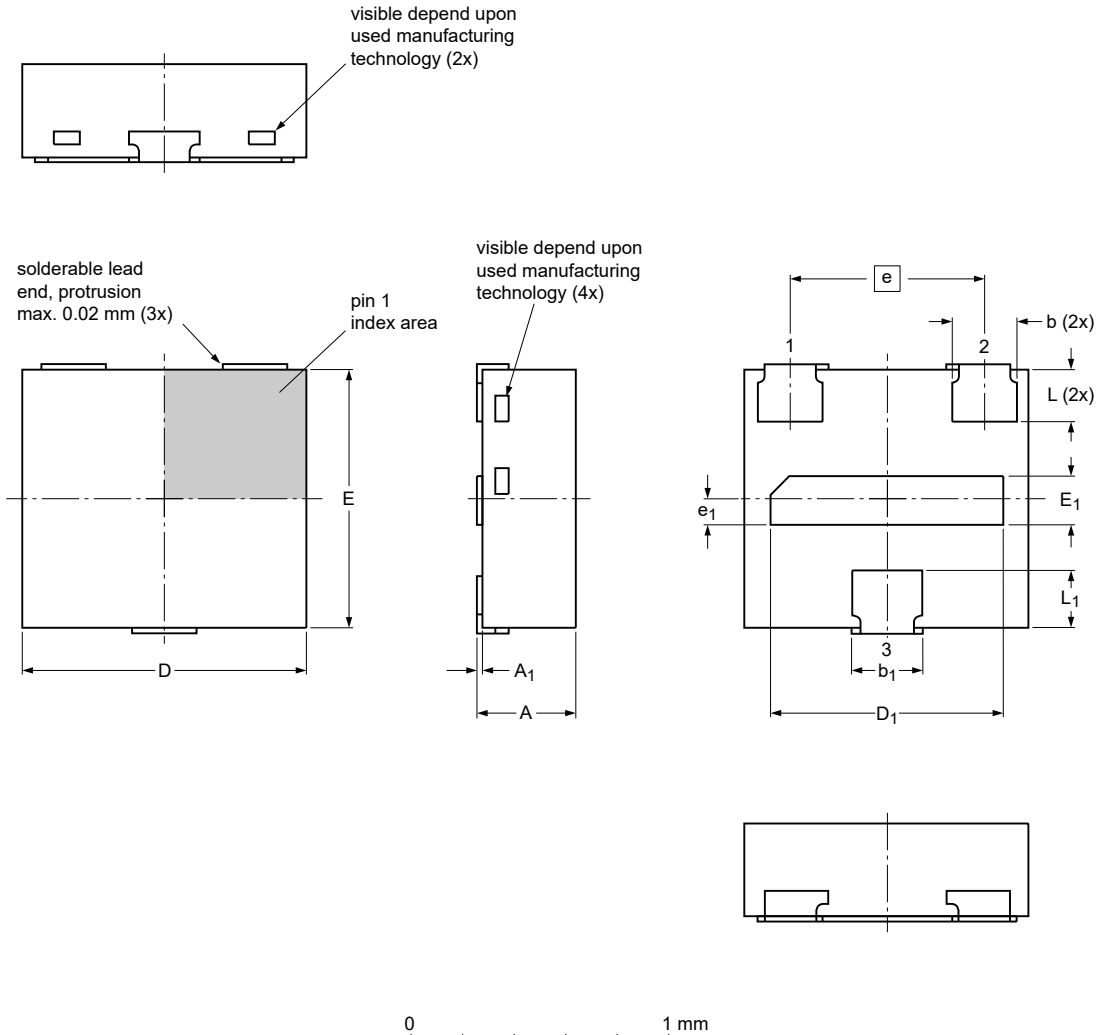
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 x 1.0 x 0.37 mm **SOT1215**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	D	D_1	E	E_1	e	e_1	L	L_1
mm	min	0.34		0.22	0.245	1.05	0.87	0.95	0.16			0.17	0.195
	nom	0.37		0.25	0.275	1.10	0.90	1.00	0.19	0.75	0.1	0.20	0.225
	max	0.40	0.04	0.30	0.325	1.15	0.95	1.05	0.24			0.25	0.275

Note
1. Dimension A is including plating thickness.

sot1215_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1215						~~13-03-05~~ 13-03-06

Fig. 12. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package **SOT1215**

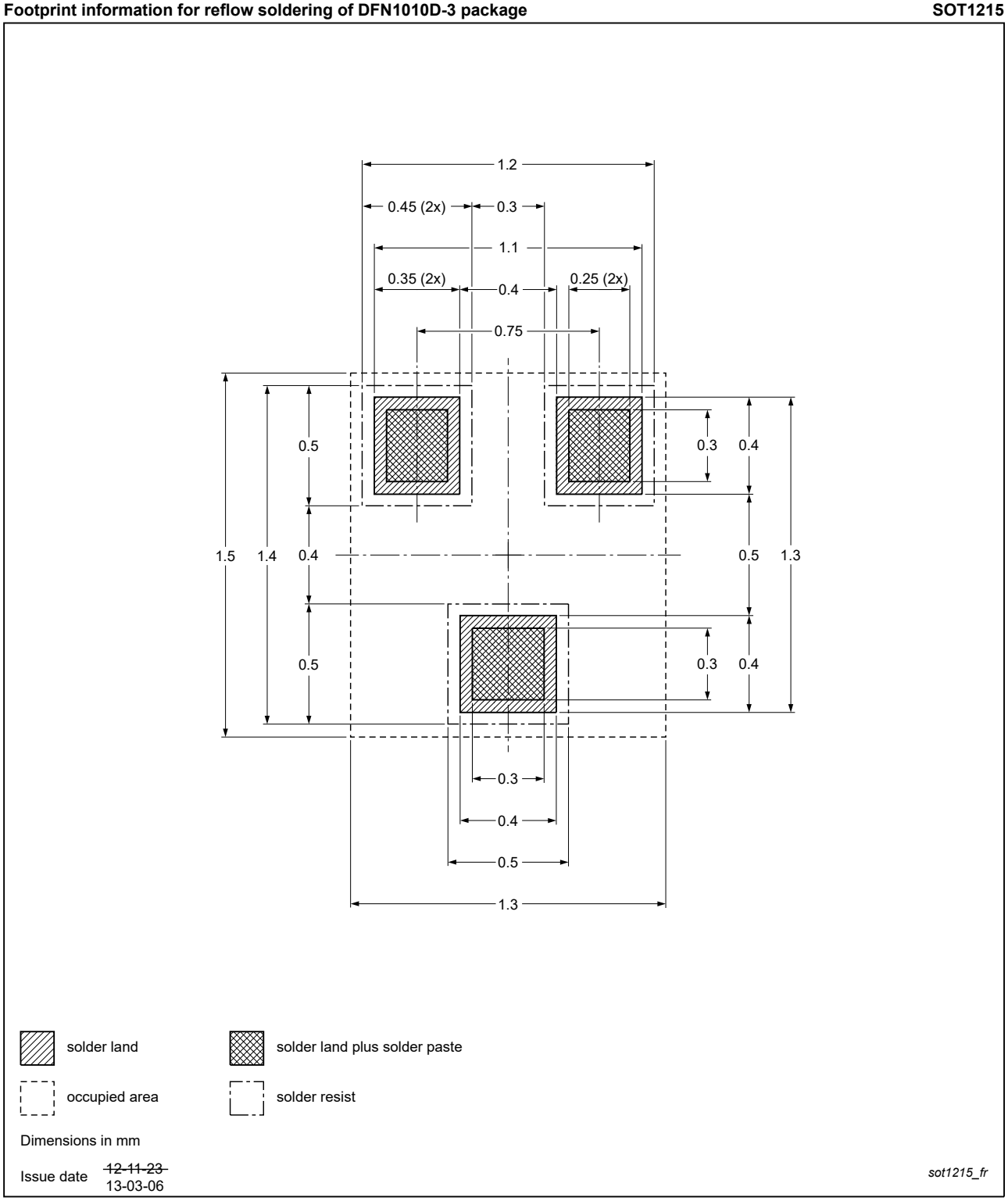


Fig. 13. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NUP1301QA-Q v.1	20220704	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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