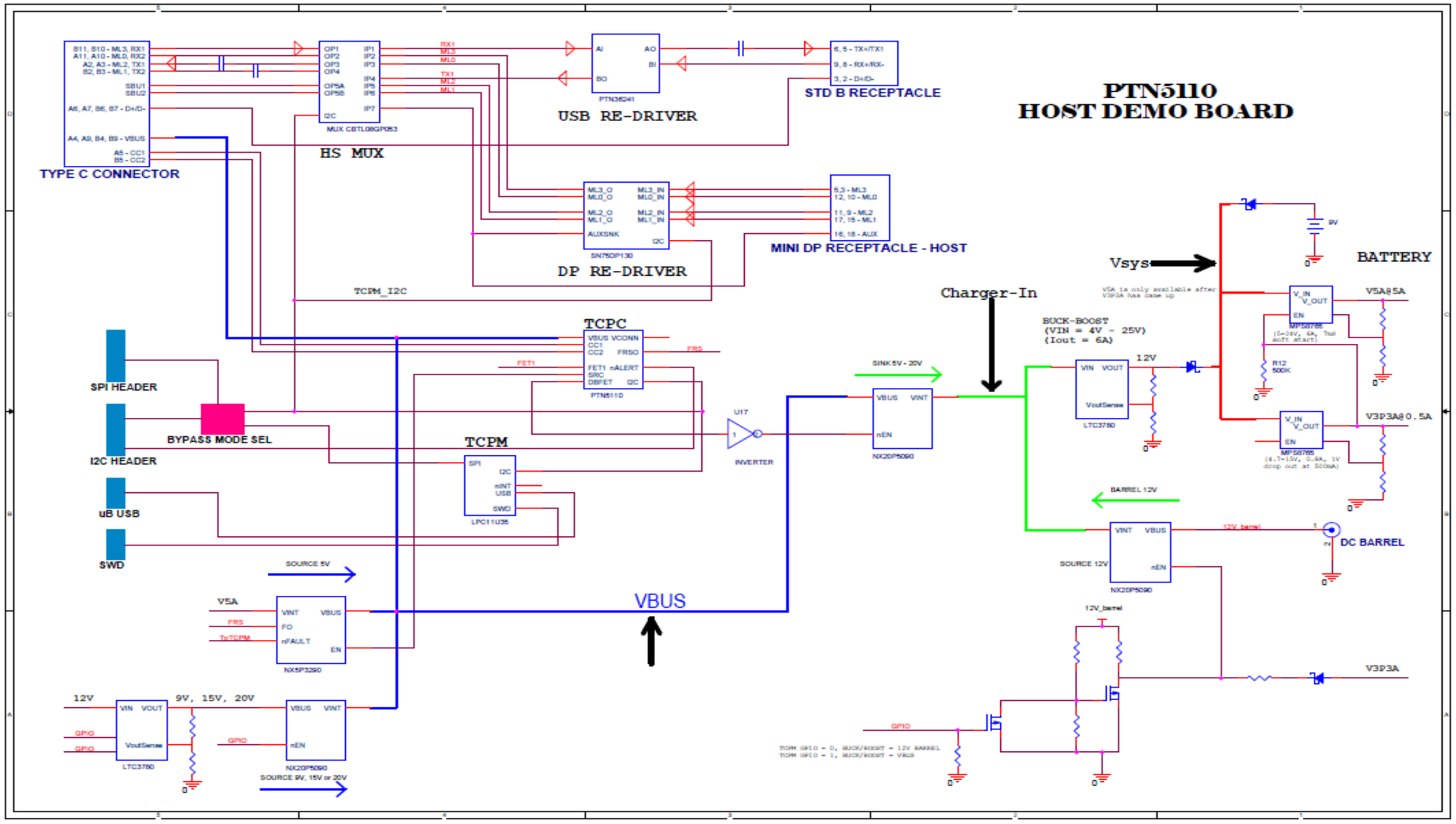
PTN5110 HOST DEMO BOARD



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Title

Block Diagram

Size	Document Number	Rev
B	USB Type-C Alternative Mode Demo Board HOST	A2

Date: Wednesday, August 17, 2016 Sheet 1 of 13

02-22-2016
---
* Re-label L1 & L2 from 2.5A to 7A

03-09-2016 (Rev 2C)
---
* Add pin 17 (GND) to PTN5110

03-12-2016
---
* Replace Q6, Q7, Q8, Q9, Q12,
  Q13, Q14, Q14 with correct part

* Replace J5 with correct part number
  from Mouser

* Replace D20, D22, D23, D25, D26
  with low reverse current version

03-13-2016
---
* Rename signal DC_BARREL_ON
  to nDC_BARREL_ON

* Add Q22 to indicate VBAT_PRESENT

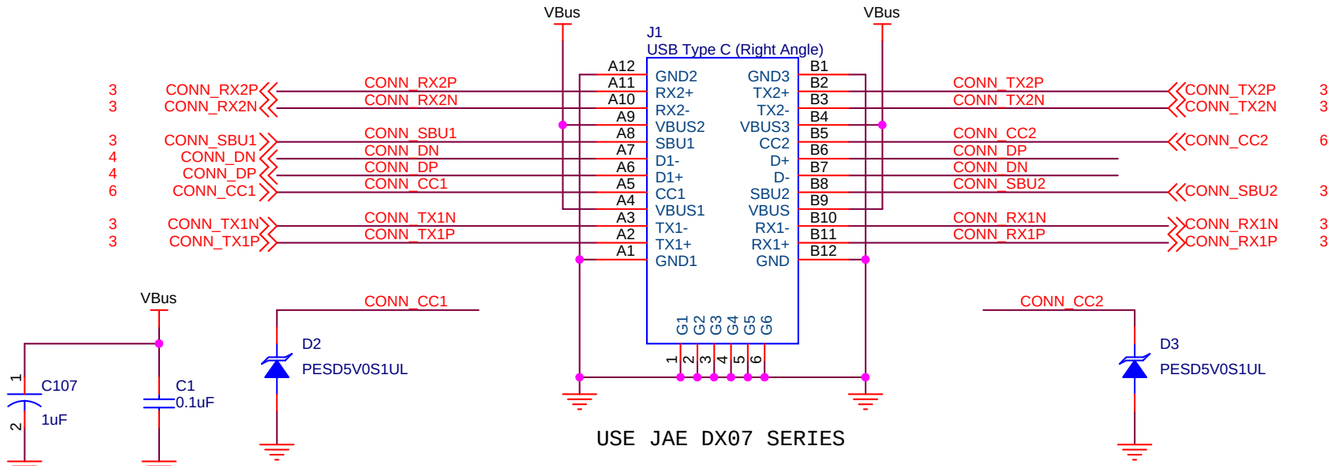
08-02-2016
---
* change C107 to 1uF
* remove U4, change pullup on R30/R31 to BYPASS
* R54 is DNS, R59 is 3.6K instead of 100K
* Added R148
* R51 is DNS
* C48 is 4.7uF instead of 10uF
* U11 and its components are DNS
* Added Q23, Q24, R139, R140
* R123 is 30K and R125 is 3.6K instead of 100K
* R72 and R90 are 1K instead of 100K
* Remove Q16, D45, R98, R99, Q17, R100
* Changed U15 (3290) to correct footprint
* Remove footnote to control Q17
* Changed VARIABLE_PS_LS_ENA to nVARIABLE_PS_LS_ENA

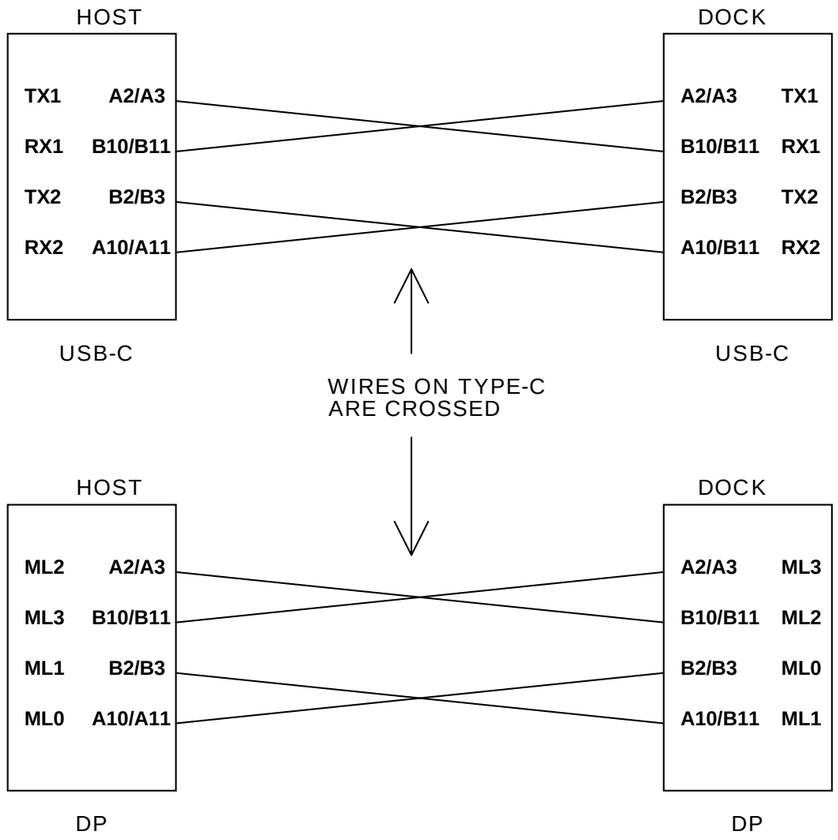
08-16-2016
---
* Add J23 for VBUS load or LCD connection

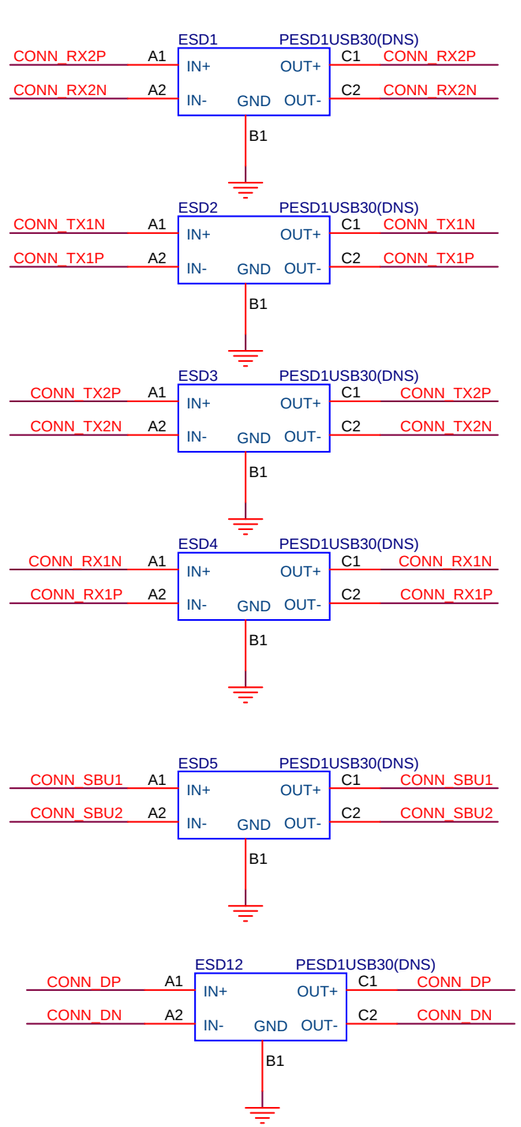
08-17-2016
---
* Change U7 footprint from SOT996-2 to SOT833-1

02-16-2017
---
* Added loading options

Title	<Title>	
Size: Custom	Document Number <Doc>	Rev A2
Date: Thursday, February 16, 2017	Sheet 1 of 1	







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Title: Type-C Connector

Size	Document Number	Rev
B	USB Type-C Alternative Mode Demo Board HOST	A2

Date: Wednesday, August 17, 2016 Sheet 2 of 13

4LANE_DP=1: Select DP Path
4LANE_DP=0: Select USB3 Path

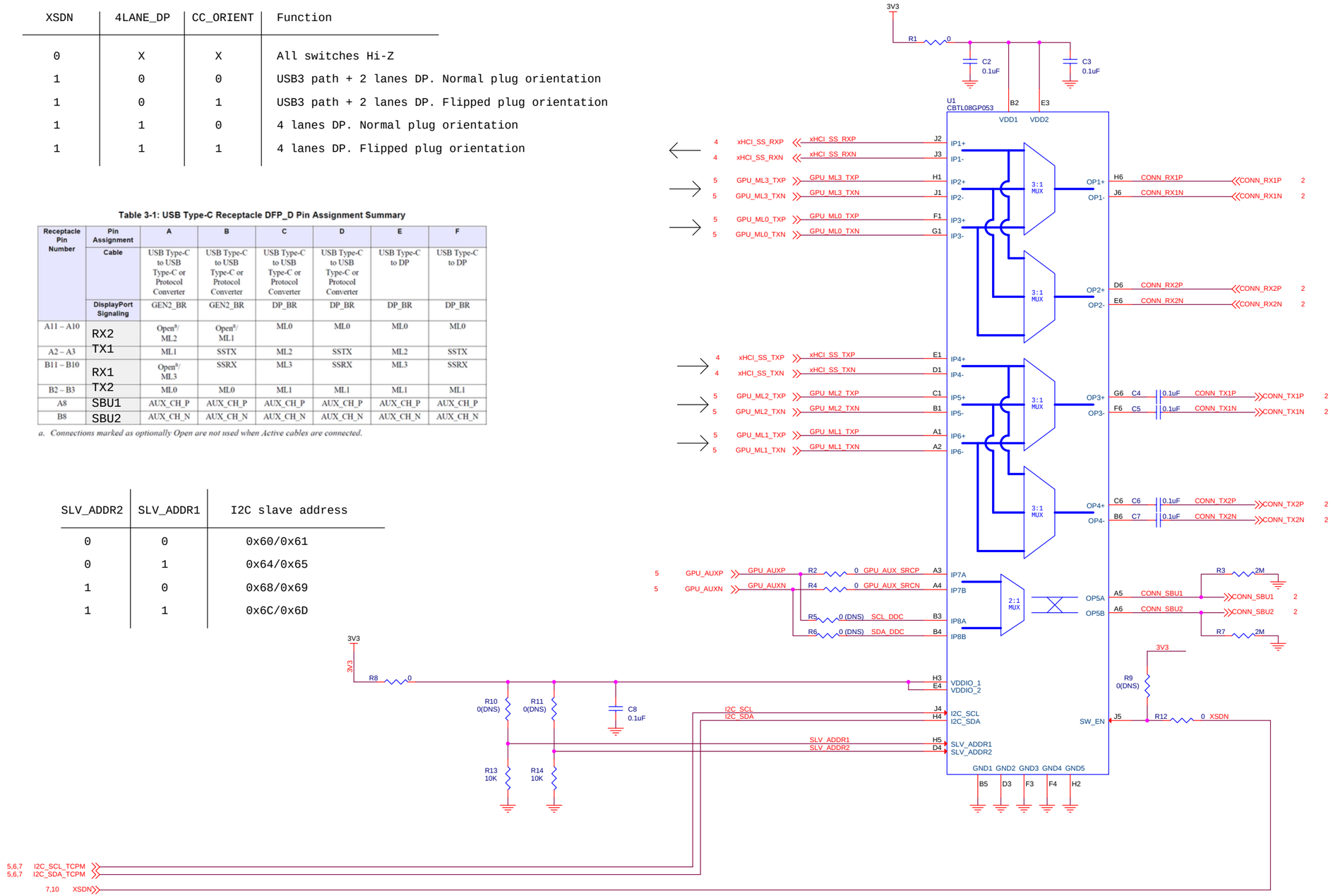
XSDN	4LANE_DP	CC_ORIENT	Function
0	X	X	All switches Hi-Z
1	0	0	USB3 path + 2 lanes DP. Normal plug orientation
1	0	1	USB3 path + 2 lanes DP. Flipped plug orientation
1	1	0	4 lanes DP. Normal plug orientation
1	1	1	4 lanes DP. Flipped plug orientation

Table 3-1: USB Type-C Receptacle DFP_D Pin Assignment Summary

Receptacle Pin Number	Pin Assignment	A	B	C	D	E	F
	Cable	USB Type-C to USB Type-C or Protocol Converter	USB Type-C to USB Type-C or Protocol Converter	USB Type-C to USB Type-C or Protocol Converter	USB Type-C to USB Type-C or Protocol Converter	USB Type-C to DP	USB Type-C to DP
	DisplayPort Signaling	GEN2_BR	GEN2_BR	DP_BR	DP_BR	DP_BR	DP_BR
A11 – A10	RX2	Open[a]/ ML2	Open[a]/ ML1	ML0	ML0	ML0	ML0
A2 – A3	TX1	ML1	SSTX	ML2	SSTX	ML2	SSTX
B11 – B10	RX1	Open[a]/ ML3	SSRX	ML3	SSRX	ML3	SSRX
B2 – B3	TX2	ML0	ML0	ML1	ML1	ML1	ML1
A8	SBU1	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P	AUX_CH_P
B8	SBU2	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N	AUX_CH_N

a. Connections marked as optionally Open are not used when Active cables are connected.

SLV_ADDR2	SLV_ADDR1	I2C slave address
0	0	0x60/0x61
0	1	0x64/0x65
1	0	0x68/0x69
1	1	0x6C/0x6D



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Title: CBTL08GP053 Switch

Size	Document Number	Rev
C	USB Type-C Alternative Mode Demo Board HOST	A2

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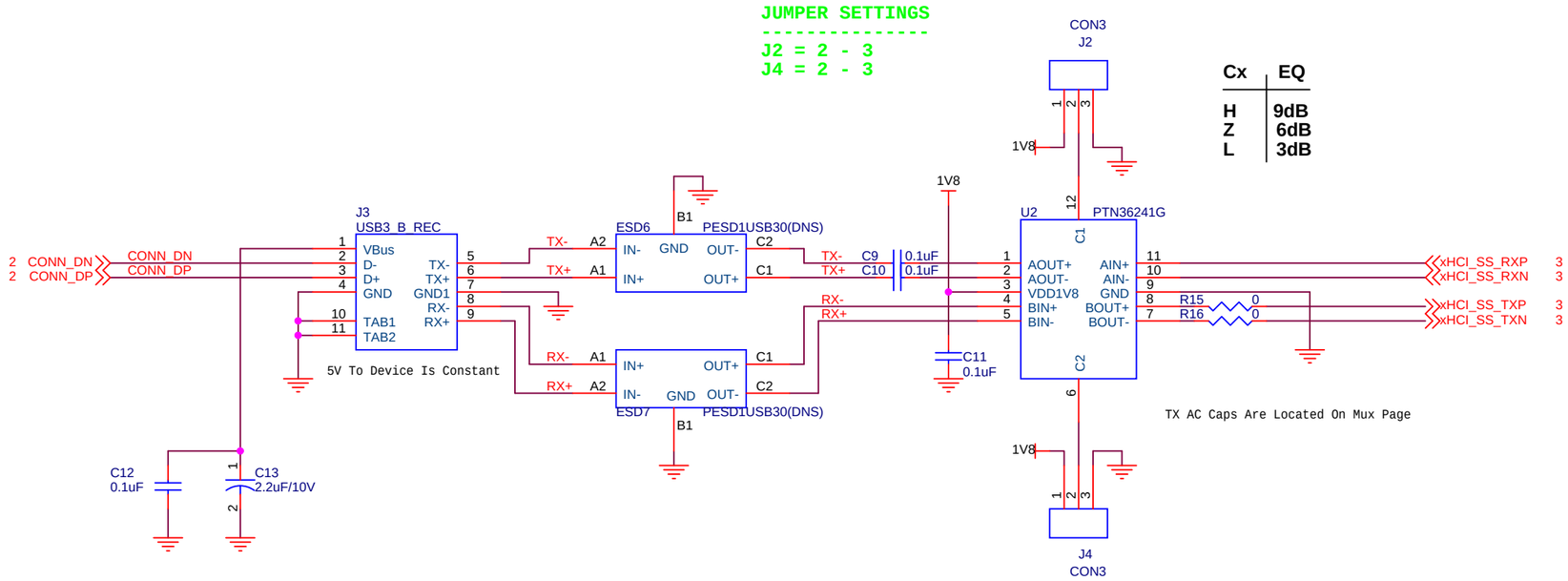
JUMPER SETTINGS

J2 = 2 - 3
J4 = 2 - 3

Cx	EQ
H	9dB
Z	6dB
L	3dB



Title	USB3.0 Redriver	
Size: Custom	Document Number: USB Type-C Alternative Mode Demo Board HOST	Rev: A2
Date: Thursday, February 16, 2017	Sheet 4 of 13	

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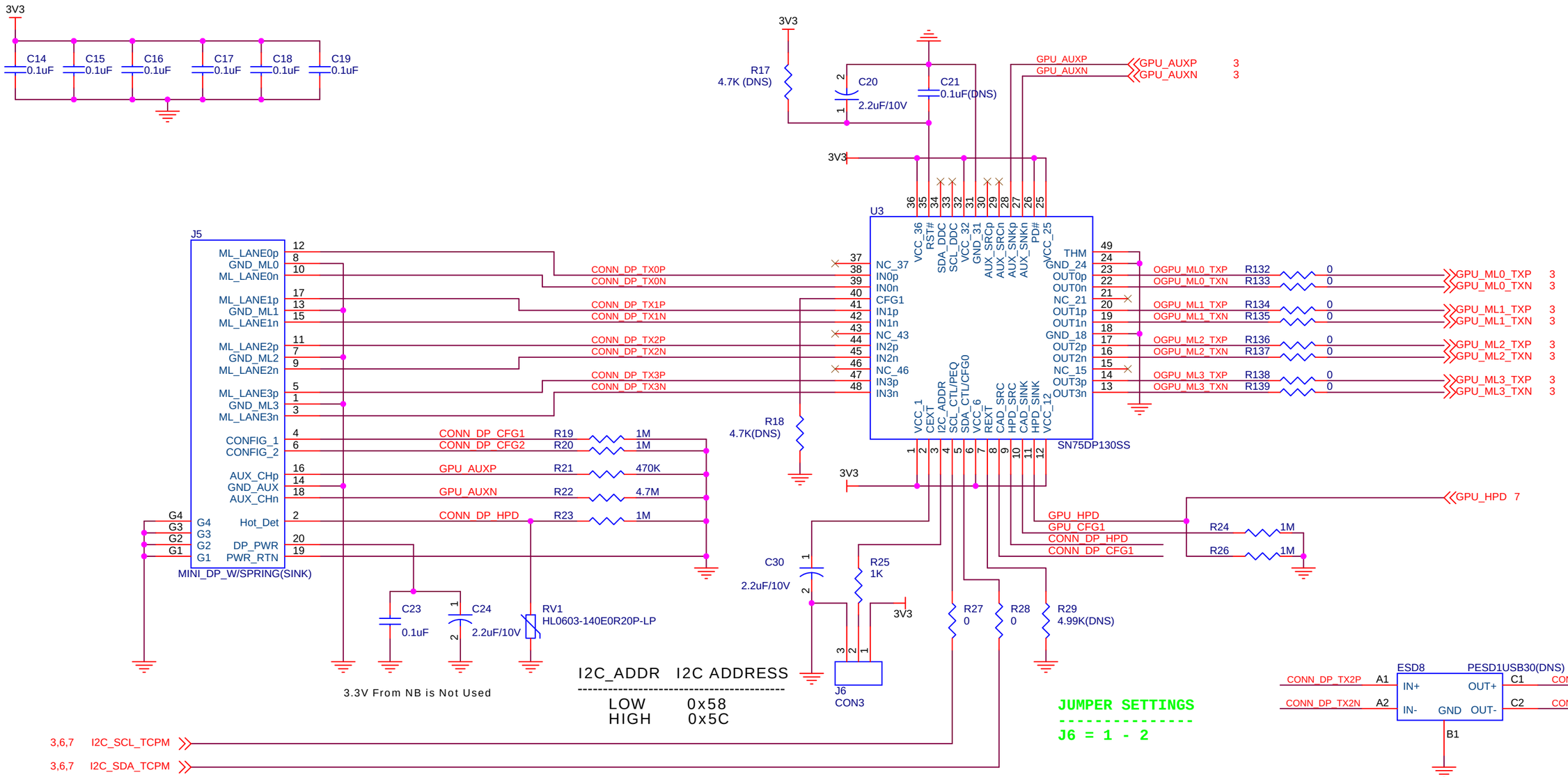
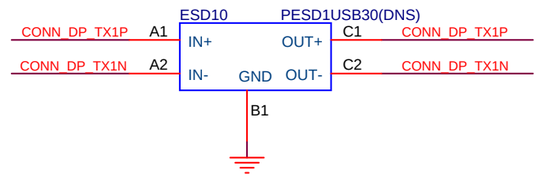


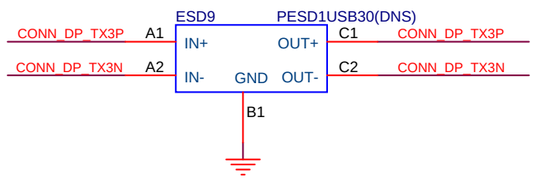
3.3V From NB is Not Used

I2C_ADDR	I2C ADDRESS
LOW	0x58
HIGH	0x5C

JUMPER SETTINGS

J6 = 1 - 2





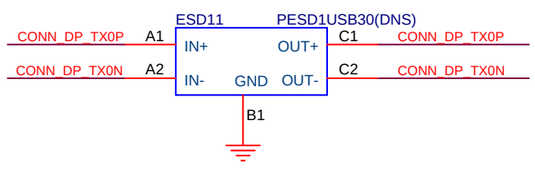


Table 4-11: Upstream Port Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	Out	Hot Plug Detect
3	In	ML_Lane 3 (n)	4	CONFIG (see note 1)	CONFIG1
5	In	ML_Lane 3 (p)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	In	ML_Lane 2 (n)	10	In	ML_Lane 0 (n)
11	In	ML_Lane 2 (p)	12	In	ML_Lane 0 (p)
13	GND	GND	14	GND	GND
15	In	ML_Lane 1 (n)	16	I/O	AUX_CH (p)
17	In	ML_Lane 1 (p)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

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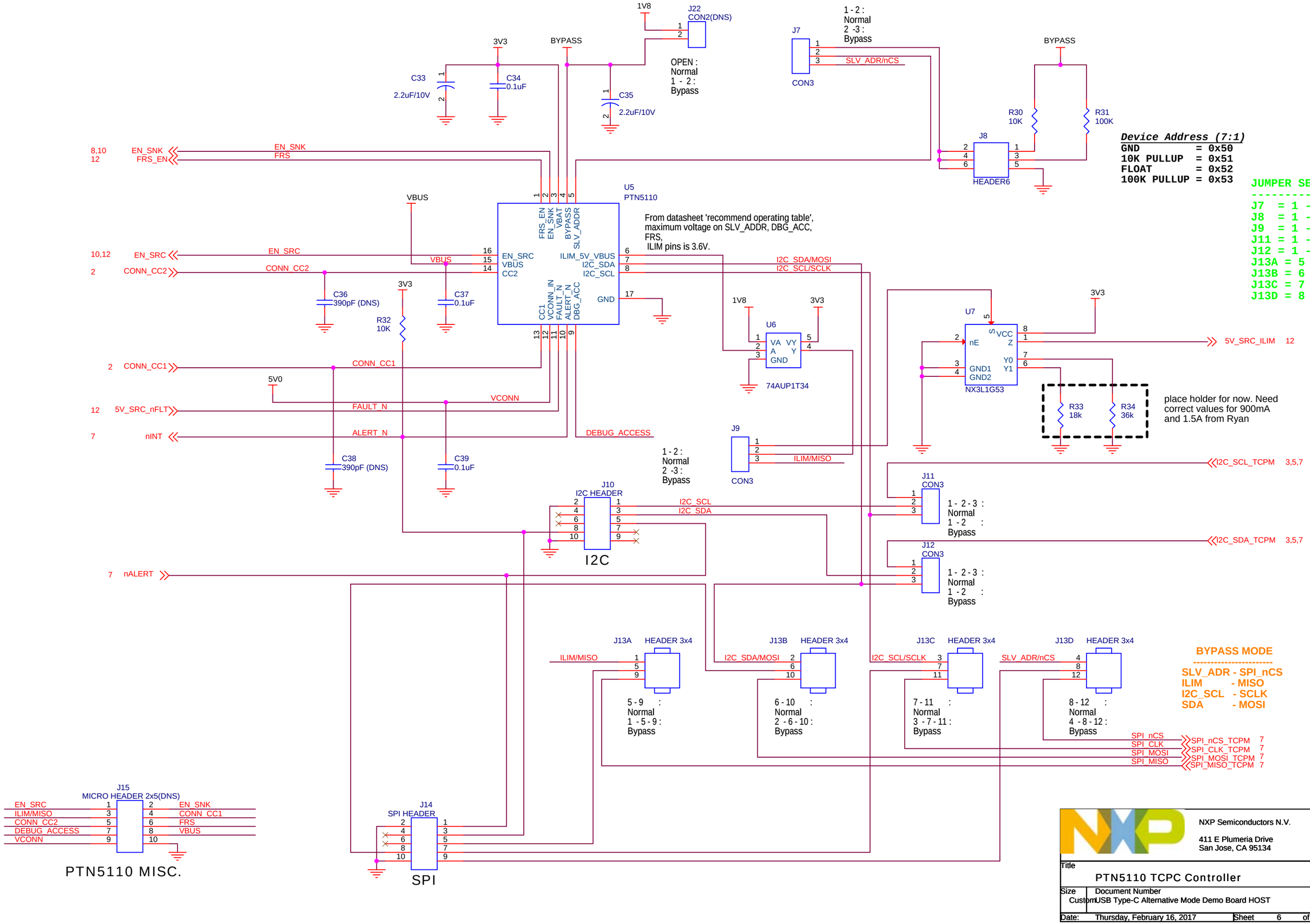
Title	DisplayPort Redriver	
Size B	Document Number USB Type-C Alternative Mode Demo Board HOST	Rev A2
Date: Thursday, February 16, 2017	Sheet 5 of 13	


1V8
J22
CON2(DNS)
OPEN :
Normal
1 - 2 :
Bypass
3V3
BYPASS
C33
2.2uF/10V
C34
0.1uF
C35
2.2uF/10V
J7
CON3
1 - 2 :
Normal
2 -3 :
Bypass
SLV_ADR/nCS
BYPASS
R30
10K
R31
100K
J8
HEADER6
Device Address (7:1)
GND = 0x50
10K PULLUP = 0x51
FLOAT = 0x52
100K PULLUP = 0x53
JUMPER SETTINGS
J7 = 1 - 2
J8 = 1 - 2
J9 = 1 - 2
J11 = 1 - 2 - 3
J12 = 1 - 2 - 3
J13A = 5 - 9
J13B = 6 - 10
J13C = 7 - 9
J13D = 8 - 12
8,10 EN_SNK
12 FRS_EN
EN_SNK
FRS
U5
PTN5110
FRS_EN
EN_SNK
VBAT
BYPASS
SLV_ADDR
From datasheet 'recommend operating table', maximum voltage on SLV_ADDR, DBG_ACC, FRS,
ILIM pins is 3.6V.
VBUS
10,12 EN_SRC
2 CONN_CC2
EN_SRC
CONN_CC2
EN_SRC
VBUS
CC2
ILIM_5V_VBUS
I2C_SDA
I2C_SCL
GND
CC1
VCONN_IN
FAULT_N
ALERT_N
DBG_ACC
I2C_SDA/MOSI
I2C_SCL/SCLK
C36
390pF (DNS)
C37
0.1uF
R32
10K
3V3
1V8
U6
74AUP1T34
U7
NX3L1G53
5V_SRC_ILIM 12
R33
18k
R34
36k
place holder for now. Need correct values for 900mA and 1.5A from Ryan
2 CONN_CC1
CONN_CC1
5V0
VCONN
12 5V_SRC_nFLT
FAULT_N
7 nINT
ALERT_N
DEBUG_ACCESS
C38
390pF (DNS)
C39
0.1uF
J9
CON3
ILIM/MISO
1 - 2 :
Normal
2 -3 :
Bypass
I2C_SCL_TCPM 3,5,7
J11
CON3
1 - 2 - 3 :
Normal
1 - 2 :
Bypass
I2C_SDA_TCPM 3,5,7
J12
CON3
1 - 2 - 3 :
Normal
1 - 2 :
Bypass
J10
I2C HEADER
I2C_SCL
I2C_SDA
I2C
7 nALERT
J13A HEADER 3x4
ILIM/MISO
5 - 9 :
Normal
1 - 5 - 9 :
Bypass
J13B HEADER 3x4
I2C_SDA/MOSI
6 - 10 :
Normal
2 - 6 - 10 :
Bypass
J13C HEADER 3x4
I2C_SCL/SCLK
7 - 11 :
Normal
3 - 7 - 11 :
Bypass
J13D HEADER 3x4
SLV_ADR/nCS
8 - 12 :
Normal
4 - 8 - 12 :
Bypass
BYPASS MODE
SLV_ADR - SPI_nCS
ILIM - MISO
I2C_SCL - SCLK
SDA - MOSI
SPI_nCS
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_nCS_TCPM 7
SPI_CLK_TCPM 7
SPI_MOSI_TCPM 7
SPI_MISO_TCPM 7
J15
MICRO HEADER 2x5(DNS)
EN_SRC
ILIM/MISO
CONN_CC2
DEBUG_ACCESS
VCONN
EN_SNK
CONN_CC1
FRS
VBUS
PTN5110 MISC.
J14
SPI HEADER
SPI
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Title
PTN5110 TCPC Controller
Size
Custom
Document Number
USB Type-C Alternative Mode Demo Board HOST
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A2
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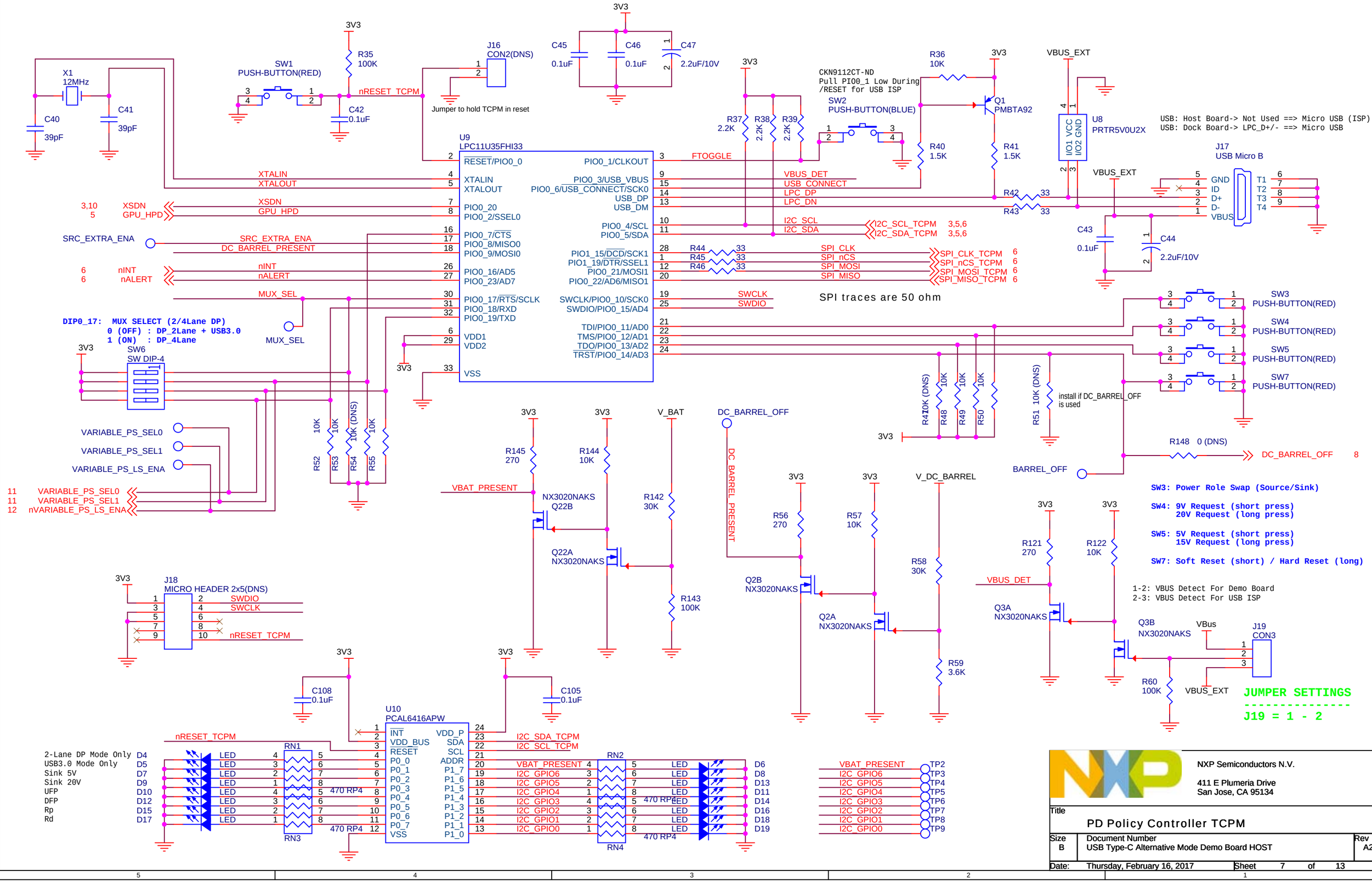
X1
12MHz
C40
39pF
C41
39pF
SW1
PUSH-BUTTON(RED)
R35
100K
C42
0.1uF
nRESET_TCPM
J16
CON2(DNS)
Jumper to hold TCPM in reset
C45
0.1uF
C46
0.1uF
C47
2.2uF/10V
U9
LPC11U35FHI33
RESET/PIO0_0
PIO0_1/CLKOUT
XTALIN
XTALOUT
PIO0_3/USB_VBUS
PIO0_6/USB_CONNECT/SCK0
USB_DP
USB_DM
PIO0_4/SCL
PIO0_5/SDA
PIO1_15/DCD/SCK1
PIO1_19/DTR/SSEL1
PIO0_21/MOSI1
PIO0_22/AD6/MISO1
SWCLK/PIO0_10/SCK0
SWDIO/PIO0_15/AD4
TDI/PIO0_11/AD0
TMS/PIO0_12/AD1
TDO/PIO0_13/AD2
TRST/PIO0_14/AD3
PIO0_20
PIO0_2/SSEL0
PIO0_7/CTS
PIO0_8/MISO0
PIO0_9/MOSI0
PIO0_16/AD5
PIO0_23/AD7
PIO0_17/RTS/SCLK
PIO0_18/RXD
PIO0_19/TXD
VDD1
VDD2
VSS
FTOGGLE
VBUS_DET
USB_CONNECT
LPC_DP
LPC_DN
I2C_SCL
I2C_SDA
SPI_CLK
SPI_nCS
SPI_MOSI
SPI_MISO
SWCLK
SWDIO
XSDN
GPU_HPD
SRC_EXTRA_ENA
DC_BARREL_PRESENT
nINT
nALERT
MUX_SEL
R44 33
R45 33
R46 33
R37 2.2K
R38 2.2K
R39 2.2K
SW2
PUSH-BUTTON(BLUE)
CKN9112CT-ND
Pull PIO0_1 Low During
/RESET for USB ISP
R36
10K
Q1
PMBTA92
R40
1.5K
R41
1.5K
R42 33
R43 33
U8
PRTR5V0U2X
I/O1 VCC
I/O2 GND
VBUS_EXT
J17
USB Micro B
GND
ID
D+
D-
VBUS
USB: Host Board-> Not Used ==> Micro USB (ISP)
USB: Dock Board-> LPC_D+/- ==> Micro USB
C43
0.1uF
C44
2.2uF/10V
SPI traces are 50 ohm
DIP0_17: MUX SELECT (2/4Lane DP)
0 (OFF) : DP_2Lane + USB3.0
1 (ON) : DP_4Lane
SW6
SW DIP-4
VARIABLE_PS_SEL0
VARIABLE_PS_SEL1
VARIABLE_PS_LS_ENA
R52 10K
R53 10K
R54 10K (DNS)
R55 10K
R47 10K (DNS)
R48 10K
R49 10K
R50 10K
R51 10K (DNS)
install if DC_BARREL_OFF
is used
SW3
PUSH-BUTTON(RED)
SW4
PUSH-BUTTON(RED)
SW5
PUSH-BUTTON(RED)
SW7
PUSH-BUTTON(RED)
R148 0 (DNS)
DC_BARREL_OFF
BARREL_OFF
SW3: Power Role Swap (Source/Sink)
SW4: 9V Request (short press)
20V Request (long press)
SW5: 5V Request (short press)
15V Request (long press)
SW7: Soft Reset (short) / Hard Reset (long)
R145 270
R144 10K
R142 30K
R143 100K
VBAT_PRESENT
NX3020NAKS
Q22B
Q22A
NX3020NAKS
V_BAT
DC_BARREL_OFF
DC_BARREL_PRESENT
R56 270
R57 10K
R58 30K
R59 3.6K
Q2B
NX3020NAKS
Q2A
NX3020NAKS
V_DC_BARREL
R121 270
R122 10K
VBUS_DET
Q3A
NX3020NAKS
Q3B
NX3020NAKS
R60 100K
VBus
J19
CON3
VBUS_EXT
1-2: VBUS Detect For Demo Board
2-3: VBUS Detect For USB ISP
JUMPER SETTINGS
J19 = 1 - 2
J18
MICRO HEADER 2x5(DNS)
SWDIO
SWCLK
nRESET_TCPM
C108
0.1uF
C105
0.1uF
U10
PCAL6416APW
INT
VDD_BUS
RESET
P0_0
P0_1
P0_2
P0_3
P0_4
P0_5
P0_6
P0_7
VSS
VDD_P
SDA
SCL
ADDR
P1_7
P1_6
P1_5
P1_4
P1_3
P1_2
P1_1
P1_0
I2C_SDA_TCPM
I2C_SCL_TCPM
VBAT_PRESENT
I2C_GPIO6
I2C_GPIO5
I2C_GPIO4
I2C_GPIO3
I2C_GPIO2
I2C_GPIO1
I2C_GPIO0
RN1
RN2
RN3
RN4
470 RP4
2-Lane DP Mode Only D4
USB3.0 Mode Only D5
Sink 5V D7
Sink 20V D9
UFP D10
DFP D12
Rp D15
Rd D17
D6
D8
D13
D11
D14
D16
D18
D19
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
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PD Policy Controller TCPM
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J23
CON2
VBUS LOAD

Q24
AO4407A (DNS)

Q23
AO4407A (DNS)

R146
100K

R147 10K (DNS)

When there is no VBUS but V_CHRG_IN present (20V from DC barrel), what would happen to the load switch? nEN pin has an internal 1M pull down. Would V_CHRG_IN present on VBUS? No. If 5090 is not enabled, and VINT is higher than VBUS by 45mV, then RCP will be turning on block DC barrel from VBUS.

SINK 5V - 20V @ 5A

U11 NX20P5090UK

VINT1 VINT2 VINT3 VINT4
VBUS1 VBUS2 VBUS3 VBUS4 VBUS5
ACK
OVLO
EN
GND3 GND2 GND1

VBus

C48
4.7uF

C49
0.1uF

C50
0.1uF

23V protection when OVLO = GND

R61 0(DNS)

R62
0

Vovl = Vbus * [(Rt + Rb] / Rb]

3V3

R63
100K

U11_ACK

R64
20K

Q18
PMXB40UNE

6,10 EN_SNK

R65
100K

V_DC_BARREL

R124
100K

R123
30K

nDC_BARREL_ON

NX3020NAKS
Q25B

Q19A
NX3020NAKS

7 DC_BARREL_OFF

R125
3.6K

R126
100K

When we want to charge from USB C
then we need to turn the load switch off

V_CHGR_IN

Q4
AO4407A

D20
PMEG6030ELP
60V, 80uA reverse, 3A

R66
100K

D22
PMEG6030ELP
60V, 80uA reverse, 3A

Q5
AO4407A

R68
100K

SINK DC BARREL

U12 NX20P5090UK

VINT1 VINT2 VINT3 VINT4
VBUS1 VBUS2 VBUS3 VBUS4 VBUS5
ACK
OVLO
EN
GND3 GND2 GND1

C52
0.1uF

C51
10uF

C53
0.1uF

C54
1nF

D21
P6SMB27A

From 20V Wall Charger

J20
PJ-082BH

R67 0(DNS)

R69
100K

U12_ACK

nEN is 29V toler.
1.2V = Vih min

R70
0

R71
100K

D23
PMEG6030ELP
60V, 80uA reverse, 3A
Vf = 500mV

nDC_BARREL_ON

R71 and D23 are used to turn off the load switch when DC barrel is not connected. Diode isolates higher barrel voltage 3.3V

If VBUS is one Vth (~2.2V) more than Vbarrel, then VBUS is driving charger input.

If Vbarrel is one Vgs more than VBUS, then Vbarel is driving charger input.

If VBUS = Vbarrel, then both FETs are off, and both diodes are conducting. Host needs to determine whether VBUS or Vbarrel is used to drive the charger. Then host turns off VBUS or Vbarrel.

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Title
Power Delivery Consumer

Size	Document Number	Rev
Custom	USB Type-C Alternative Mode Demo Board HOST	A2

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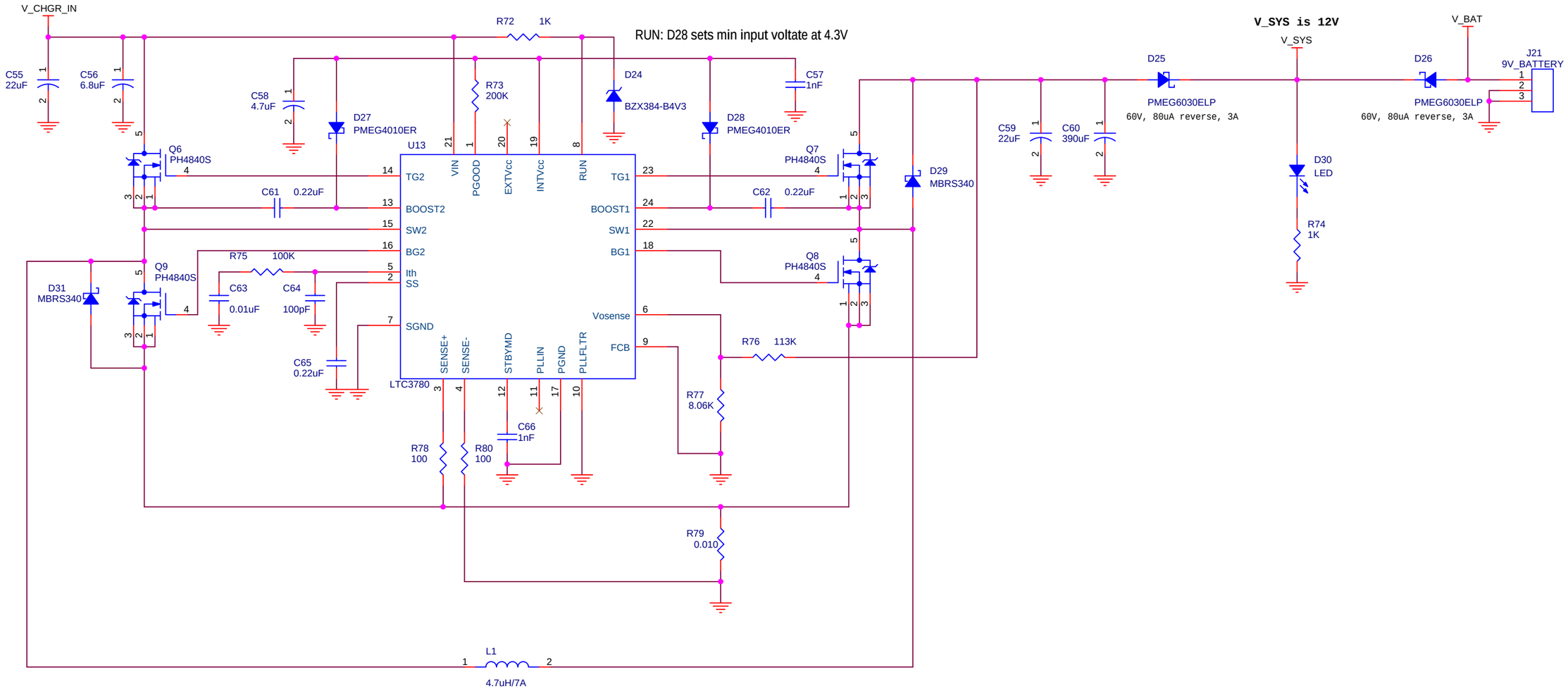

<Variant Name>

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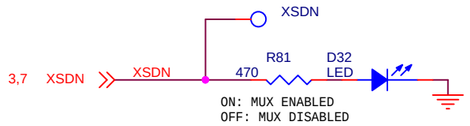
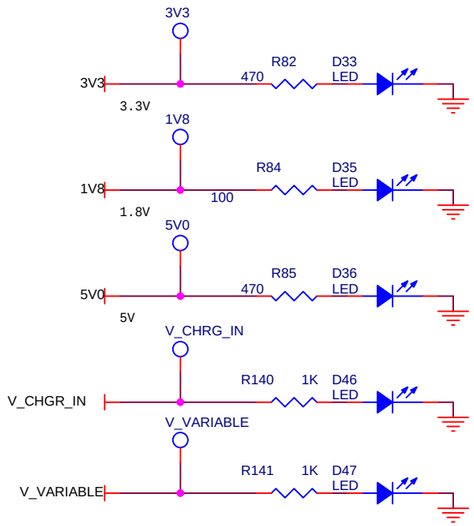
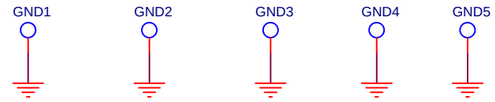
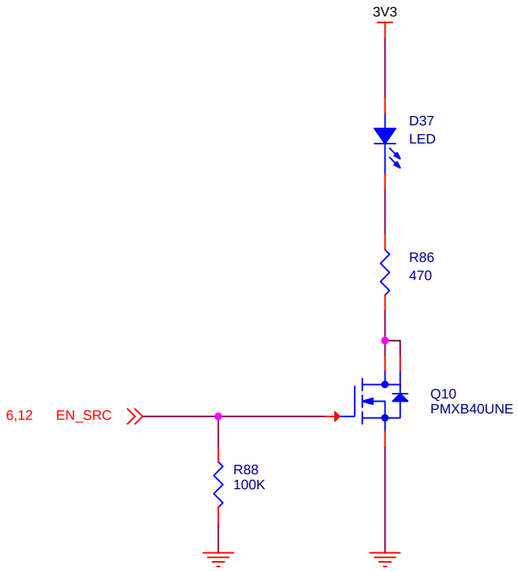
Title: DC Barrel & Charger		
Size: Custom	Document Number: USB Type-C Alternative Mode Demo Board HOST	Rev: A2
Date: Saturday, February 04, 2017	Sheet 9 of 13	

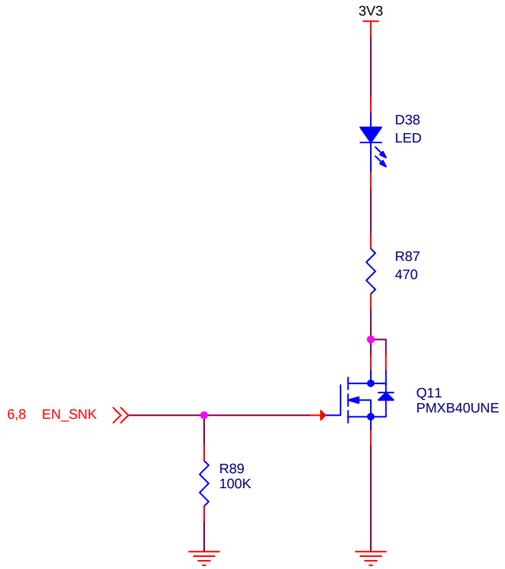






PLACE GND TEST POINTS AROUND THE BOARD





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Title: LEDs		
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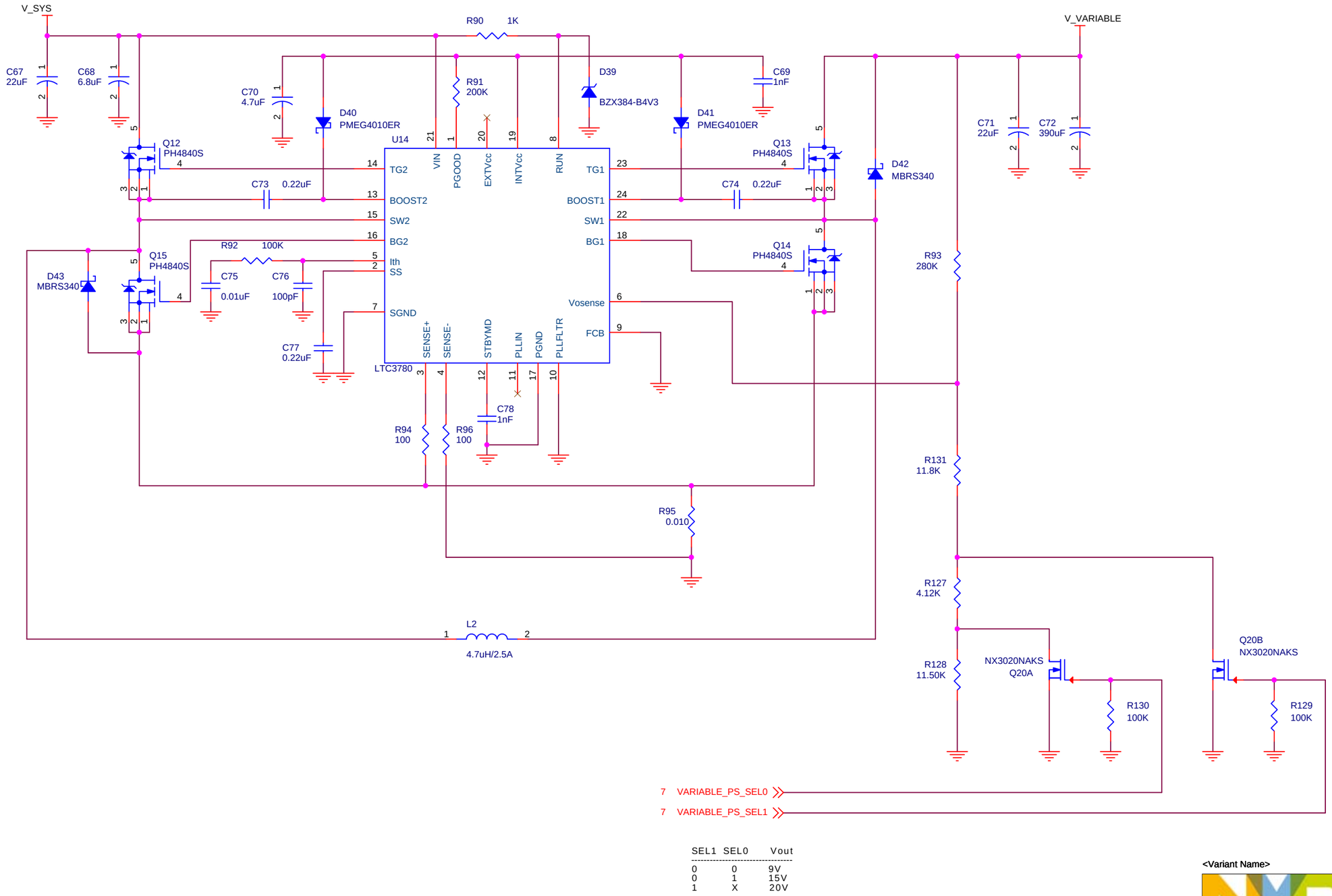

SEL1	SEL0	Vout
0	0	9V
0	1	15V
1	X	20V

<Variant Name>

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Title

Variable Power Supply

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LOAD EITHER SELECT 1
OR SELECT 2

SOURCING
5V

D44 PMEG6030ELP (DNS)
60V, 80uA reverse, 3A

VBus
C79
0.1uF
6 FRS_EN

U15
D1 VBUS1
D2 VBUS2
C2 VBUS3
C4 FO
D4 CAP
GND3 GND2 GND1
D3 C3 B3
EN
NX5P3290
A1 VIN1
A2 VIN2
A4 nFLT
A3 ILIM
B1 VCP1
B2 VCP2
C1 VCP3
B4 EN

5V0
1V8
R97
100K
C80
0.1uF

5V_SRC_nFLT 6
5V_SRC_ILIM 6
EN_SRC 6,10

SELECT 1

U16
NX5P3090A (DNS)
C2 VBUS1
D1 VBUS2
D2 VBUS3
VINT1 B1
VINT2 B2
VINT3 C1
EN
nFAULT
ILIM
A1
A2
A3
GND3 GND2 GND1
D3 C3 B3

5V0

SELECT 2

SOURCING 9V, 15V, 20V

VBus
C81
0.1uF
U17_ACK

U17 NX20P5090UK
A1 VINT1
B1 VINT2
C1 VINT3
D1 VINT4
A2 ACK
EN
GND3 GND2 GND1
E3 D3 C3
VBUS1 B2
VBUS2 C2
VBUS3 D2
VBUS4 E1
VBUS5 E2
OVLO B3

C82
10uF
C83
0.1uF
V_VARIABLE
R101 0(DNS)
R103
0
3V3
R102
100K
R104
100K
R105 0
nVARIABLE_PS_LS_ENA 7

<Variant Name>

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Title
Power Deliver Provider

Size	Document Number	Rev
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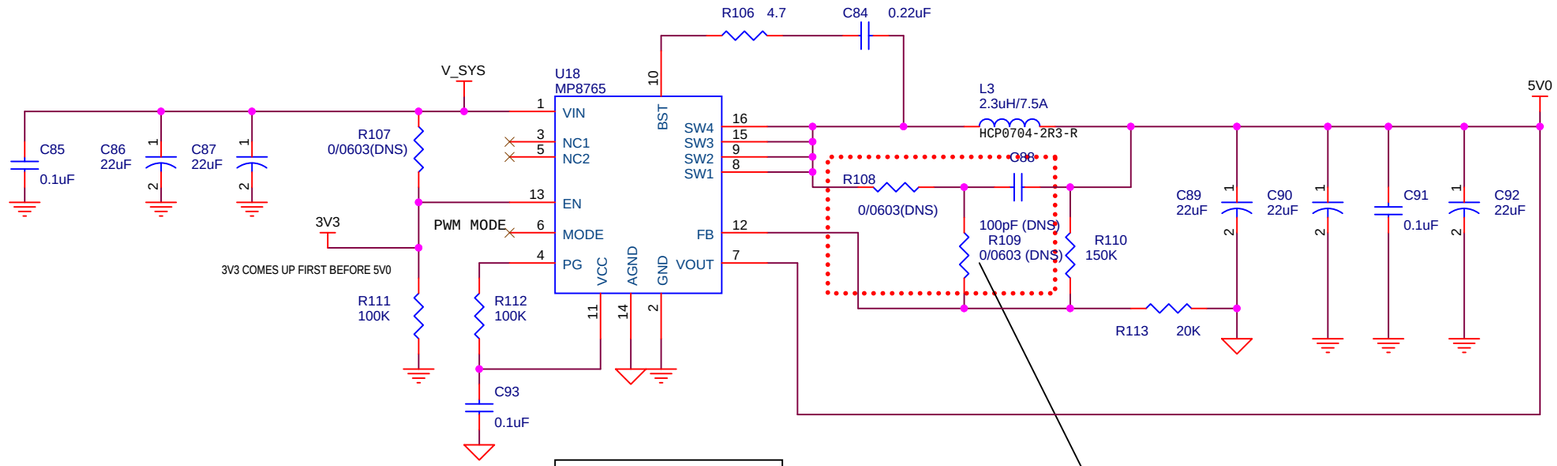
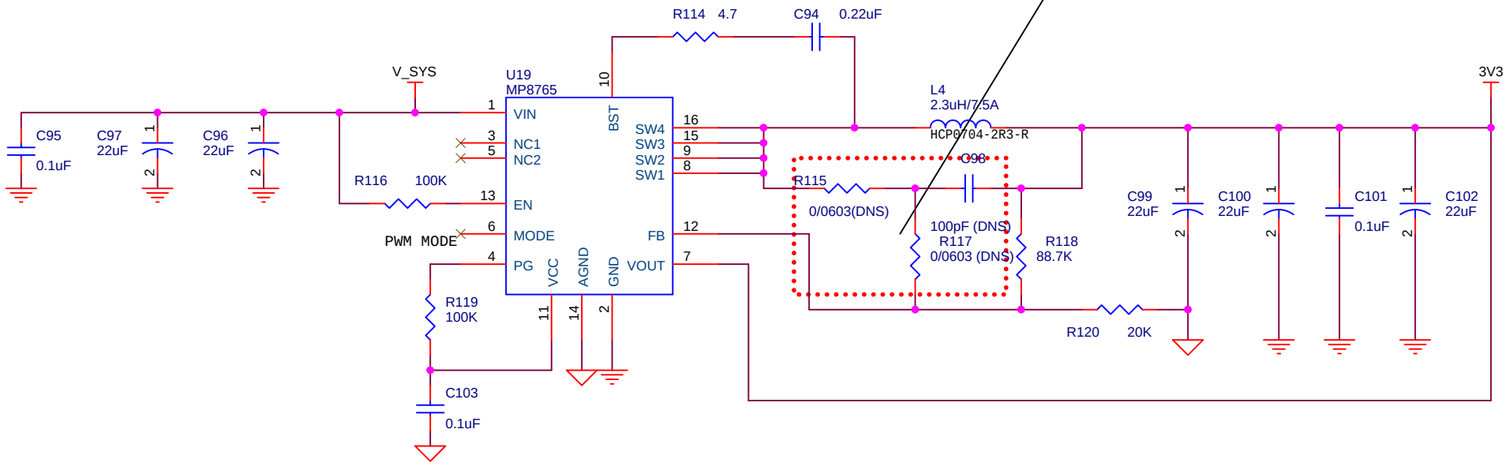
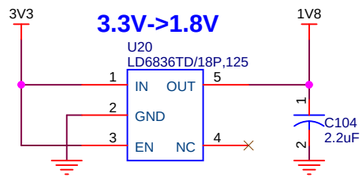


See datasheet for layout example

KELVIN CONNECTION

These are not used for POS cap.
Need them for ceramic cap





Power Up Sequence:

1. 12V (Vsys)
2. 3V3
3. 1V8
4. 5V0

<Variant Name>

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Title: 3V3, 5V0, 1V8 LDO		
Size: Custom	Document Number: USB Type-C Alternative Mode Demo Board HOST	Rev: A1
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