

## N-Channel 20 V (D-S) MOSFET

# PowerPAK® 0806 Single

Top View

**Bottom View** 

Marking Code: C

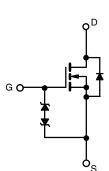
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	20					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.73					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	0.87					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 1.8 \text{ V}$	1.10					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 1.5 \text{ V}$	1.80					
Q <sub>g</sub> typ. (nC)	0.5					
I <sub>D</sub> (A) <sup>a</sup>	1					
Configuration	Single					

#### **FEATURES**

- TrenchFET® power MOSFET
- Ultra small 0.8 mm x 0.6 mm outline
- Ultra thin 0.4 mm max. height
- 100 % R<sub>q</sub> tested
- Typical ESD protection 2000 V (HBM)
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## **APPLICATIONS**

- · Load switch
- · High speed switching
- DC/DC converters
- · For smart phones, tablet PCs and mobile computing
- Small signal switching



RoHS

COMPLIANT

HALOGEN FREE

N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 0806
Lead (Pb)-free and halogen-free	SiUD402ED-T1-GE3

#### Note

The lead finish is NiPdAu and classed as E4 finish

Parameter		Symbol	Limit	Unit	
Drain-source voltage		$V_{DS}$	20	V	
Gate-source voltage		$V_{GS}$	± 8	V	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C		1 a		
	T <sub>A</sub> = 70 °C		0.8 <sup>a</sup>		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	0.35 <sup>b</sup>		
	T <sub>A</sub> = 70 °C		0.28 <sup>b</sup>	Α	
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	1.4		
October a second dela dia dia della second	T <sub>A</sub> = 25 °C		1 <sup>a</sup>		
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	I <sub>s</sub>	0.37 b		
Maximum power dissipation	T <sub>A</sub> = 25 °C		1.25 <sup>a</sup>		
	T <sub>A</sub> = 70 °C		0.8 <sup>a</sup>	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	0.37 b	VV	
	T <sub>A</sub> = 70 °C		0.24 b		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum junction-to-ambient a, d	t < 5 s	D	80	100	°C/W		
Maximum junction-to-ambient b, e	1535	R <sub>thJA</sub>	265	335	] 5/44		

#### **Notes**

- a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s
- a. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering d. Maximum under steady state conditions is 135 °C/W

- Maximum under steady state conditions is 400 °C/W



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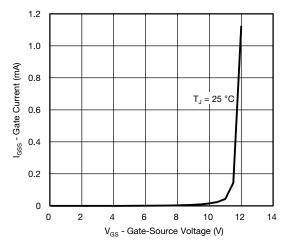
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)         Parameter       Symbol       Test Conditions       Min.       Typ.       Max.								
Static	Syllibol	rest Conditions	141111.	Typ.	IVIAA.	Unit		
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20	_	_	V		
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	VGS = 0 V, 1β = 200 μ/ (	-	18	_	mV/°C		
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		-1.9				
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.4	-	0.9	V		
	V GS(th)	$V_{DS} = V_{GS}$ , $V_{DS} = 230  \text{ps}$ V <sub>DS</sub> = 0 V, $V_{GS} = \pm 4.5  \text{V}$	-	_	± 0.5	· ·		
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$		_	± 10	-		
		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}$		_	1	μΑ		
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$		_	10	A		
On-state drain current <sup>a</sup>	ler v	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, 1J = 33 \text{ C}$ $V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	1	_	10			
On-State drain current	I <sub>D(on)</sub>	$V_{DS} \ge 3 \text{ V}, V_{GS} = 4.3 \text{ V}$ $V_{GS} = 4.5 \text{ V}, I_D = 0.2 \text{ A}$	<u>'</u>	0.57	0.73			
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.2 A V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 0.1 A		0.57	0.73	1		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 2.3 \text{ V, } I_D = 0.1 \text{ A}$ $V_{GS} = 1.8 \text{ V, } I_D = 0.02 \text{ A}$	<u> </u>	0.80	1.10	Ω		
		V <sub>GS</sub> = 1.6 V, I <sub>D</sub> = 0.02 A V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 0.01 A		0.80	1.10	-		
Forward transconductance a	~			1.2	1.00	S		
Dynamic b	9fs	$V_{DS} = 10 \text{ V}, I_D = 0.2 \text{ A}$		1.2		3		
				16	1	1		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz			-			
Output capacitance	Coss	$v_{DS} = 10 \text{ v}, v_{GS} = 0 \text{ v}, 1 = 1 \text{ MHz}$	-	7.5	-	pF		
Reverse transfer capacitance	C <sub>rss</sub>	V 10 V V 0 V I 0 0 A		3.5	1.00	1		
Total gate charge	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 8 \text{ V}, I_{D} = 0.2 \text{ A}$		0.75	1.20	nC		
Cata aguiras abarras	0			1	0.75			
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 0.2 \text{ A}$	-	0.09	-			
Gate-drain charge	Q <sub>gd</sub>	f 1 MH=	-	0.09	-			
Gate resistance	R <sub>g</sub>	f = 1 MHz	3	24	50	Ω		
Turn-on delay time	t <sub>d(on)</sub>	-	-	7	15	4		
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 50 \Omega$ $I_D \cong 0.2 \text{ A}, V_{GEN} = 4.5 \text{ V}, Rg = 1 \Omega$	-	10	20	_		
Turn-off delay time	t <sub>d(off)</sub>	$ID = 0.2 \text{ A}, V_{GEN} = 4.3 \text{ V}, GEN = 1.22$	-	23	50	ns		
Fall time	t <sub>f</sub>		-	7	15			
Turn-on delay time	t <sub>d(on)</sub>		-	5	10			
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 15 \Omega$	-	5	10			
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 0.2 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$	-	11	25			
Fall time	t <sub>f</sub>		-	5	10			
Drain-Source Body Diode Characteristic				T	T	T		
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	1 <sup>c</sup>	Α		
Pulse diode forward current	I <sub>SM</sub>		-	-	1.4			
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.2 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V		
Body diode reverse recovery time	t <sub>rr</sub>	_	-	11	25	ns		
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 0.2 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	3.5	7	nC		
Reverse recovery fall time	ta	, 512 / , divat = 100 / t po, 15 = 20 0	-	5.3	-	ns		
Reverse recovery rise time	t <sub>b</sub>		-	5.7	-	113		

#### Note

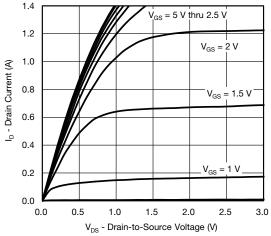
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing
- c. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

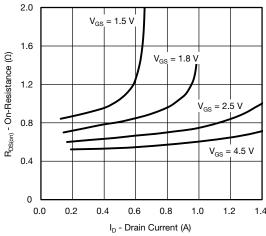




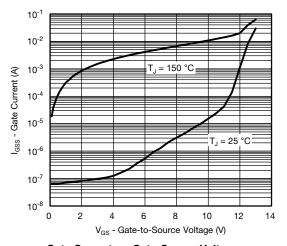
#### Gate Current vs. Gate-Source Voltage



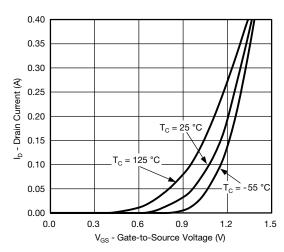
**Output Characteristics** 



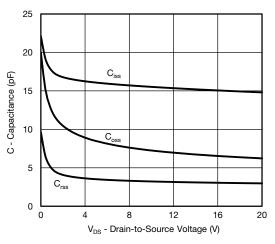
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage

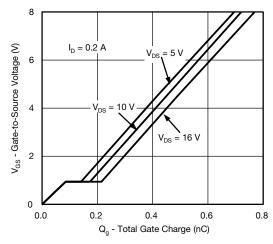


**Transfer Characteristics** 

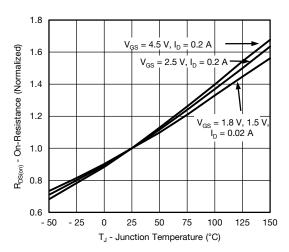


Capacitance vs. Drain-to-Source Voltage

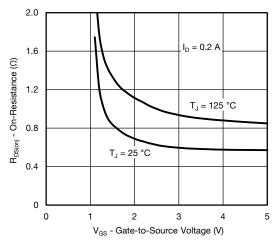




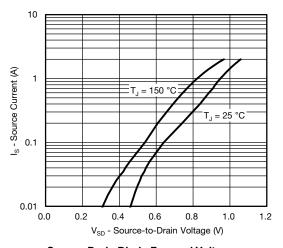
#### **Gate Charge**



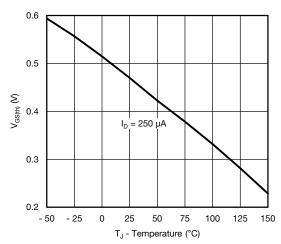
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

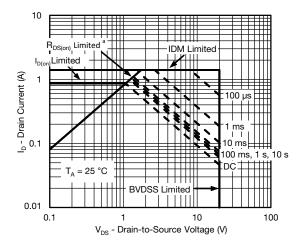


#### Source-Drain Diode Forward Voltage

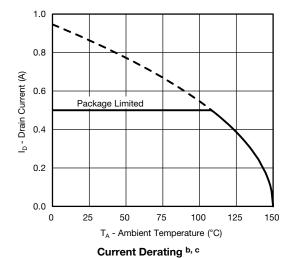


**Threshold Voltage** 



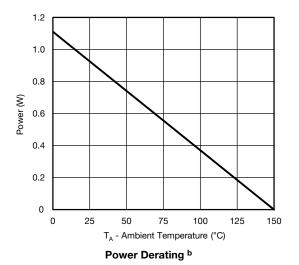


#### Safe Operating Area (Junction-to-Ambient) <sup>b</sup>



4.0 3.0 1.0 0.0 0.0001 0.001 0.01 0.1 1 10 100 1000 Time (s)

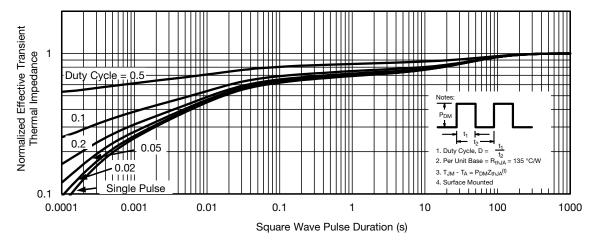
Single Pulse Power, Junction-to-Ambient b



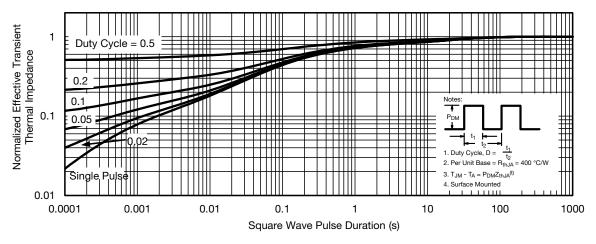
#### Note

- a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified
- b. When mounted on 1" x 1" FR4 with full copper
- c. The power dissipation  $P_D$  is based on  $T_J$  (max.) = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient <sup>a</sup>



Normalized Thermal Transient Impedance, Junction-to-Ambient <sup>a</sup>

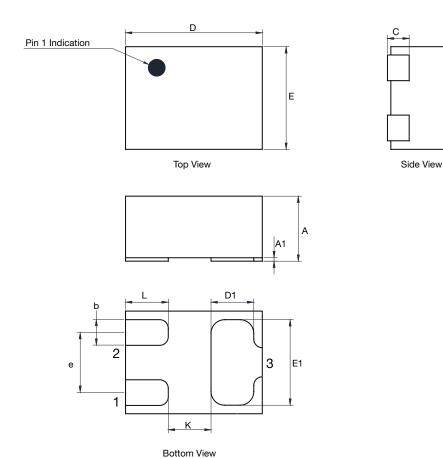
#### Note

a. When mounted on 1" x 1" FR4 with minimum copper

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## Case Outline for PowerPAK 0.8 mm x 0.6 mm



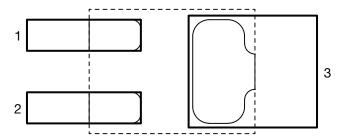
	MILLIMETERS			INCHES		
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	0.350	0.380	0.400	0.0138	0.0150	0.0157
A1	0	-	0.020	0	-	0.0008
b	0.120	0.150	0.180	0.0047	0.0059	0.0071
С	0.119	0.127	0.135	0.0047	0.0050	0.0053
D	0.750	0.800	0.850	0.0295	0.0315	0.0335
D1	0.200	0.250	0.300	0.0078	0.0098	0.0118
E	0.550	0.600	0.650	0.0217	0.0236	0.0256
E1	0.450	0.500	0.550	0.0177	0.0197	0.0217
е	0.300	0.350	0.400	0.0118	0.0138	0.0158
K	0.150	0.250	0.350	0.0058	0.0098	0.0138
Ĺ	0.200	0.250	0.300	0.0078	0.0098	0.0118

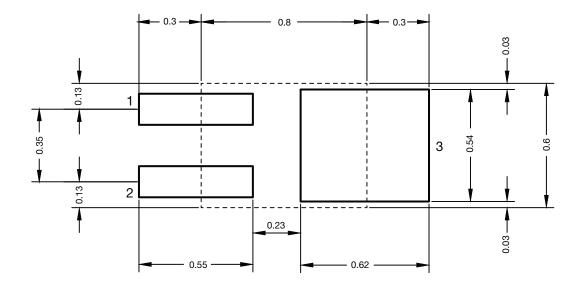
ECN: C13-1574-Rev. A, 23-Dec-13

DWG: 6020



## Recommended Land Pattern PowerPAK® 0806







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Vishay

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