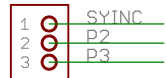
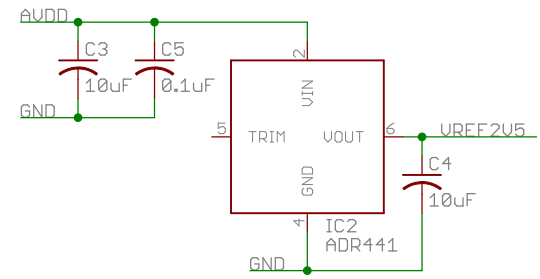


J1

Note: The voltage applied to DVDD must be kept between 3.0V and 5.25V in order to avoid damaging the parts used in this circuit.

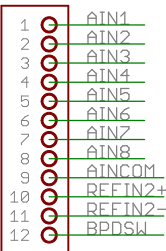


J3

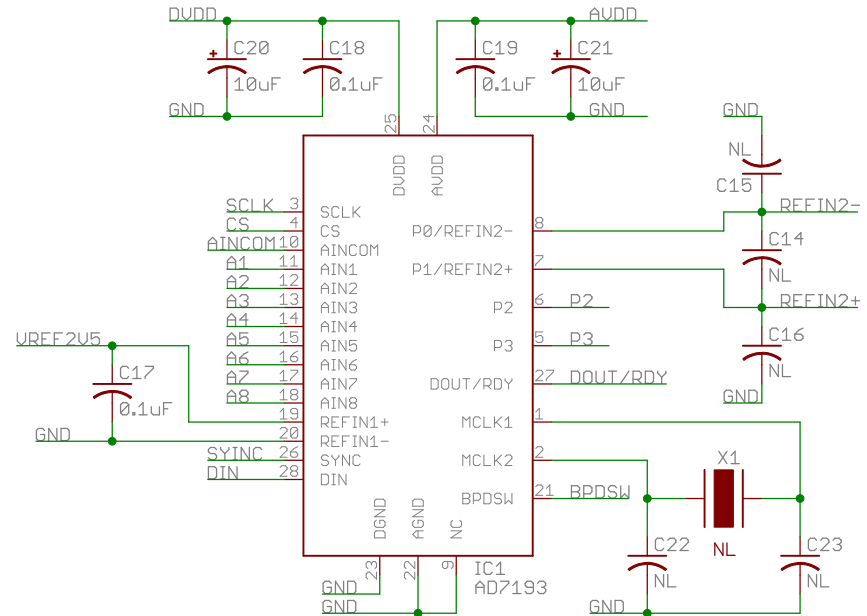
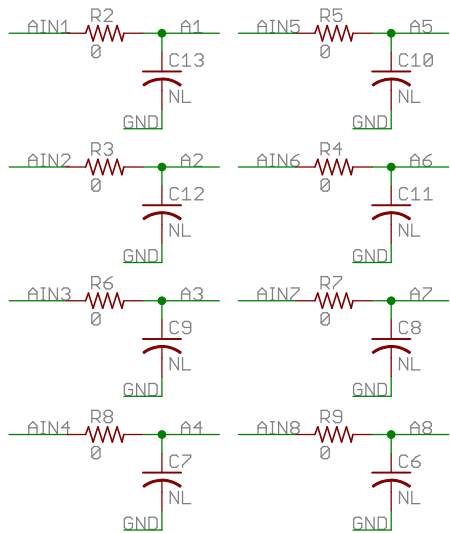
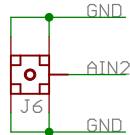
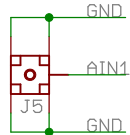


J4

Note: Any external voltage applied to AVDD must be kept between 3.0V and 5.25V in order to avoid damaging the parts used in this circuit.



J2



Note: By default X1, C22, and C23 are not loaded and the AD7193 should be configured to use the on-chip 4.92 MHz clock. To provide an external clock to the AD7193, install an 18pF 11.40mm x 4.80mm (HC49/US) crystal for X1 and 6 pF capacitors for C22 and C23. The pads on the PCB were originally designed for a TXC Corporation 9C-4.9152MAAJ-T crystal but they will accommodate other similarly sized crystals.

For more information on the parts used in this design, please refer to:
www.analog.com/AD7193 - 4-Channel, 4.8 KHz, Ultralow Noise, 24-Bit Sigma-Delta ADC with PGA
www.analog.com/ADR441 - Ultralow Noise, LDO XFET 2.5 Volt Reference

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